# Advanced Features and Techniques of Embedded Systems Design

Embedded Hardware 4

EMBD-ADVHW-ILT (v1.0)

**Course Specification**

## Course Description

*Advanced Features and Techniques of Embedded Systems Design* provides embedded systems developers the necessary skills to develop complex embedded systems and enables them to improve their designs by using the tools available in the Vivado® IP Integrator. This course also helps developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq® System on a Chip (SoC), Zynq UltraScale+™ MPSoC, and/or MicroBlaze™ soft processor.

This course builds on the skills gained in the *Embedded Systems Design* course. Labs provide hands-on experience with developing, debugging, and simulating an embedded system. Utilizing memory resources and implementing high-performance DMA are also covered. Labs use demo boards in which designs are downloaded and verified.

**Level** – Embedded Hardware 4

**Course Duration** – 2 days

**Course Part Number** – EMBD-ADVHW-ILT

**Who Should Attend?** – Hardware, firmware, and system design engineers who are interested in Xilinx embedded systems development flow

**Prerequisites**

- *Embedded Systems Development* course or experience with embedded systems design and the Vivado Design Suite
- Basic C programming
- Working knowledge of the Zynq SoC (Cortex™-A9 processor), Zynq UltraScale+ MPSoC processors (Cortex-A53 or Cortex-R5 processors), or MicroBlaze processor

**Software Tools**

- Vivado Design or System Edition 2017.3

**Hardware**

- Architecture: Zynq-7000 SoC, Zynq UltraScale+ MPSoC*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*, QEMU

* This course focuses on the Zynq-7000 SoC, Zynq UltraScale+ MPSoC, and MicroBlaze processor architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations. Zynq UltraScale+ MPSoC designs target QEMU rather than a specific board.

After completing this comprehensive training, you will have the necessary skills to:

- Assemble an advanced embedded system
- Take advantage of the various features of the Zynq SoC, Zynq UltraScale+ MPSoC, and Cortex and MicroBlaze processors, including the AXI interconnect, and the various memory controllers
- Apply advanced debugging techniques, including the use of the Vivado logic analyzer tool for debugging an embedded system and HDL system simulation of processor-based designs
- Identify the steps involved in integrating a memory controller into an embedded system using the Cortex and MicroBlaze processors
- Integrate an interrupt controller and interrupt handler into an embedded design
- Design a flash memory-based system and boot load from off-chip flash memory
- Perform HDL-based system simulation

## Course Outline

**Day 1**

- Overview of Embedded Hardware Development {Demo}
- Hardware-Software Flow {Lab}
- Software Overview
- Zynq-7000 SoC Architecture Overview {Lab, Demo}
- MicroBlaze Processor Architecture Overview {Lab}
- Zynq UltraScale+ MPSoC Architecture Overview {Lab, Demo}
- Debugging
  - Hardware Introduction {Demo}
  - Hardware - Marking Nets {Lab}
  - Hardware-Software Co-Debugging (Cross-Triggering) {Lab}
- Memory Types
  - Memory Overview
  - Block RAM Controllers
  - Static Memory Controllers
  - DDRx Memory Operation
  - Dynamic Memory Controller (Zynq-7000 Device)
- Interrupt Concepts
  - Introduction to Interrupts
  - Interrupts and the Zynq-7000 Device
  - General Interrupt Controller
  - Interrupts and the MicroBlaze Processor
  - AXI Interrupt Controller for the MicroBlaze Processor

**Day 2**

- AXI Concepts
  - AXI Streaming: Introduction
  - MicroBlaze Processor Streaming Ports
  - AXI Streaming FIFO
  - Connecting AXI IP {Demo}
  - DMA
- Zynq-7000 Device PS-PL Interface {Demo}
- PS Peripherals
  - High-Speed: USB
  - High-Speed: Gigabit Ethernet {Lab}
  - Low-Speed: Overview {Lab}
  - Low-Speed: CAN {Demo}
  - Low-Speed: I2C
  - Low-Speed: SD/SDIO
  - Low-Speed: SPI
  - Low-Speed: UART {Demo}
- Utility Logic
- Sharing PS Resources (Hardware Perspective) {Lab}
- Multi-Processor Hardware Architecture
- Caching
- Processor Caching and SCLR
- Accelerator Coherency Port
- Booting
  - Flow
  - PL {Lab}
  - Flash Image Generation
- QEMU: Introduction {Demo}

## Topic Descriptions

**Day 1**

- Overview of Embedded Hardware Development – Provides an overview of embedded hardware development.
- Hardware-Software Flow – Illustrates how design information generated during the hardware development process is moved into the SDK tool realm.
- Software Overview – Provides a thorough understanding of how the integrated design environment works, including how the compiler and linker behave, basics of makefiles, DMA usage, and variable scope.

- Zynq-7000 SoC Architecture Overview – Overview of the Zynq-7000 SoC architecture.
- MicroBlaze Processor Architecture Overview – Overview of the MicroBlaze microprocessor architecture.
- Zynq UltraScale+ MPSoC Architecture Overview – Overview of the Zynq UltraScale+ MPSoC architecture.
- Debugging
  - Hardware Introduction – Introduces the need and offers a solution for in-chip testing of hardware designs.
  - Hardware - Marking Nets – Reviews the process of marking nets to show which signals should be monitored without having to explicitly instantiate ILA cores.
  - Hardware-Software Co-Debugging (Cross-Triggering) – Describes how to enable events in hardware to pause the software execution and breakpoints in software to cause an ILA trigger.
- Memory Types
  - Memory Overview – Provides a brief overview of the different types of memory available, as well as when one type of memory would be selected over another.
  - Block RAM Controllers – Introduces two versions of block RAM controllers and how and why they are needed.
  - Static Memory Controllers – Discusses static memory controllers in general and the SMC implementation in the Zynq-7000 family of devices.
  - DDRx Memory Operation – Provides additional details regarding how DDRx memory interfaces with a controller.
  - Dynamic Memory Controller (Zynq-7000 Device) – Covers how the DMC is implemented as well as many of its key behaviors.
- Interrupt Concepts
  - Introduction to Interrupts – Introduces the concept of interrupts, basic terminology, and generic implementation.
  - Interrupts and the Zynq-7000 Device – Presents the details of how the Zynq-7000 platform uses interrupts from both a hardware and software perspective.
  - General Interrupt Controller – Introduces the general interrupt controller (GIC), its features, and some examples of its use.
  - Interrupts and the MicroBlaze Processor – Describes how interrupts are handled within the MicroBlaze processor system from a hardware perspective.
  - AXI Interrupt Controller for the MicroBlaze Processor – Introduces the AXI Interrupt Controller, which augments the MicroBlaze processor's interrupt capabilities by managing multiple interrupt sources.

**Day 2**

- AXI Concepts
  - AXI Streaming: Introduction – Provides the context and background for the the streaming configuration of the AXI protocol.
  - MicroBlaze Processor Streaming Ports – Describes and illustrates how data streaming is performed using the MicroBlaze processor.
  - AXI Streaming FIFO – Introduces the AXI Streaming FIFO and its capabilities.
  - Connecting AXI IP – Focuses on the relationships between different types of AXI interfaces and how they can be connected to form hierarchies.
  - DMA – Introduces various IP that supports DMA and DMA-like functionality.
- Zynq-7000 Device PS-PL Interface – Discusses the various connection points between the PS and PL.
- PS Peripherals
  - High-Speed: USB – Introduces the USB high-speed peripheral.
  - High-Speed: Gigabit Ethernet – Introduces the Gigabit Ethernet high-speed peripheral.
  - Low-Speed: Overview – Introduces the low-speed peripherals in the Zynq SoC.
  - Low-Speed: CAN – Introduces the CAN low-speed peripheral.
  - Low-Speed: I2C – Introduces the I2C low-speed peripheral.
  - Low-Speed: SD/SDIO – Introduces the SD/SDIO low-speed peripheral.
  - Low-Speed: SPI – Introduces the SPI low-speed peripheral.
  - Low-Speed: UART – Introduces the UART low-speed peripheral.
- Utility Logic – Covers the IP that provides basic logic support within the block design.
- Sharing PS Resources (Hardware Perspective) – Illustrates from the hardware design perspective how a master in the PL can leverage resources within the PS.
- Multi-Processor Hardware Architecture – Addresses some of the mechanisms that a designer canleverage to support cross-processor communications.
- Caching – Introduces the concept of caching and describes how this technique is implemented using the Xilinx processor systems.
- Processor Caching and SCLR – Introduces the concepts behind processing caching and the System-Level Control Register.
- Accelerator Coherency Port – Describes the purpose and general behavior of the accelerator coherency port (ACP).
- Booting
  - Flow – Provides a low-level view of the booting process.
  - PL – Introduces the concepts behind configuring the PL at boot.
  - Flash Image Generation – Introduces the Flash Image Generator tool, which is used to collect up a variety of files and order them properly in the Flash so that the FSBL can correctly read them.
- QEMU: Introduction – Introduction to the Quick Emulator, which is the tool used to run software for the Zynq device when hardware is not available.

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