Introduction to the Zynq All Programmable SoC Architecture

Embedded Hardware and Firmware 3

INTRO-ZARCH-ILT (v1.0)

Course Specification

Course Description

This course provides hardware and firmware engineers with the knowledge to effectively utilize a Zynq® All Programmable System on a Chip (SoC). It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL).

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Hardware and Firmware 3

Course Duration – 1 day

Course Part Number – INTRO-ZARCH-ILT

Who Should Attend? – Hardware and firmware engineers who are interested in implementing a system on a chip using the Zynq All Programmable SoC and programmable logic.

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Evaluate a processing system (PS) and programmable logic (PL) AXI interface
- Identify the boot options for the Zynq All Programmable SoC

Course Outline

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1:** Building a Zynq All Programmable SoC Platform
- Zynq All Programmable SoC PS-PL Interface
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- **Lab 3:** Impact of Port Selection on System Performance
- Zynq All Programmable SoC Booting
- Zynq All Programmable SoC Memory Resources
- **Lab 4:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

Lab Descriptions

- **Lab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **Lab 2:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 3:** Impact of Port Selection on System Performance – Explore bandwidth issues surrounding the use of the Accelerator Coherency Port (ACP) and the High Performance (HP) ports.
- **Lab 4:** Running and Debugging a Linux Application on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.

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