Introduction to the Zynq All Programmable SoC Architecture

Embedded Hardware and Firmware 3

INTRO-ZARCH-ILT (v1.0)

Course Specification

Course Description

This course provides hardware and firmware engineers with the knowledge to effectively utilize a Zynq® All Programmable System on a Chip (SoC). It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL).

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Hardware and Firmware 3

Course Duration – 1 day

Course Part Number – INTRO-ZARCH-ILT

Who Should Attend? – Hardware and firmware engineers who are interested in implementing a system on a chip using the Zynq All Programmable SoC and programmable logic.

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2017.3

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Evaluate a processing system (PS) and programmable logic (PL) AXI interface
- Identify the boot options for the Zynq All Programmable SoC

Course Outline

- Zynq All Programmable SoC Overview {Lecture, Demo}
- Zynq All Programmable SoC Application Processor Unit (APU) {Lecture, Lab}
- Zynq All Programmable SoC Processor Input/Output Peripherals {Lecture, Demo}
- Zynq All Programmable SoC PS-PL Interface {Lecture, Demo, Lab}
- Zynq All Programmable SoC Booting {Lecture, Lab}
- Zynq All Programmable SoC Memory Resources {Lecture, Demo}

Topic Descriptions

- Zynq All Programmable SoC Overview – Provides a general overview of the Zynq All Programmable SoC.
- Zynq All Programmable SoC Application Processor Unit (APU) – Explores the individual components that comprise the APU.
- Zynq All Programmable SoC Processor Input/Output Peripherals – Introduces the components that comprise the IOP block of the Zynq device PS.
- Zynq All Programmable SoC PS-PL Interface – Describes in detail the PS interconnect and how it affects PL architecture decisions.
- Zynq All Programmable SoC Booting – Explains the boot process of the PC and configuration of the PL.
- Zynq All Programmable SoC Memory Resources – Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS.

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