

## Course Description

The Xilinx Zynq® System on a Chip (SoC) provides a new level of system design capabilities. This course provides system architects with the knowledge to effectively architect a Zynq SoC.

This course presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq SoC.

The course details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

**Level** – Embedded Architect 3

**Course Duration** – 2 days

**Course Part Number** – EMBD-ZSA-ILT

**Who Should Attend?** – System architects who are interested in architecting a system on a chip using the SoC.

#### Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

#### Software Tools

- Vivado® Design or System Edition 2017.3

#### Hardware

- Architecture: Zynq-7000 SoC\*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard\*

\* This course focuses on the Zynq-7000 SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

## Course Outline

### Day 1

- Overview {Demo}
- Application Processor Unit (APU) {Lab}
- Neon Co-Processor
- Input/Output Peripherals {Demo}
- PS Peripherals
  - Low-Speed: Overview {Lab}
  - Low-Speed: UART {Demo}
  - Low-Speed: CAN {Demo}
  - Low-Speed: I2C
  - Low-Speed: SD/SDIO
  - Low-Speed: GPIO

- High-Speed: USB
- High-Speed: Gigabit Ethernet {Lab}
- DMA Controller (DMAC) {Lab}
- DMA
  - Introduction and Features
  - Block Design and Interrupts
  - Read and Write

### Day 2

- AXI
  - Introduction
  - Variations
  - Transactions {Demo, Lab}
- PS-PL Interface {Demo, Lab}
- Booting {Lab}
- Memory Resources {Demo}
- Meeting Performance Goals {Lab}
- Hardware Design {Lecture}
- Software Design {Demo, Lab}
- Debugging {Lab}
- Tools and Reference Designs

## Topic Descriptions

### Day 1

- Overview – Provides a general overview of the Zynq SoC.
- Application Processor Unit (APU) – Explores the individual components that comprise the APU.
- Neon Co-Processor – Describes the Neon co-processor that is the companion to each Cortex-A9 processor.
- Input/Output Peripherals – Introduces the components that comprise the IOP block of the Zynq device PS.
- Peripherals
  - Low-Speed: Overview – Introduces the low-speed peripherals in the Zynq SoC.
  - Low-Speed: UART – Introduces the UART low-speed peripheral.
  - Low-Speed: CAN – Introduces the CAN low-speed peripheral.
  - Low-Speed: I2C – Introduces the I2C low-speed peripheral.
  - Low-Speed: SD/SDIO – Introduces the SD/SDIO low-speed peripheral.
  - Low-Speed: GPIO – Introduces the GPIO low-speed peripheral.
  - High-Speed: USB – Introduces the USB high-speed peripheral.
  - High-Speed: Gigabit Ethernet – Introduces the Gigabit Ethernet high-speed peripheral.
- DMA Controller (DMAC) – Explores the operation of the DMAC, which is located in the APU.
- DMA
  - Introduction and Features – Introduces the direct memory access controller.
  - Block Design and Interrupts – Introduces the DMA block design and the DMA interrupts.
  - Read and Write – Introduces the concepts behind DMA reading and writing.

### Day 2

- AXI
  - Introduction – Introduces the AXI protocol.
  - Variations – Describes the differences and similarities among the three primary AXI variations.
  - Transactions – Describes different types of AXI transactions.
- PS-PL Interface – Describes in detail the PS interconnect and how it affects PL architecture decisions.

- **Booting** – Explains the boot process of the PC and configuration of the PL.
- **Memory Resources** – Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS.
- **Meeting Performance Goals** – Focuses on Zynq device performance, including DDR access from the PL, DMA considerations, and power control and reduction techniques.
- **Hardware Design** – Discusses the use and configuration of the PS in a hardware design.
- **Software Design** – Explores the software side of the Zynq device.
- **Debugging** – Introduces debug tools and methodology on the Zynq SoC.
- **Tools and Reference Designs** – Describes Xilinx-provided reference design platforms, use cases, and third-party operating systems and tools for the Zynq SoC.

## Register Today

Xilinx's network of Authorized Training Providers (ATP) delivers public and private courses in locations throughout the world. Please contact your closest ATP for more information, to view schedules, or to register online.

Visit [www.xilinx.com/training](http://www.xilinx.com/training) and click on the region where you want to attend a course.

**Americas**, contact your training provider at [www.xilinx.com/training/atp.htm#NA](http://www.xilinx.com/training/atp.htm#NA) or send your inquiries to [registrar@xilinx.com](mailto:registrar@xilinx.com).

**Europe**, contact your training provider at [www.xilinx.com/training/atp.htm#EU](http://www.xilinx.com/training/atp.htm#EU) or send your inquiries to [eurotraining@xilinx.com](mailto:eurotraining@xilinx.com).

**Asia Pacific**, contact your training provider at [www.xilinx.com/training/atp.htm#AP](http://www.xilinx.com/training/atp.htm#AP), or send your inquiries to [education\\_ap@xilinx.com](mailto:education_ap@xilinx.com), or call +852-2424-5200.

**Japan**, contact your training provider at [www.xilinx.com/training/atp.htm#JP](http://www.xilinx.com/training/atp.htm#JP), or send your inquiries to [education\\_kk@xilinx.com](mailto:education_kk@xilinx.com), or call +81-3-6744-7970