Xilinx Partial Reconfiguration Tools and Techniques

FPGA 4

FPGA-PR-ILT (v1.0)

Course Specification

Course Description

This course demonstrates how to use the Vivado® Design Suite to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow. This course also demonstrates how to use thee PR controller and PR decoupler IP in the PR process. You will also gain an understanding of PR implementation in an embedded system environment.

This course covers both the tool flow and mechanics of successfully creating a PR design. This course also covers both UltraScale™ and 7 series architecture design requirements, recommendations, and expectations for PR systems. In addition, it describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications. You will also identify techniques to debug PR designs.

Level – FPGA 4

Course Duration – 2 days

Course Part Number – FPGA-PR-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need of partial reconfiguration techniques

Prerequisites

- *Essentials of FPGA Design* course
- *Vivado Design Suite Static Timing Analysis and Xilinx Design Constraints* course
- *Advanced Tools and Techniques of the Vivado Design Suite* course
- Working HDL knowledge (VHDL or Verilog)

Software Tools

- Vivado Design or System Edition 2016.1 with PR license

Hardware

- Architecture: UltraScale and 7 series FPGAs*
- Demo board: Kintex® UltraScale FPGA KCU105 board, Kintex-7 FPGA KC705 board, and ZedBoard**

* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

** The UltraScale architecture versions of the "Using the PRC IP in a Partial Reconfiguration Design" lab and the "Using ILA Cores to Debug Partial Reconfiguration Designs" lab are not available because of QSPI and PRC issues on the KCU105 board. These two labs support only the 7 series architecture. The "Partial Reconfiguration in Embedded Systems" lab requires a ZedBoard for implementation.

After completing this comprehensive training, you will have the necessary skills to:

- Build and assemble a Partially Reconfigurable system (UltraScale, 7 series, and Zynq® devices)
- Define PR regions and reconfigurable modules with the Vivado Design Suite
- Generate the appropriate full and partial bitstreams for a PR design
- Use the ICAP and PCAP components to deliver the partially reconfigurable systems
- Identify how Partial Reconfiguration affects various silicon resources, including block RAM, IOBs, fabric, clock buffers, and MGTs
- Implement a Partial Reconfiguration system using the following techniques:
  - Direct JTAG connection
  - Floorplanning
  - Timing constraints and analysis
- Implement a PR system using the PRC IP
- Implement a PR system in an embedded environment
- Debug PR designs

Course Outline

Day 1

- Partial Reconfiguration Methodology
- **Demo:** Introduction to Partial Reconfiguration
- Partial Reconfiguration Tool Flow
- **Lab 1:** Partial Reconfiguration Flow
- **Lab 2:** Floorplanning the PR Design
- Optional: FPGA Configuration Overview
- Partial Reconfiguration Bitstreams
- **Demo:** Partial Reconfiguration Controller (PRC) IP
- **Lab 3:** Using the Partial Reconfiguration Controller in a PR Design

Day 2

- Managing Clocks, I/Os, and GTs
- Partial Reconfiguration: Managing Timing
- **Lab 4:** Partial Reconfiguration Timing Analysis and Constraints
- Partial Reconfiguration in Embedded Systems
- **Lab 5:** Partial Reconfiguration in Embedded Systems
- Debugging Partial Reconfiguration Designs
- **Lab 6:** Debugging a Partial Reconfiguration Design
- Partial Reconfiguration Design Recommendations
- PCIe Core and Partial Reconfiguration

Lab Descriptions

- **Lab 1:** Partial Reconfiguration Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- **Lab 2:** Floorplanning the PR Design – Illustrates how to create efficient Pblocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.
- **Lab 3**: Using the Partial Reconfiguration Controller in a PR Design – Illustrates using the PRC IP and hardware triggers to manage partial bitstreams.
- **Lab 4:** Partial Reconfiguration Timing Analysis and Constraints – Shows how area groups and Reconfigurable Partitions affect design performance.
- **Lab 5**: Partial Reconfiguration in Embedded Systems – Illustrates implementing PR designs in an embedded environment.
- **Lab 6**: Debugging a Partial Reconfiguration Design – Demonstrates using ILA cores to debug PR designs and shows which signals to monitor during debugging.

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