

## Course Description

This course describes the FPGA design best practices and skills to be successful using the Vivado® Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

#### Level – FPGA 3

**Course Duration** – 2 days

**Course Part Number** – FPGA-VDM-ILT

**Who Should Attend?** – Engineers who seek training for FPGA design best practices that increase design performance and increase development productivity.

#### Prerequisites

- Some knowledge of FPGA design techniques is helpful
- Experience with the Vivado Design Suite or attendance of one of our existing Vivado Design Suite training courses is required
- Intermediate knowledge of Verilog or VHDL

#### Software Tools

- Vivado Design or System Edition 2017.1

#### Hardware

- Architecture: UltraScale™ and 7 series FPGAs\*
- Demo board: None\*

\* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the UltraFast™ design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experience

## Course Outline

### Day 1

- UltraFast Design Methodology: Planning {Lecture, Demo}
- UltraFast Design Methodology: Design Creation and Analysis {Lecture}
- HDL Coding Techniques {Lecture}
- Resets {Lecture, Lab}
- Register Duplication {Lecture}
- Synchronous Design Techniques {Lecture}
- Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Vivado Design Rule Checks {Lab}
- Creating and Packaging Custom IP {Lecture, Lab}

### Day 2

- UltraFast Design Methodology: Design Closure {Lecture}
- UltraFast Design Methodology: Advanced Techniques {Lecture}
- Baselining {Lecture, Lab, Demo}
- Pipelining {Lecture, Lab}
- Inference {Lecture, Lab}
- Revision Control Systems in the Vivado Design Suite {Lecture, Lab}
- Synchronization Circuits {Lecture, Lab, Case Study}
- Introduction to Floorplanning {Lecture}
- Physical Optimization {Lecture, Lab}
- Power Management Techniques {Lecture}
- Vivado Design Suite Debug Methodology {Lecture}

## Topic Descriptions

### Day 1

- UltraFast Design Methodology: Planning – Introduces the methodology guidelines on planning and the UltraFast Design Methodology checklist.
- UltraFast Design Methodology: Design Creation and Analysis – Overview of the methodology guidelines on design creation and analysis.
- HDL Coding Techniques – Covers basic digital coding guidelines used in an FPGA design.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Synchronous Design Techniques – Introduces synchronous design techniques used in an FPGA design.
- Vivado Design Suite I/O Pin Planning – Use the I/O Pin Planning layout to perform pin assignments in a design.
- Vivado Design Rule Checks – Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations.
- Creating and Packaging Custom IP – Create your own IP and package and include it in the Vivado IP catalog.

### Day 2

- UltraFast Design Methodology: Design Closure – Introduces the UltraFast™ methodology guidelines on design closure.
- UltraFast Design Methodology: Advanced Techniques – Introduces the methodology guidelines for advanced techniques.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Pipelining – Use pipelining to improve design performance.
- Inference – Infer Xilinx dedicated hardware resources by writing appropriate HDL code.
- Revision Control Systems in the Vivado Design Suite – Use version control systems with Vivado design flows.
- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Physical Optimization – Use physical optimization techniques for timing closure.
- Power Management Techniques – Identify techniques used for low power design.
- Vivado Design Suite Debug Methodology – Understand and follow the debug core recommendations. Employ the debug methodology for debugging a design using the Vivado logic analyzer.

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