Essentials of FPGA Design

FPGA 2

FPGA-VESS-ILT (v1.0)

Course Specification

Course Description

Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set basic XDC timing constraints, and use the Vivado® Design Suite to build, synthesize, implement, and download a design.

Level – FPGA 2

Course Duration – 2 days

Course Part Number – FPGA-VESS-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Optional Videos

- Basic HDL Coding Techniques*
- Virtex-6 and Spartan-6 FPGA HDL Coding Techniques*

Software Tools

- Vivado Design or System Edition 2015.3

Hardware

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board (optional): Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 evaluation board**

* Go to www.xilinx.com/training and click the FPGA Design link under Online Training to view these videos.

** This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the Xilinx UltraScale FPGA resources
- Use the Project Manager to start a new project
- Identify the available Vivado IDE design flows (project based and non-project batch)
- Identify file sets (HDL, XDC, simulation)
- Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize and implement an HDL design
- Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
- Build custom IP with the IP Library utility
- Make basic timing constraints (create_clock, set_input_delay, and set_output_delay)
- Use the primary Tcl-based reports (check_timing, report_clock_interaction, report_clock_networks, and report_timing_summary)
- Describe and analyze common STA reports
- Identify synchronous design techniques
- Describe how an FPGA is configured

Course Outline

Day 1

- UltraFast Design Methodology Summary
- CLB Resources
- Introduction to the Vivado Design Suite
- Vivado Design Flows
- **Lab 1**: Vivado Tool Overview
- Demo: Visualization for Design Analysis
- Designing with IP
- Demo: IP Flow
- Demo: Designing with IPI
- Basic Timing Constraints and STA
- Demo: Reading Synthesis and Implementation Reports
- **Lab 2:** Vivado Synthesis, Implementation, and Timing Closure

Day 2

- I/0 Resources
- Other FPGA Resources
- Clocking Resources
- **Lab 3:** Designing with FPGA Resources
- Timing Reports
- **Lab 4:** Basic XDC and Timing Reports
- Synchronous Design Techniques
- FPGA Configuration
- UltraScale+ Families Overview
- Course Summary
- Appendix: Visualization for Analysis
- Appendix: Designing with IP
- Appendix: Designing with IP – IP Integrator Flow Lab

Lab Descriptions

- **Lab 1**: Vivado Tool Overview – Create a project in the Vivado Design Suite. Add files, simulate, and elaborate the design. Review the available reports, analyze the design with the Schematic and Hierarchy viewers, and run a design rule check (DRC). Finally, assign some of the I/O pins using the IO Planner.
- **Lab 2**: Vivado Synthesis, Implementation, and Timing Closure – Synthesize and analyze the design with the Schematic viewer, apply a systematic approach to applying timing constraints and timing closure (i.e., understand the Xilinx baselining recommendation). Run basic static timing analysis using the `check_timing` and `report_clock_utilization` reports. Implement the design and analyze some timing-critical paths with the Schematic viewer. Download the bitstream to the demonstration board.
- **Lab 3:** Designing with FPGA Resources – Use the Xilinx Clocking Wizard to configure a clocking subsystem to provide various clock outputs and clock buffers to connect clock signals to global clock networks.
- **Lab 4:** Basic XDC and Timing Reports – Use timing constraints to improve design performance. Perform static timing analysis before and after implementation to validate the performance results.

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