Debugging Techniques Using the Vivado Logic Analyzer

FPGA 2

FPGA-VLA-ILT (v1.0)

Course Specification

Course Description

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use Vivado® logic analyzer debug solution helps minimize the amount of time required for verification and debug.

This one-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the Vivado debug tool can address advanced verification and debugging challenges.

Level – FPGA 2

Course Duration – 1 day

Course Part Number – FPGA-VLA-ILT

Who Should Attend? – System and logic designers who want to minimize verification and debug time

Prerequisites

- Basic language concepts
  - *Designing with VHDL* or equivalent knowledge of VHDL
  - *Designing with Verilog* or equivalent knowledge of Verilog
- Basic FPGA skills
  - *Essentials of FPGA Design*
- Intermediate FPGA skills
  - *Vivado Static Timing Analysis and Xilinx Design Constraints*
- Programming and Debug videos recommended

Software Tools

- Vivado Design or System Edition 2015.3

Hardware

- Architecture: N/A*
- Demo boards: Kintex®-7 FPGA KC705 board

* This course does not focus on any particular architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify each Vivado IDE debug core and explain its purpose
- Effectively utilize the Vivado logic analyzer
- Implement the Vivado IDE debug cores using both the netlist insertion and HDL instantiation tool flows
- Select effective test points in your design
- Optimize design and core performance when debug cores are used
- Execute various techniques for collecting data including
  - File storage
  - Scripting
  - Building custom triggers

Course Outline

- Introduction to Vivado Logic Analyzer
- Demo: JTAG-to-AXI Master Debug IP Transactions
- Adding the Debug Cores – Netlist Insertion Flow
- **Lab 1:** Inserting a Debug Core Using the Netlist Insertion Flow
- Instantiating the Debug Cores – HDL Instantiation Flow
- **Lab 2:** Adding a Debug Core Using the HDL Instantiation Flow
- Debug Flow in IP Integrator
- **Lab 3:** Debugging Flow – IPI Block Design
- Triggering and Visualizing Data
- Demo: Using Dashboards in the Vivado Logic Analyzer
- Demo: Trigger on Startup
- Tips and Tricks
- **Lab 4:** Tips and Tricks
- Scripting
- **Lab 5:** VIO Tcl Scripting
- Remote Access
- **Lab 6:** Remote Access (Optional)*

* Check with your Authorized Training Provider to confirm whether this content is included with your specific class.

Lab Descriptions

- **Labs 1:** Inserting a Debug Core Using the Netlist Insertion flow – Insert ILA cores into an existing synthesized netlist and debug a common problem.
- **Lab 2:** Adding a Debug Core Using the HDL Instantiation flow – Build upon a provided design to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- **Lab 3:** Debugging Flow – IPI Block Design – Add an ILA IP core to a provided block design and connect nets to the core. Observe its behavior using the Vivado logic analyzer.
- **Lab 4:** Tips and Tricks – Sample across multiple time domains and use advanced trigger and capture capabilities.
- **Lab 5:** VIO Tcl Scripting - Configure automated analysis.
- **Lab 6:** Remote Access – Use the Vivado logic analyzer to configure an FPGA, set up triggering, and view the sampled data from a remote location.

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