Designing with Verilog

FPGA 1

LANG-VERILOG-ILT (v1.0)

Course Specification

Course Description

This comprehensive course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization. This course covers Verilog 1995 and 2001.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Level – FPGA 1

Course Duration – 3 days

Course Part Number – LANG-VERILOG-ILT

Who Should Attend? – Engineers who want to use Verilog effectively for modeling, design, and synthesis of digital designs

Prerequisites

- Basic digital design knowledge

Software Tools

- Vivado® Design or System Edition 2017.1

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Run a timing simulation by using Xilinx Simprim libraries
- Create and manage designs within the Vivado Design Suite environment
- Download to the evaluation demo board

Course Outline

Day 1

- Introduction to Verilog {Lecture}
- Verilog Keywords and Identifiers {Lecture}
- Verilog Data Values and Number Representation {Lecture}
- Verilog Data Types {Lecture}
- Verilog Buses and Arrays {Lecture}
- Verilog Modules and Ports {Lecture, Lab, Demo}
- Verilog Operators {Lecture}
- Continuous Assignment {Lecture}
- Gate-Level Modeling {Lecture}
- Procedural Assignment {Lecture}
- Blocking and Non-Blocking Procedural Assignment {Lecture, Lab}
- Procedural Timing Control {Lecture}

Day 2

- Verilog Conditional Statements: if_else {Lecture, Lab}
- Verilog Conditional Statements: case {Lecture}
- Verilog Loop Statements {Lecture}
- Introduction to Verilog Testbenches {Lecture, Lab}
- System Tasks {Lecture}
- Verilog Sub-Programs {Lecture}
- Verilog Functions {Lecture}
- Verilog Tasks {Lecture}
- Verilog Compiler Directives {Lecture}
- Verilog Parameters {Lecture, Lab}
- Verilog Generate Statement {Lecture}

Day 3

- Verilog Timing Checks {Lecture}
- Finite State Machines {Lecture}
- Mealy Finite State Machine {Lecture, Lab}
- Moore Finite State Machine {Lecture, Lab}
- FSM Coding Guidelines {Lecture}
- File I/O: Introduction {Lecture}
- File I/O: Read Functions {Lecture, Lab}
- File I/O: Write Functions {Lecture}
- Targeting Xilinx FPGAs {Lecture, Lab}
- User-Defined Primitives {Lecture}
- Programming Language Interface {Lecture}

Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

Register Today

Xilinx's network of Authorized Training Providers (ATP) delivers public and private courses in locations throughout the world. Please contact your closest ATP for more information, to view schedules, or to register online.

Visit **www.xilinx.com/training** and click on the region where you want to attend a course.

Americas, contact your training provider at www.xilinx.com/training/atp.htm#NA or send your inquiries to registrar@xilinx.com.

Europe, contact your training provider at www.xilinx.com/training/atp.htm#EU or send your inquiries to eurotraining@xilinx.com.

Asia Pacific, contact your training provider at www.xilinx.com/training/atp.htm#AP, or send your inquiries to education_ap@xilinx.com, or call +852-2424-5200.

Japan, contact your training provider at www.xilinx.com/training/atp.htm#JP, or send your inquiries to education_kk@xilinx.com, or call +81-3-6744-7970.