Designing with VHDL

FPGA 1

Course Specification

- Documentation in VHDL
- Data Types
- Concurrent Operations
- Lab 2: Using Concurrent Statements
- Processes and Variables
- Lab 3: Designing a Simple Process

Day 2

- Introduction to Testbenches
- ISim Simulation Tool Basics
- Lab 4: Simulating a Simple Design
- Creating Memory
- Lab 5: Building a Dual-Port Memory
- Finite State Machines
- Lab 6: Building a Moore Finite State Machine
- Targeting Xilinx FPGAs
- Lab 7: Xilinx Tool Flow

Day 3

- Loops and Conditional Elaboration
- Lab 8: Using Loops
- Attributes
- Functions and Procedures
- Packages and Libraries
- Lab 9: Building Your Own Package
- Interacting with the Simulation
- Writing a Good Testbench
- Lab 10: Building a Meaningful Testbench

Lab Descriptions

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. You will write, synthesize, simulate, and implement all the labs. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits.

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Course Outline

Day 1

- The "Shape" of VHDL
- Demo: Multiplexer
- Lab 1: Using the Tools

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