Class Schedule by Location

Important Notice:

1. Class Schedule list below is as of Jan 15, 2018.
2. Class dates are subject to change due to low enrollment. Please contact your local training representative if you have any questions.
3. Confirm any timezone differences with the ATP when you register.

If you have any questions, please contact the Registrar at registrar@xilinx.com.

AUSTRIA

Date	Location	Facility	Price	TC	Reg. URL
2018-02-08	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-03-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-05-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-07-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-08-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-10-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-11-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with Multi-Gigabit Serial I/O					
2018-02-05	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Multi-Gigabit Serial I/O					
2018-03-26	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Multi-Gigabit Serial I/O					
2018-07-02	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Multi-Gigabit Serial I/O					
2018-08-20	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Multi-Gigabit Serial I/O					
2018-10-08	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	28	Register
Designing with Multi-Gigabit Serial I/O					
2018-11-26	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-02-06	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-03-27	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-05-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-05-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-07-03	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-08-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-10-09	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with UltraScale FPGA Transceivers					
2018-11-27	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-02-08	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-03-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-05-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-07-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-08-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-10-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Connectivity Memory Interfaces					
2018-11-29	Lustkandlg. 52 Vienna	So-logic	0.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-02-08	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					

2018-03-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-05-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-07-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-08-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-10-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing a LogiCORE PCI Express System					
2018-11-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-02-05	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-03-26	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-05-14	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-07-02	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-08-20	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-10-08	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-11-26	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
C-based HLS Coding for Hardware Designers					
2018-02-23	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-04-06	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-06-01	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-07-20	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-09-07	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-10-25	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Hardware Designers					
2018-12-14	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-02-23	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-04-06	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-06-01	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-07-20	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	18	Register
C-based HLS Coding for Software Designers					
2018-09-07	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-10-25	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
C-based HLS Coding for Software Designers					
2018-12-14	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-02-19	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-04-03	Lustkandlg. 52 Vienna	So-logic	0.00 (EUR)	18	Register

Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-05-28	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-07-16	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-09-03	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-10-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-12-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-04-04	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-05-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-07-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-09-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-10-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-12-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-02-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-04-04	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-05-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-07-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-09-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-10-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-12-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-02-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-03-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-05-03	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-06-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-08-09	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-11-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-01-31	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-03-14	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-05-02	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register

Advanced Features and Techniques of Embedded Systems Software Design					
2018-06-20	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-08-08	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-09-26	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-11-14	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
2018-02-01	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	18	Register
2018-03-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-05-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-06-28	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-08-16	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-10-04	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-11-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-01-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-03-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-05-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-06-19	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-08-07	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-09-25	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Design					
2018-11-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Open-Source Linux Development					
2018-01-29	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-03-19	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-05-07	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-06-25	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-08-13	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-10-01	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Open-Source Linux Development					
2018-11-19	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Embedded Systems Software Development					
2018-01-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Software Development					
2018-03-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Software Development					
2018-04-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Software Development					
2018-06-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Software Development					
2018-08-06	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Embedded Systems Software Development					
2018-09-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register

Embedded Systems Software Development					
2018-11-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-01-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-03-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-04-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-06-07	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-07-26	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-09-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-11-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-02-02	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-03-23	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-06-29	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-08-17	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-10-05	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-11-11	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-11-23	Lustkandlg. 52 Vienna	So-logic	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-01-31	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-03-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-05-09	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-06-28	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-08-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-10-03	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-11-21	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-01-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-03-19	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-05-07	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-06-25	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-08-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-10-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Software Developer					

2018-11-19	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-01-16	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-02-27	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-04-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-06-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-07-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-09-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-10-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-01-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-03-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-04-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-06-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-07-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-09-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-11-05	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-01-16	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-02-27	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-04-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-06-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-07-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-09-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-10-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-01-24	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-03-07	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-04-25	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-06-13	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-08-01	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-09-19	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					

2018-11-07	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-02-26	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-04-09	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-06-04	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-07-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-09-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-10-29	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	27	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-01-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-28	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-04-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-06-06	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-07-25	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-09-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-10-31	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-03-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-04-23	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-06-11	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-07-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-09-17	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-11-05	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-01-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-03-07	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-04-25	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-06-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-08-01	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-09-19	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-11-07	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced VHDL					
2018-02-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register

Advanced VHDL					
2018-05-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced VHDL					
2018-07-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced VHDL					
2018-08-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced VHDL					
2018-10-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Advanced VHDL					
2018-12-06	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
2018-09-18	Lustkandlg. 52 Vienna	So-logic	0.00 (EUR)	27	Register
2018-09-18	Lustkandlg. 52 Vienna	So-logic	0.00 (EUR)	27	Register
Designing with System Verilog					
2018-02-13	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with System Verilog					
2018-05-22	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with System Verilog					
2018-07-10	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with System Verilog					
2018-08-28	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with System Verilog					
2018-10-16	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with System Verilog					
2018-12-04	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-02-15	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-05-24	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-07-12	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-08-30	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-10-18	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Verification with System Verilog					
2018-12-06	Lustkandlg. 52 Vienna	So-logic	1,500.00 (EUR)	18	Register
Designing with Verilog					
2018-02-12	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-02-12	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-05-21	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-05-21	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-07-09	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-07-09	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-08-27	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-08-27	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-10-15	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-10-15	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register

Designing with Verilog					
2018-12-03	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register
Designing with Verilog					
2018-12-03	Lustkandlg. 52 Vienna	So-logic	2,250.00 (EUR)	27	Register

AZ

Date	Location	Facility	Price	TC	Reg. URL
Designing FPGAs Using the Vivado Design Suite 3					
2018-02-12	1031 East Apache Blvd Tempe	Holiday Inn Express	1,400.00 (USD)	14	Register

CA - LOS ANGELES

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-14	5665 Hollister Ave Goleta	Hampton Inn	1,400.00 (USD)	14	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-19	2100 E Mariposa Ave El Segundo	Hilton Garden Inn, LAX	1,400.00 (USD)	14	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-02-28	2100 E Mariposa Ave El Segundo	Hilton Garden Inn, LAX	700.00 (USD)	7	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-01-30	2100 E Mariposa Ave El Segundo	Hilton Garden Inn, LAX	1,400.00 (USD)	14	Register

CA - ORANGE COUNTY

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-16	220 Commerce, Suite 100 Irvine	Avnet	1,400.00 (USD)	14	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-19	220 Commerce, Suite 100 Irvine	Avnet	1,400.00 (USD)	14	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-01-18	220 Commerce, Suite 100 Irvine	Avnet	700.00 (USD)	7	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-21	220 Commerce, Suite 100 Irvine	Avnet	700.00 (USD)	7	Register

CA - SAN DIEGO

Date	Location	Facility	Price	TC	Reg. URL
Designing FPGAs Using the Vivado Design Suite 1					
2018-03-12	10815 Rancho Bernardo Dr. San Diego	Xilinx	1,400.00 (USD)	14	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-05	10815 Rancho Bernardo Dr. San Diego	Xilinx	1,400.00 (USD)	14	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-22	10815 Rancho Bernardo Dr. San Diego	Xilinx	1,400.00 (USD)	14	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-03-14	10815 Rancho Bernardo Dr. San Diego	Xilinx	1,400.00 (USD)	14	Register

CHINA

Date	Location	Facility	Price	TC	Reg. URL
Designing with Ethernet MAC Controllers					
2018-01-22	Shanghai Shanghai	E-elements	400.00 (USD)	4	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-25	Shanghai Shanghai	E-elements	400.00 (USD)	4	Register
High-Level Synthesis for Software Engineers					
2018-01-24	Beijing Beijing	E-elements	200.00 (USD)	2	Register
DSP Design Using System Generator					
2018-01-18	Shenzhen Shenzhen	E-elements	400.00 (USD)	4	Register
DSP Implementation Techniques for Xilinx FPGAs					
2018-01-29	Shenzhen Shenzhen	E-elements	200.00 (USD)	2	Register
Embedded Systems Design					
2018-01-22	Beijing Beijing	E-elements	400.00 (USD)	4	Register
Introduction to Zynq EPP Architecture					
2018-01-31	Shanghai Shanghai	E-elements	100.00 (USD)	1	Register
Embedded Design with PetaLinux Tools					
2018-01-29	Shanghai Shanghai	E-elements	400.00 (USD)	4	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-01-24	Shenzhen Shenzhen	E-elements	200.00 (USD)	2	Register
Zynq-7000 All Programmable SoC					
2018-01-18	Beijing Beijing	E-elements	400.00 (USD)	4	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-01-17	Webex Webex	E-elements	200.00 (USD)	2	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-01-31	Beijing Beijing	E-elements	200.00 (USD)	2	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-01-18	Shanghai Shanghai	E-elements	400.00 (USD)	4	Register
Vivado Design Suite Tool Flow					
2018-01-17	Shenzhen Shenzhen	E-elements	100.00 (USD)	1	Register
Vivado Design Suite Tool Flow					
2018-01-24	Webex Webex	E-elements	0.00 (USD)	0	Register
Designing with VHDL					
2018-01-25	Beijing Beijing	E-elements	300.00 (USD)	3	Register

CO

Date	Location	Facility	Price	TC	Reg. URL
Embedded Systems Design					
2018-02-21	1951 S. Fordham Longmont	Xilinx Learning Center	1,400.00 (USD)	14	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-03-21	1951 S. Fordham Longmont	Xilinx Learning Center	1,400.00 (USD)	14	Register

FL

Date	Location	Facility	Price	TC	Reg. URL
Designing with UltraScale FPGA Transceivers					
2018-02-01	Florida Florida	Florida	1,600.00 (USD)	16	Register
Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology					
2018-01-29	Florida Florida	Florida	2,400.00 (USD)	24	Register
Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology					
2018-03-20	Florida Florida	Florida	2,400.00 (USD)	24	Register
Zynq-7000 All Programmable SoC					
2018-01-18	Florida Florida	Florida	1,600.00 (USD)	16	Register
Vivado Design Suite for ISE Project Navigator Users					
2018-01-25	Florida Florida	Florida	1,600.00 (USD)	16	Register

IL - CHICAGO

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-29	600 N Martingale Rd Schaumburg, IL 60173 Schaumburg	Quality Inn Schaumburg	1,600.00 (USD)	16	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-14	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-04-24	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
DSP Design Using System Generator					
2018-04-05	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
Xilinx HLS and SDSoC					
2018-01-29	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	2,400.00 (USD)	24	Register
Xilinx HLS and SDSoC					
2018-04-24	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	2,400.00 (USD)	24	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-01-31	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	800.00 (USD)	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-04-26	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	800.00 (USD)	8	Register
Essential Microprocessor Systems					
2018-01-24	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	800.00 (USD)	8	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-03-06	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-04-02	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
Designing with 7 Series					
2018-04-05	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,400.00 (USD)	14	Register
Partial Reconfiguration					
2018-02-22	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,800.00 (USD)	18	Register
Designing with the UltraScale Architecture					
2018-03-08	TBD Champaign	TBD	1,400.00 (USD)	14	Register
Designing with the UltraScale Architecture					
2018-04-04	475 Martingale Road, Schaumburg, IL 60173 Schaumburg	Xilinx - Suite 750, 7th Floor Conference Room	1,400.00 (USD)	14	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-04-16	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-01-25	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Schaumburg	Xilinx Suite 280	1,600.00 (USD)	16	Register

INDIA

Date	Location	Facility	Price	TC	Reg. URL
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-03-07	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
High-Level Synthesis for Hardware Engineers					
2018-03-15	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
High-Level Synthesis for Software Engineers					
2018-01-22	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-03-27	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
C Language Programming with Xilinx SDK					
2018-03-12	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Embedded Systems Design					
2018-02-07	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Embedded Design with PetaLinux Tools					
2018-03-05	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Zynq-7000 All Programmable SoC					
2018-01-24	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Partial Reconfiguration					
2018-01-31	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	300.00 (USD)	3	Register
Designing with the UltraScale Architecture					
2018-02-21	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-02-12	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-14	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-16	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-02-16	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-01-18	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-02-19	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
UltraFast Design Methodology					
2018-01-29	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Advanced VHDL					
2018-02-05	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Verification with System Verilog					
2018-03-22	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register

INDIA

Date	Location	Facility	Price	TC	Reg. URL
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-03-07	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
High-Level Synthesis for Hardware Engineers					
2018-03-15	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
High-Level Synthesis for Software Engineers					
2018-01-22	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-03-27	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
C Language Programming with Xilinx SDK					
2018-03-12	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Embedded Systems Design					
2018-02-07	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Embedded Design with PetaLinux Tools					
2018-03-05	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Zynq-7000 All Programmable SoC					
2018-01-24	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Partial Reconfiguration					
2018-01-31	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	300.00 (USD)	3	Register
Designing with the UltraScale Architecture					
2018-02-21	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-02-12	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-14	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-16	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-02-16	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-01-18	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-02-19	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
UltraFast Design Methodology					
2018-01-29	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Advanced VHDL					
2018-02-05	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	600.00 (USD)	6	Register
Verification with System Verilog					
2018-03-22	#21, 7th Main ,1st Block Koramangala Bangalore	Sandeepani School of Embedded System Design	400.00 (USD)	4	Register

JAPAN

Date	Location	Facility	Price	TC	Reg. URL
Designing a LogiCORE PCI Express System					
2018-02-20	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
C for beginner with Vivado HLS tool					
2018-03-14	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-16	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-22	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
DSP Design Using System Generator					
2018-01-23	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	8	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-03-27	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-03-29	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
MicroBlaze for beginner with ARTY Board					
2018-03-29	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Embedded Systems Design					
2018-02-08	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-02-01	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-15	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded Systems Software Design					
2018-03-08	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Zynq-7000 All Programmable SoC					
2018-01-25	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Understand simulation with Vivado Design Suite					
2018-01-16	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Debugging Techniques Using the Vivado Logic Analyzer					
2018-01-18	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
RTL(VHDL) Design with Vivado Design Suite					
2018-01-18	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
RTL(Verilog) Design with Vivado Design Suite					
2018-01-25	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
Vivado Design Suite Tool Flow					
2018-01-30	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
Vivado Design Suite Static Constraints and Timing Analysis					
2018-02-05	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Vivado Design Suite Static Timing Closure					
2018-02-13	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Essentials of FPGA Design					
2018-02-15	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Vivado Design Suite Tool Flow					
2018-02-28	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
Essentials of FPGA Design					
2018-03-06	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
RTL(Verilog) Design with Vivado Design Suite					
2018-03-06	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
Vivado Design Suite Tool Flow with Artix-7 Board					
2018-03-13	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Debugging Techniques Using the Vivado Logic Analyzer					
2018-03-22	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Partial Reconfiguration					
2018-02-14	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register

UltraFast Design Methodology

2018-02-27 Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama hdLab, Inc. 98,000.00 () 10 Register

JAPAN

Date	Location	Facility	Price	TC	Reg. URL
Designing a LogiCORE PCI Express System					
2018-02-20	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
C for beginner with Vivado HLS tool					
2018-03-14	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-16	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-22	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
DSP Design Using System Generator					
2018-01-23	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	8	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-03-27	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-03-29	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
MicroBlaze for beginner with ARTY Board					
2018-03-29	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Embedded Systems Design					
2018-02-08	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-02-01	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-15	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Embedded Systems Software Design					
2018-03-08	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Zynq-7000 All Programmable SoC					
2018-01-25	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Understand simulation with Vivado Design Suite					
2018-01-16	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Debugging Techniques Using the Vivado Logic Analyzer					
2018-01-18	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
RTL(VHDL) Design with Vivado Design Suite					
2018-01-18	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
RTL(Verilog) Design with Vivado Design Suite					
2018-01-25	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
Vivado Design Suite Tool Flow					
2018-01-30	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
Vivado Design Suite Static Constraints and Timing Analysis					
2018-02-05	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Vivado Design Suite Static Timing Closure					
2018-02-13	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Essentials of FPGA Design					
2018-02-15	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Vivado Design Suite Tool Flow					
2018-02-28	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register
Essentials of FPGA Design					
2018-03-06	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
RTL(Verilog) Design with Vivado Design Suite					
2018-03-06	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register
Vivado Design Suite Tool Flow with Artix-7 Board					
2018-03-13	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	49,000.00 ()	4	Register
Debugging Techniques Using the Vivado Logic Analyzer					
2018-03-22	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	98,000.00 ()	8	Register
Partial Reconfiguration					
2018-02-14	Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo	Xilinx K.K.	49,000.00 ()	4	Register

UltraFast Design Methodology					
2018-02-27	Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama	hdLab, Inc.	98,000.00 ()	10	Register

KOREA S

Date	Location	Facility	Price	TC	Reg. URL
Designing a LogiCORE PCI Express System					
2018-02-22	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-22	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
DSP Design Using System Generator					
2018-02-20	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Embedded Systems Design					
2018-02-08	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Embedded Design with PetaLinux Tools					
2018-01-27	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	855.00 (USD)	9	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-12	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Designing with VHDL					
2018-02-05	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	600.00 (USD)	6	Register

KOREA S

Date	Location	Facility	Price	TC	Reg. URL
Designing a LogiCORE PCI Express System					
2018-02-22	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-22	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
DSP Design Using System Generator					
2018-02-20	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Embedded Systems Design					
2018-02-08	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Embedded Design with PetaLinux Tools					
2018-01-27	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	855.00 (USD)	9	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-12	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	570.00 (USD)	6	Register
Designing with VHDL					
2018-02-05	#B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul	WEDU SOLUTION CO., LTD.	600.00 (USD)	6	Register

KS

Date	Location	Facility	Price	TC	Reg. URL
STA, XDC, and Advanced Tools and Techniques of Vivado Design Suite-custom					
2018-02-12	10556 Marty Avenue Overland Park, KS 66212 Overland Park	Homewood Suites by Hilton Kansas City/Overland Park	2,700.00 (USD)	27	Register

MA

Date	Location	Facility	Price	TC	Reg. URL
Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology					
2018-01-17	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	2,400.00 (USD)	24	Register
Embedded Design with PetaLinux Tools					
2018-03-20	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	1,600.00 (USD)	16	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-01-24	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	800.00 (USD)	8	Register
Embedded Systems Software Design					
2018-03-20	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	1,600.00 (USD)	16	Register
Zynq-7000 All Programmable SoC					
2018-02-14	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	1,600.00 (USD)	16	Register
Debugging Techniques Using the Vivado Logic Analyzer					
2018-01-16	217 Middlesex Turnpike, Suite 205 Burlington	Genesis	8,000.00 (USD)	8	Register

MD

Date	Location	Facility	Price	TC	Reg. URL
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-03-21	Columbia	Bottom Line Technologies Training Center - Columbia,MD	2,000.00 (USD)	20	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-05	Columbia	Bottom Line Technologies Training Center - Columbia,MD	1,800.00 (USD)	18	Register
Vivado Boot Camp Phase-1					
2018-02-06	Columbia	Bottom Line Technologies Training Center - Columbia,MD	2,700.00 (USD)	27	Register
Vivado Boot Camp Phase-2					
2018-02-27	Columbia	Bottom Line Technologies Training Center - Columbia,MD	2,700.00 (USD)	27	Register

MN

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
DSP Design Using System Generator					
2018-02-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Zynq SoC Master Training for Experienced FPGA Designers					
2018-02-05	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	2,700.00 (USD)	27	Register
Xilinx HLS and SDSoC					
2018-02-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	2,400.00 (USD)	24	Register
Xilinx HLS and SDSoC					
2018-03-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	2,400.00 (USD)	24	Register
Embedded Design with PetaLinux Tools					
2018-02-14	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,800.00 (USD)	18	Register
Embedded Design with PetaLinux Tools					
2018-04-10	475 N Martingale Road, Suite 280, Schaumburg, IL 60173 Orono (Minneapolis)	Xilinx Suite 280	1,800.00 (USD)	18	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-02-21	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	800.00 (USD)	8	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-21	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	800.00 (USD)	8	Register
Embedded Systems Software Design					
2018-02-12	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-02-01	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Partial Reconfiguration					
2018-02-15	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,800.00 (USD)	18	Register
Partial Reconfiguration					
2018-02-21	2500 Shadywood Road Suite 505, Orono, MN 55331 Minneapolis	Freshwater Business Center	1,800.00 (USD)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-03-05	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-03-07	2500 Shadywood Road Suite 505, Orono, MN 55331 Minneapolis	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-04-12	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-22	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-03-12	2500 Shadywood Road Suite 505, Orono, MN 55331 Minneapolis	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 3					

2018-04-19	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-03-26	2500 Shadywood Road Suite 505, Orono, MN 55331 Orono (Minneapolis)	Freshwater Business Center	1,600.00 (USD)	16	Register

MO - ST LOUIS

Date	Location	Facility	Price	TC	Reg. URL
Embedded Design with PetaLinux Tools					
2018-03-13	TBD St Louis	TBD	1,800.00 (USD)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-02-05	TBD St Louis	TBD	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-08	TBD St Louis	TBD	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-02-12	TBD St Louis	TBD	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-02-19	TBD St Louis	TBD	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-02-15	TBD St Louis	TBD	1,600.00 (USD)	16	Register

NETHERLANDS

Date	Location	Facility	Price	TC	Reg. URL
Designing with Multi-Gigabit Serial I/O					
2018-03-07	Cereslaan 10b Heesch	Core|Vision	2,175.00 (EUR)	27	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-03-12	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-05-22	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-05	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-04-19	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-03-14	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
DSP Design Using System Generator					
2018-05-24	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-02-07	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-04-16	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-02-09	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-04-18	Cereslaan 10b Heesch	Core|Vision	750.00 (EUR)	9	Register
Embedded Systems Design					
2018-03-19	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-02-21	Cereslaan 10b Heesch	Core|Vision	750.00 (EUR)	9	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-05-02	Cereslaan 10b Heesch	Core|Vision	750.00 (EUR)	9	Register
Embedded Systems Software Design					
2018-03-21	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-02-19	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Zynq-7000 All Programmable SoC					
2018-04-30	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-05-17	Cereslaan 10b Heesch	Core|Vision	750.00 (EUR)	9	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-05-15	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-02-05	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing with 7 Series					
2018-04-23	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Doulos Essential Digital Design Techniques					
2018-03-12	Cereslaan 10b Heesch	Core|Vision	1,695.00 (EUR)	26	Register
Doulos Essential Digital Design Techniques					
2018-04-25	Cereslaan 10b Heesch	Core|Vision	1,695.00 (EUR)	26	Register
Partial Reconfiguration					
2018-01-22	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Partial Reconfiguration					
2018-04-03	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-02-05	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing with the UltraScale Architecture					
2018-04-23	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register

Vivado Design Suite for ISE Project Navigator Users					
2018-03-26	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-01-17	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users					
2018-03-28	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-03-26	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-01-17	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-03-28	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-01-22	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-04-03	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-01-24	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-04-05	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
UltraFast Design Methodology					
2018-01-24	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
UltraFast Design Methodology					
2018-04-05	Cereslaan 10b Heesch	Core|Vision	1,500.00 (EUR)	18	Register
Doulos VHDL for FPGA Design					
2018-01-29	Cereslaan 10b Heesch	Core|Vision	2,495.00 (EUR)	38	Register
Doulos Comprehensive VHDL					
2018-01-29	Cereslaan 10b Heesch	Core|Vision	3,595.00 (EUR)	54	Register
Doulos Advanced VHDL					
2018-02-01	Cereslaan 10b Heesch	Core|Vision	1,795.00 (EUR)	27	Register
Doulos Expert VHDL					
2018-02-26	Cereslaan 10b Heesch	Core|Vision	3,795.00 (EUR)	57	Register
Doulos Expert VHDL Design					
2018-02-26	Cereslaan 10b Heesch	Core|Vision	1,945.00 (EUR)	29	Register
Doulos Expert VHDL Verification					
2018-02-28	Cereslaan 10b Heesch	Core|Vision	2,595.00 (EUR)	39	Register
Doulos VHDL for FPGA Design					
2018-04-09	Cereslaan 10b Heesch	Core|Vision	2,495.00 (EUR)	38	Register
Doulos Comprehensive VHDL					
2018-04-09	Cereslaan 10b Heesch	Core|Vision	3,595.00 (EUR)	54	Register
Doulos Advanced VHDL					
2018-04-12	Cereslaan 10b Heesch	Core|Vision	1,795.00 (EUR)	27	Register
Doulos VHDL for FPGA Design					
2018-01-29	Cereslaan 10b Heesch	Core|Vision	2,495.00 (EUR)	38	Register
Doulos Comprehensive VHDL					
2018-01-29	Cereslaan 10b Heesch	Core|Vision	3,595.00 (EUR)	54	Register
Doulos Advanced VHDL					
2018-02-01	Cereslaan 10b Heesch	Core|Vision	1,795.00 (EUR)	27	Register
Doulos Expert VHDL					
2018-02-26	Cereslaan 10b Heesch	Core|Vision	3,795.00 (EUR)	57	Register
Doulos Expert VHDL Design					
2018-02-26	Cereslaan 10b Heesch	Core|Vision	1,945.00 (EUR)	29	Register
Doulos Expert VHDL Verification					
2018-02-28	Cereslaan 10b Heesch	Core|Vision	2,595.00 (EUR)	39	Register
Doulos VHDL for FPGA Design					
2018-04-09	Cereslaan 10b Heesch	Core|Vision	2,495.00 (EUR)	38	Register

Doulos Comprehensive VHDL					
2018-04-09	Cereslaan 10b Heesch	Core|Vision	3,595.00 (EUR)	54	Register
Doulos Advanced VHDL					
2018-04-12	Cereslaan 10b Heesch	Core|Vision	1,795.00 (EUR)	27	Register

NJ - NORTHERN

Date	Location	Facility	Price	TC	Reg. URL
Vivado Boot Camp Phase-1					
2018-01-29	3769 Route 46 East Parsippany	Courtyard Marriott - Parsippany,NJ	2,700.00 (USD)	27	Register
Vivado Boot Camp Phase-2					
2018-03-07	3769 Route 46 East Parsippany	Courtyard Marriott - Parsippany,NJ	2,700.00 (USD)	27	Register

NJ - SOUTHERN

Date	Location	Facility	Price	TC	Reg. URL
Vivado Boot Camp Phase-1					
2018-01-29	13000 Lincoln Drive West Marlton	Avnet Marlton - Marlton,NJ	2,700.00 (USD)	27	Register
Vivado Boot Camp Phase-2					
2018-03-07	13000 Lincoln Drive West Marlton	Avnet Marlton - Marlton,NJ	2,700.00 (USD)	27	Register

NM

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-01	2601 Yale Blvd SE Albuquerque,	Hilton Garden Inn	1,400.00 (USD)	14	Register

NY - NEW YORK METRO

Date	Location	Facility	Price	TC	Reg. URL
Vivado Boot Camp Phase-2					
2018-01-29	135 Engineers Rd Hauppauge	Avnet - Hauppauge,NY	2,700.00 (USD)	27	Register
Designing with VHDL					
2018-02-07	135 Engineers Rd Hauppauge	Avnet - Hauppauge,NY	2,700.00 (USD)	27	Register

NY - ROCHESTER

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-02-26	245 Kenneth Drive Rochester	Avnet - Rochester,NY	1,800.00 (USD)	18	Register
Vivado Boot Camp Phase-1					
2018-01-24	245 Kenneth Drive Rochester	Avnet - Rochester,NY	2,700.00 (USD)	27	Register
Vivado Boot Camp Phase-2					
2018-02-21	245 Kenneth Drive Rochester	Avnet - Rochester,NY	2,700.00 (USD)	27	Register
Vivado Boot Camp Phase-3					
2018-03-26	245 Kenneth Drive Rochester	Avnet - Rochester,NY	3,000.00 (USD)	30	Register

ONTARIO - OTTAWA

Date	Location	Facility	Price	TC	Reg. URL
2018-02-21	Ottawa Ottawa	Ottawa, ON	2,400.00 (USD)	24	Register
Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology					
2018-02-28	Ottawa Ottawa	Ottawa, ON	2,400.00 (USD)	24	Register
Embedded System Design for the Zynq UltraScale+ MPSoC					
2018-06-06	Ottawa Ottawa	Ottawa, ON	2,400.00 (USD)	24	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-01-17	Ottawa Ottawa	Ottawa, ON	800.00 (USD)	8	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-03-08	Ottawa Ottawa	Ottawa, ON	1,600.00 (USD)	16	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-04-03	Ottawa Ottawa	Ottawa, ON	1,600.00 (USD)	16	Register

ONTARIO - TORONTO

Date	Location	Facility	Price	TC	Reg. URL
Designing with UltraScale FPGA Transceivers					
2018-04-12	Toronto Toronto	Toronto, ON	1,600.00 (USD)	16	Register
Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology					
2018-01-17	Toronto Toronto	Toronto, ON	2,400.00 (USD)	24	Register
Embedded System Design for the Zynq UltraScale+ MPSoC					
2018-03-14	Toronto Toronto	Toronto, ON	2,400.00 (USD)	24	Register
Embedded System Design for the Zynq UltraScale+ MPSoC					
2018-05-09	Toronto Toronto	Toronto, ON	2,400.00 (USD)	24	Register
Designing with VHDL					
2018-03-13	Toronto Toronto	Toronto, ON	2,400.00 (USD)	24	Register

QUEBEC

Date	Location	Facility	Price	TC	Reg. URL
Embedded System Design for the Zynq UltraScale+ MPSoC					
2018-01-17	450 Saint Pierre, #300 Montreal	Hardent	2,400.00 (USD)	24	Register
Partial Reconfiguration					
2018-02-27	450 Saint Pierre, #300 Montreal	Hardent	1,600.00 (USD)	16	Register

RUSSIA

Date	Location	Facility	Price	TC	Reg. URL
Designing with Ethernet MAC Controllers					
2018-02-07	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with Ethernet MAC Controllers					
2018-04-25	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with Multi-Gigabit Serial I/O					
2018-03-26	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing with Multi-Gigabit Serial I/O					
2018-06-18	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing with UltraScale FPGA Transceivers					
2018-04-04	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with UltraScale FPGA Transceivers					
2018-06-27	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing a LogiCORE PCI Express System					
2018-01-23	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing a LogiCORE PCI Express System					
2018-04-16	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
PCIe Protocol					
2018-01-22	78, prospect Vernadskogo Moscow	MIREA	24,900.00 (RUB)	5	Register
PCIe Protocol					
2018-04-12	78, prospect Vernadskogo Moscow	MIREA	24,900.00 (RUB)	5	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-02-15	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Signal Integrity and Board Design for Xilinx FPGAs					
2018-05-17	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-06-04	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
DSP Design Using System Generator					
2018-05-14	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	15	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-02-26	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Advanced Features and Techniques of Embedded Systems Design					
2018-06-20	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Advanced Features and Techniques of Embedded Systems Software Design					
2018-04-09	78, prospect Vernadskogo Moscow	MIREA	24,900.00 (RUB)	5	Register
Embedded Systems Design					
2018-02-19	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Embedded Systems Design					
2018-06-06	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Embedded Design with PetaLinux Tools					
2018-05-21	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-19	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Embedded Systems Software Design					
2018-03-28	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Zynq-7000 All Programmable SoC					
2018-05-28	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Zynq UltraScale+ MPSoC for the Hardware Designer					
2018-03-05	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-01-29	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Zynq UltraScale+ MPSoC for the Software Developer					
2018-04-18	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with 7 Series					
2018-04-11	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register

Partial Reconfiguration					
2018-04-02	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with the UltraScale Architecture					
2018-04-23	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-02-12	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-06-13	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing FPGAs Using the Vivado Design Suite 3					
2018-03-01	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing FPGAs Using the Vivado Design Suite 4					
2018-03-15	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Advanced VHDL					
2018-03-22	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with System Verilog					
2018-02-05	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with System Verilog					
2018-05-30	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Verification with System Verilog					
2018-02-21	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Verification with System Verilog					
2018-06-25	78, prospect Vernadskogo Moscow	MIREA	48,900.00 (RUB)	10	Register
Designing with VHDL					
2018-03-12	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register
Designing with VHDL					
2018-05-24	78, prospect Vernadskogo Moscow	MIREA	72,900.00 (RUB)	15	Register

SPAIN

Date	Location	Facility	Price	TC	Reg. URL
Advanced Features and Techniques of Embedded Systems Design					
2018-10-17	Fco Tomas y Valiente 14	Universidad Autonoma de Madrid	980.00 (EUR)	12	Register
Embedded Design with PetaLinux Tools					
2018-10-29	Fco Tomas y Valiente 15	Universidad Autonoma de Madrid	980.00 (EUR)	12	Register

SPAIN

Date	Location	Facility	Price	TC	Reg. URL
Advanced Features and Techniques of Embedded Systems Design					
2018-10-17	Fco Tomas y Valiente 14	Universidad Autonoma de Madrid	980.00 (EUR)	12	Register
Embedded Design with PetaLinux Tools					
2018-10-29	Fco Tomas y Valiente 15	Universidad Autonoma de Madrid	980.00 (EUR)	12	Register

TAIWAN

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-01-24	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Embedded Systems Design					
2018-02-21	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Embedded C/C++ SDSoC Development Environment and Methodology					
2018-03-28	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Zynq-7000 All Programmable SoC					
2018-03-07	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Zynq UltraScale+ MPSoC for the System Architect					
2018-03-21	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Designing with the UltraScale Architecture					
2018-01-17	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-02-07	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register
Designing FPGAs Using the Vivado Design Suite 2					
2018-03-14	Taipei Taipei	E-Elements	20,000.00 (NTD)	6	Register

TN

Date	Location	Facility	Price	TC	Reg. URL
Designing a LogiCORE PCI Express System					
2018-02-07	Knoxville Knoxville	Knoxville, TN	1,600.00 (USD)	16	Register
PCIe Protocol					
2018-02-06	Knoxville Knoxville	Knoxville, TN	800.00 (USD)	8	Register

TX - DALLAS

Date	Location	Facility	Price	TC	Reg. URL
C-based design: High-Level Synthesis with Vivado HLx					
2018-04-25	3101 E. Pres George Bush Richardson	Avnet-Dallas	1,400.00 (USD)	14	Register
Designing FPGAs Using the Vivado Design Suite 1					
2018-04-10	3101 E. Pres George Bush Richardson	Avnet-Dallas	1,400.00 (USD)	14	Register

VA

Date	Location	Facility	Price	TC	Reg. URL
Essential DSP Implementation Techniques for Xilinx FPGAs					
2018-03-21	22685 Holiday Park Drive, Suite 60 Sterling	Executive Conference & Training Center - Sterling,VA	2,000.00 (USD)	20	Register
C-based design: High-Level Synthesis with Vivado HLx					
2018-03-05	22685 Holiday Park Drive, Suite 60 Sterling	Executive Conference & Training Center - Sterling,VA	1,800.00 (USD)	18	Register
Vivado Boot Camp Phase-2					
2018-01-17	22685 Holiday Park Drive, Suite 60 Sterling	Executive Conference & Training Center - Sterling,VA	2,700.00 (USD)	27	Register

WI - EASTERN

Date	Location	Facility	Price	TC	Reg. URL
Designing with Verilog and SystemVerilog					
2018-02-26	TBD Milwaukee	TBD	4,000.00 (USD)	40	Register
Designing with System Verilog					
2018-03-01	TBD Milwaukee	TBD	1,600.00 (USD)	16	Register
Designing with Verilog					
2018-02-26	TBD Milwaukee	TBD	2,400.00 (USD)	24	Register