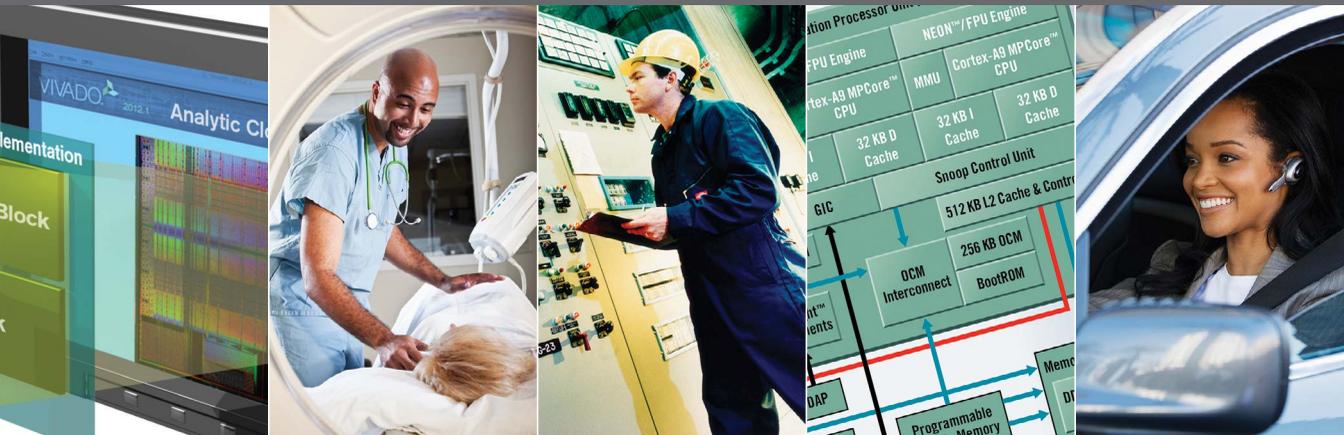


Xilinx Training Course Listing



Effective April 1, 2015

TABLE OF CONTENTS

Overview.....	1
Xilinx Training Course Listing.....	2
Core Design Skills.....	3
Product Training.....	4
Specialty Design Skills.....	6
Point Technologies.....	9
Application Specific.....	9
Languages.....	10
Xilinx Worldwide Training.....	11
Additional Training Resources.....	11

The Design Challenges of Time and Complexity

- System designers are faced with two rapidly growing challenges: shrinking time-to-market product development cycles; and the increasing complexity of product design
- Today's competitive environment demands the timely, efficient delivery of your most innovative solutions
- To beat the competition, you must be on budget, on time, every time

Xilinx Training— Training Solutions that Put You On The Fast Track to Success

Xilinx provides targeted, high-quality training designed by experts in programmable logic design, and delivered by Xilinx qualified trainers. We offer instructor-led classes and recorded e-learning for self-paced training. Some courses are completely free! To sign up for a class or to find out more go to www.xilinx.com/training.

Xilinx Productivity Advantage (XPA)— Everything You Need in a Customizable Bundle

The Xilinx Productivity Advantage (XPA) program allows you to create customized bundles of software and services to meet the specific needs of your team. An XPA provides for all of your FPGA design needs up-front through a one stop shopping experience. This solution bundle includes access to:

- Training credits that can be applied towards a comprehensive portfolio of hands-on training led by expert instructors.
- All of your user licenses for the industry-leading ISE™ design tools and development system options.
- Pre-verified and pre-optimized Intellectual Property (IP) cores and reference designs for Xilinx FPGAs.
- Complete suite of development and evaluation boards customized for your team's needs.

To find out how you can benefit from an XPA go to www.xilinx.com/xpa.

XILINX TRAINING COURSE LISTING

Xilinx offers public, private and online training available worldwide so you can be sure to find a training that best fits your needs. See below for a detailed description of all of the courses offered by Xilinx.

<p>Core Design Skills</p>	<p>Key for all designers. Focuses on tools, architecture, and methodology. From best practice FPGA design techniques through advanced skills and methodology to meet your design goals.</p>	<p>Xilinx Recommended Design Methodology Vivado Design Flows - Page 3 ISE Design Flows - Page 3</p>
<p>Product Training</p>	<p>Latest product training. Focused on in-depth training to become proficient using these products in the minimum time possible. Includes all new HW and SW products</p>	<p>Vivado Tool Flows - Page 4 ISE Tool Flows - Page 4 7-Series - Page 4 6-Series - Page 4 Zynq All Programmable SOC - Page 5</p>
<p>Specialty Design Skills</p>	<p>Focused training around specific types of FPGA design. DSP for video and communication markets. Connectivity for high-speed interfaces and Embedded design for BOM reduction and system integration in every market and application.</p>	<p>Embedded Design - Page 6 DSP Design - Page 7 Connectivity Design - Pages 7-8</p>
<p>Point Technologies</p>	<p>Training required on point technology solutions as High-Level Synthesis, AMS technology for ADC, Partial Reconfiguration, Memory, power Optimization, and On-Chip Debug.</p>	<p>Low-Power - Page 9 Debug - Page 9 Analog Mixed Signal - Page 9 Partial Reconfiguration - Page 9</p>
<p>Application Specific</p>	<p>Training targeted at applications in select markets.</p>	<p>Motor Control - Page 9 High Speed Networks - Page 9</p>
<p>Languages</p>	<p>Focus on language skills needed to create reliable and optimal hardware using Xilinx design tools. includes Hardware Description Languages (HDLs), such as Verilog, System Verilog, and VHDL, Tcl scripting language, and C language.</p>	<p>C - Page 10 Tcl - Page 10 Verilog and System Verilog - Page 10 VHDL - Page 10</p>

CORE DESIGN SKILLS

Vivado Design Flows

Essentials of FPGA Design

Level: 2

Duration: 2 days

Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set basic XDC timing constraints, and use the Vivado™ Design Suite to build, synthesize, implement, and download a design.

UltraFast Design Methodology

Level: 3

Duration: 1 day

This course describes the FPGA design best practices and skills to be successful using the Vivado™ Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an FPGA design methodology case study. The full FPGA Design Methodology Checklist is also introduced.

Vivado Design Suite Static Timing Analysis and Design Constraints

Level: 3

Duration: 2 days

This course offers detailed training on the Vivado software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

Advanced Tools and Techniques of Vivado Design Suite

Level: 4

Duration: 2 days

This course offers detailed training on the Vivado software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

ISE Design Flows

FPGA Design Techniques for Lower Cost

Level: 2

Duration: 1 day

This course will appeal to engineers who have an interest in developing low-cost products, particularly in high-volume markets. The course and exercises cover several different design techniques, which will be interesting and challenging for any digital designer regardless of the final application.

Essentials of FPGA Design

Level: 2

Duration: 1 day

Use the ISE® software tools to implement an FPGA design and gain a firm understanding of the Xilinx FPGA architecture. Learn the best design practices from the pros and understand the subtleties of the Xilinx design flow. This course covers ISE software features such as the Architecture Wizard, I/O Planner, and the Constraints Editor. Other topics include FPGA architecture, good design practices, understanding report contents, and global timing constraints.

Designing for Performance

Level: 3

Duration: 2 days

Attending the Designing for Performance class will help you create more efficient FPGA designs. This course will enable you to optimize your design for usage in a smaller FPGA or a lower speed grade for reducing system costs. In addition, by mastering the tools and the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Advanced FPGA Implementation

Level: 4

Duration: 2 days

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE design suite and Xilinx hardware. Labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools. This course requires the Essentials of FPGA Design and Designing for Performance courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE tools and 7 series FPGAs.

PRODUCT TRAINING

Vivado Tool Flows

Vivado Design Suite Tool Flow

Level: 1

Duration: 1 day

This course provides the overall context and framework for the development cycle of FPGAs. For those uninitiated to FPGA design, this course will arm you with the proper planning techniques, strategy, and FPGA tool flow to get up and designing an FPGA design now. The flow will take you from behavioral specification to tuning specifications for the FPGA, synthesis, verification, and onto implementation and download. Throughout the design cycle, the various tools within the Vivado™ Design Suite are introduced.

Vivado Design Suite for ISE Project Navigator Users

Level: 2

Duration: 1 day

This course offers introductory training on the Vivado Design Suite. This course is for experienced ISE software users who want to take full advantage of the Vivado Design Suite feature set. Learn about the Vivado Design Suite projects, design flow, Xilinx design constraints, and basic timing reports.

Vivado Design Suite–Advanced XDC and Timing Analysis for ISE Users

Level: 2

Duration: 2 days

This course will update experienced ISE software users to utilize the Vivado Design Suite. Learn the underlying database and static timing analysis (STA) mechanisms. Utilize Tcl for navigating the design, creating Xilinx design constraints (XDC), and creating timing reports. Learn to make appropriate timing constraints for SDR, DDR, source-synchronous, and system-synchronous interfaces for your FPGA design.

ISE Tool Flows

ISE Design Tool Flow

Level: 1

Duration: 1 day

ISE Design Tool Flow provides the overall context and framework for the development cycle of FPGAs. For those uninitiated to FPGA design, this course will arm you with the proper planning techniques, strategy, and FPGA tool flow to get up and designing an FPGA design now. The flow will take you from behavioral specification to tuning specifications for the FPGA, synthesis, verification, and onto implementation and download. Throughout the design cycle, the various tools within the Project Navigator tool are introduced.

Essential Design with the PlanAhead Analysis and Design Tool

Level: 2

Duration: 1 day

Learn to manage design performance, plan an I/O pin layout, and implement by using the PlanAhead™ software tool. Topics include: a tool overview, running a Design Rule Check (DRC) and Simultaneous Switching Noise (SSN) analysis of pin assignments, design and timing analysis, creating cores, and completing synthesis and implementation with the PlanAhead tool.

Advanced Design with the PlanAhead Analysis and Design Tool

Level: 3

Duration: 2 days

Learn to increase design performance and achieve repeatable performance by using the PlanAhead software tool. Topics include: synthesis and project tips, design analysis, creating a floorplan, improving performance with area constraints and Pblocks, design debugging with the ChipScope™ Pro tool, and design preservation with partitions.

7-Series

Designing with the 7 Series Families

Level: 3

Duration: 2 days

Are you interested in learning how to effectively utilize 7 series architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the Essentials of FPGA Design course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family. Topics covered include device overviews, CLB construction, MMCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, FIFO resources, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the families (PCI Express technology, analog to digital converters and gigabit transceivers) are also introduced. This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

6-Series

Designing with the Spartan-6 and Virtex-6 Families

Level: 3

Duration: 3 days

Are you interested in learning how to effectively utilize Spartan®-6 or Virtex®-6 FPGA architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the Essentials of FPGA Design course. This course focuses on understanding as well as how to properly design for the primary resources found in these popular device families. Topics covered include device overviews, CLB construction, DCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the sub-families (EMAC, PCI Express® technology, and GTP transceivers) are also introduced. This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught. A two-day Spartan-6 family only course or two-day Virtex-6 family only course is also available.

PRODUCT TRAINING

Zynq All Programmable SOC

Introduction to the Zynq All Programmable SoC Architecture

Level: 3

Duration: 1 day

This course provides hardware and firmware engineers with the knowledge to effectively utilize a Zynq™ All Programmable System on a Chip (SoC). It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL). The course also details the individual components that comprise the PS, I/O peripherals, timers, and caching, as well as the DMA, interrupt, and memory controllers. Emphasis will be placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques.

Zynq All Programmable SoC System Architecture

Level: 3

Duration: 2 days

The Xilinx Zynq All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides experienced system architects with the knowledge to effectively architect a Zynq All Programmable SoC. This course presents the features and benefits of the Zynq architecture for making decisions on architecting a Zynq All Programmable SoC project. It covers the architecture of the ARM Cortex-A9 processor-based processing system (PS) and the integration of programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC. The course also details the individual components that comprise the PS, I/O peripherals, timers, and caching, as well as the DMA, interrupt, and memory controllers. Emphasis will be placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

SPECIALTY DESIGN SKILLS

Embedded Design

Essentials of Microprocessors

Level: 1

Duration: 1 day

Learn what makes microprocessors tick! This class offers insights into all major aspects of microprocessors, from registers through coprocessors and everything in between. Differences between RISC and CISC architectures are explored as well as the concept of interrupts. A generic microprocessor is programmed and run in simulation to reinforce the principles learned in the lecture modules. The student will leave the class well prepared for the Xilinx Zynq training curriculum.

How to Design Xilinx Embedded Systems in One Day

Level: 2

Duration: 1 day

The workshop introduces you to fundamental embedded design concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of Xilinx embedded tools, IP, and the Embedded Targeted Reference Design (TRD). Design examples and labs are drawn from the Embedded TRD. Only essential theory is introduced in order to lay a foundation for the material and topics covered in this workshop, which complements more detailed training found in subsequent Xilinx courses.

Embedded Systems Design

Level: 3

Duration: 2 days

The Xilinx Zynq All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course brings experienced FPGA designers up to speed on developing embedded systems using the Embedded Development Kit (EDK). The features and capabilities of the Zynq All Programmable SoC as well as concepts, tools, and techniques are included in the lectures and labs. The hands-on labs provide students with experience designing, expanding, and modifying an embedded system, including adding and simulating a custom AXI-based peripheral. Additionally, the features and capabilities of the Xilinx MicroBlaze™ soft processor are also included in the lectures and labs.

Embedded Systems Software Design

Level: 3

Duration: 2 days

This two-day course introduces you to software design and development for the Xilinx Zynq All Programmable System on a Chip (SoC) using the Xilinx Software Development Kit (SDK). You will learn the concepts, tools, and techniques required for the software phase of the design cycle. Topics are comprehensive, covering the design and implementation of the board support package (BSP) for resource access and management of the Xilinx Standalone library. Major topics include device driver use and custom development and user application debugging and integration. Practical implementation tips and best practices are also provided throughout to enable you to make good design decisions and keep your design cycles to a minimum. You will have enough practical information to start developing software applications for the ARM Cortex-A9 and MicroBlaze processors. Additionally, this course covers developing software applications for a Xilinx embedded system based on a MicroBlaze processor.

Advanced Features and Techniques of Embedded Systems Design

Level: 4

Duration: 2 days

Advanced Features and Techniques of Embedded Systems Design provides embedded systems developers the necessary skills to develop complex embedded systems and enables them to improve their designs by using the tools available in the Vivado™ IP Integrator. This course also helps developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq™ All Programmable System on a Chip (SoC) or Microblaze™ soft processor. This course builds on the skills gained in the Embedded Systems Design course. Labs provide hands-on experience with developing, debugging, and simulating an embedded system. Utilizing memory resources and implementing high-performance DMA are also covered. Labs use demo boards in which designs are downloaded and verified.

Advanced Features and Techniques of Embedded Systems Software Design

Level: 4

Duration: 1 day

This course will help software engineers fully utilize the components available in the Zynq All Programmable System on a Chip (SoC) processing system (PS). This course covers advanced Zynq All Programmable SoC topics for the software engineer, including advanced boot methodology, the NEON co-processor, programming PS system-level function control registers, the general interrupt controller, the DMA, Ethernet, and USB controllers, and the various low-speed peripherals included in the Zynq processing system.

Embedded Design with PetaLinux Tools

Level: 4

Duration: 2 days

This intermediate-level, two-day course provides embedded systems developers with experience in creating an embedded PetaLinux SDK operating system on a Xilinx Zynq All Programmable System on a Chip (SoC) processor development board. The course offers students hands-on experience on building the environment and booting the system using a basic Zynq All Programmable SoC design with PetaLinux SDK on the ARM Cortex-A9 processor. This course also introduces embedded Linux components, use of open-source components, environment configurations, network components, and debugging/profiling options for embedded Linux platforms. The primary focus is on embedded Linux development in conjunction with the Xilinx tool flow.

SPECIALTY DESIGN SKILLS

DSP Design

How to Design a Xilinx Digital Signal Processing System in One Day

Level: 3

Duration: 1 day

This workshop introduces you to fundamental DSP concepts, algorithms, and techniques for implementation in Xilinx FPGAs. Design examples and labs are drawn from several common applications spaces, including wireless communications, video, and imaging. Only essential theory is introduced in order to lay a foundation for the material and topics covered in this workshop, which complements more detailed training found in subsequent Xilinx courses. The material is also complementary to the Avnet SpeedWay Design Workshop on FPGA-Based System Design with High-Speed Data Converters.

Essential DSP Implementation Techniques for Xilinx FPGAs

Level: 3

Duration: 2 days

This course provides a foundation for Digital Signal Processing (DSP) techniques for Xilinx FPGAs. The course begins with a refresher of basic binary number theory, mathematics, and the essential features within the FPGA that are important to signal processing. The body of the course explores a variety of filter techniques with emphasis on optimal implementation in Xilinx devices and continues with an examination of FFTs, video, and image processing. Throughout the course, Xilinx cores and IP relevant to signal processing are introduced. The course is complemented by hands-on exercises to reinforce the concepts learned.

DSP Design Using System Generator

Level: 3

Duration: 2 days

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost Digital Signal Processing designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

C-Based Design: High-Level Synthesis with Vivado HLS

Level: 3

Duration: 2 days

The course provides a thorough introduction to Vivado HLS (high-level synthesis). This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. Utilize Vivado HLS to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

Connectivity Design

How to Design a Xilinx Connectivity System in One Day

Level: 2

Duration: 1 day

This workshop introduces you to fundamental connectivity concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of transceivers, PCIe® technology, memory interfaces, and Ethernet MACs. Only essential theory is introduced in order to lay a foundation for the material and topics covered in this workshop, which complements more detailed training found in subsequent Xilinx courses. Design examples and labs are drawn from the Connectivity Targeted Reference Design (TRD). In addition, an IBERT lab is available that highlights use of the MGT.

PCIe Protocol Overview

Level: 2

Duration: 1 day

This course focuses on the fundamentals of the PCI Express protocol specification. The typical PCIe architecture, including data space, data movement, and the most commonly used Transaction Layer Packets (TLPs) are covered. Interrupts and error handling are also discussed.

Designing a LogiCORE PCI Express System

Level: 3

Duration: 2 days

Attending the Designing a LogiCORE PCI Express System will provide you a working knowledge of how to implement a Xilinx PCI Express core in your applications. This course focuses on the implementation of a Xilinx PCI Express system within the Connectivity Targeted Reference Design (TRD). With this experience, you can improve your time to market with your PCIe core design. Various Xilinx PCI Express core products will be enumerated to aid you in selecting the proper solution. This course focuses on the AXI streaming interconnect.

Designing with Multi-Gigabit Serial I/O

Level: 3

Duration: 3 days

Learn how to employ GTP and GTX serial transceivers in your 7 series FPGA design. Understand and utilize the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection. Additional topics include use of the Architecture Wizard, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

Designing with Ethernet MAC Controllers

Level: 3

Duration: 2 days

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements.

SPECIALTY DESIGN SKILLS

Connectivity Design

Signal Integrity and Board Design for Xilinx FPGAs

Level: 3

Duration: 3 days

Learn when and how to apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and other components. This comprehensive course combines design techniques and methodology with relevant background concepts of high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using Mentor Graphics HyperLynx. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules with instructor demonstrations and practical hands-on labs.

How to Design a High-Speed Memory Interface

Level: 3

Duration: 2 days

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debugging using 7 series FPGAs. Additionally, students will learn about the tools available for high-speed memory interface design, debug, and implementation of high-speed memory interfaces. The major memory types covered are DDR2 and DDR3. The following memory types are covered on demand: RLDRAMII, LPDDR, and QDRII+. Labs are available for DDR3 on the Kintex™-7 FPGA KC705 board.

POINT TECHNOLOGIES

FPGA Power Optimization

Level: 2

Duration: 1 day

Attending the FPGA Power Optimization class will help you create a more power efficient FPGA design. This course can help you fit your design into a smaller FPGA, reduce your FPGA's power consumption, or run your FPGA at a lower temperature. In addition, by mastering the tools and design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Debugging Techniques Using the Vivado

Level: 2

Duration: 1 day

Logic Analyzer

As FPGA designs become increasingly more complex, designers continue look to reduce design and debug time. The powerful, yet easy-to-use Vivado® logic analyzer debug solution helps minimize the amount of time required for verification and debug. This one-day course will not only introduce you to the cores and tools and illustrate how to use the triggers effectively, but also show you effective ways to debug designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the Vivado debug tool can address advanced verification and debugging challenges.

Designing with the Xilinx

Level: 3

Duration: 1 day

Analog Mixed Signal Solution

This course introduces the Xilinx Analog Mixed Signal (AMS) solution and the appropriate tools and techniques for hardware engineers and analog engineers to utilize this solution. The complete front-to-back design flow is covered, including the evaluation of the Xilinx Analog-to-Digital Converter (XADC) block utilizing the KC705 board and the evaluator add-on card, the various ways to include the XADC in your design, XADC simulation of an analog input, viewing the digital output, and implementation. Additionally, labs are provided that support each topic, including the complete flow.

Xilinx Partial Reconfiguration

Level: 4

Duration: 2 days

Tools and Techniques

This course demonstrates how to use the ISE, PlanAhead, and Embedded Development Kit (EDK) software tools to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow. This course covers both the tool flow and mechanics of successfully creating a PR design. It also describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications.

APPLICATION SPECIFIC

Industrial Motor Control Using FPGAs and SoCs

Level: 1

Duration: 1 day

Learn how to implement motor control solutions using Xilinx All Programmable devices. This course requires basic knowledge of motor control; this comprehensive course covers motor control concepts; identifies the challenges in typical motor control solutions such as brushless direct current (DC), stepper, and permanent magnet synchronous motor (PMSM) motor control solutions and then demonstrates motor control techniques in Xilinx FPGAs and SoCs with the help of IPs provided by QDESYS.

High Speed (500 Mhz) Design Techniques for Smart Networks

Level: 1

Duration: 1 day

Implement next generation wireless performance @ 491 MHz designs in Kinex-7 (-2 speed grade) devices. Utilize the architecture in VHDL to meet this design goal. Identify the methodology, architecture, techniques, IP, and tools that will enable this performance.

LANGUAGES

C

C Language Programming with SDK

Level: 1

Duration: 2 days

This course is broken into a day of C language review, including variable naming, usage, and modifiers as well as an introduction to the Software Development Kit (SDK) environment, an explanation of the use of the preprocessors, program control, and proper use of functions. The second day consists of common issues and techniques employed by embedded programmers in the Xilinx SDK environment. This comprehensive course equally balances lecture modules with practical hands-on lab work.

C-based HLS Coding for Hardware Designers

Level: 3

Duration: 1 day

C-based coding is increasingly used for the modeling and high-level synthesis of hardware components. This course provides hardware engineers with sufficient knowledge of C-programming techniques for Vivado HLS to take advantage of Xilinx FPGAs. Learn high-level synthesis best practices, methodology, and subtleties of C-based coding for hardware modeling, synthesis, and verification.

C-Based HLS Coding for Software Designers

Level: 3

Duration: 1 day

C-based coding is increasingly used for the modeling and high-level synthesis of hardware components. This course provides software engineers with sufficient knowledge of FPGA hardware to efficiently code for high-level synthesis. Learn the high-level synthesis best practices, methodology, and subtleties of C-based coding for hardware modeling, synthesis, and verification.

Tcl

Essential Tcl Scripting for the Vivado Design Suite

Level: 1

Duration: 1 day

Learn how to use basic Tcl syntax and language structures to build scripts suitable for use with Xilinx FPGA design tools. Learn about the effective use of variables, data types, and Tcl constructs to build effective conditional statements and loop controls. You will also have the opportunity to use Tcl language constructs with several labs designed to provide you scripting experience within the Vivado Design Suite.

Verilog and System Verilog

Designing with Verilog

Level: 1

Duration: 3 days

Learn when and how to apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and other components. This comprehensive course combines design techniques and methodology with relevant background concepts of high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using Mentor Graphics HyperLynx. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules with instructor demonstrations and practical hands-on labs.

Designing with System Verilog

Level: 1

Duration: 2 days

This comprehensive course is a thorough introduction to SystemVerilog constructs for design. This class addresses writing RTL code using the new constructs available in SystemVerilog. New data types, structs, unions, arrays, procedural blocks, re-usable tasks and functions, and packages, are all covered. The information gained can be applied to any digital design. This course combines insightful lectures with practical lab exercises to reinforce key concepts.

Verification with System Verilog

Level: 1

Duration: 2 days

This comprehensive course is a thorough introduction to SystemVerilog constructs for design. This class addresses writing RTL code using the new constructs available in SystemVerilog. New data types, structs, unions, arrays, procedural blocks, re-usable tasks and functions, and packages, are all covered. The information gained can be applied to any digital design. This course combines insightful lectures with practical lab exercises to reinforce key concepts.

VHDL

Designing with VHDL

Level: 1

Duration: 3 days

This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, Register Transfer Level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn best coding practices that will increase your overall VHDL proficiency.

Advanced VHDL

Level: 4

Duration: 2 days

Increase your VHDL proficiency by learning advanced techniques that will help you write more robust and reusable code. This comprehensive course is targeted toward designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs as compared to lecture modules.

XILINX WORLDWIDE TRAINING

Xilinx training courses are offered by Authorized Training Providers (ATPs) in most regions of the world, providing you expert training opportunities. Customer courses offered by our ATPs use high-quality training materials developed by Xilinx, and leverage the specialized knowledge and extensive network of our ATPs. Pricing and availability of classes varies by region.

AUTHORIZED TRAINING PARTNER	CONTACT	COUNTRY/REGION(S) SUPPORTED
Xilinx Training Worldwide	www.xilinx.com/training	Worldwide
AMERICAS	registrar@xilinx.com	
Anacom Eletrônica	www.anacom.com.br	Brazil
Bottom Line Technologies	www.bltn.com	Delaware, District of Columbia, Maryland, New Jersey, New York, Eastern Pennsylvania, Virginia
Doulos	www.doulos.com/xilinx	Northern California
Faster Technology	www.fastertechology.com	Arkansas, Colorado, Louisiana, Montana, Oklahoma, Southern Idaho, Texas, Utah, Wyoming
Hardent	www.hardent.com	Alabama, Connecticut, Eastern Canada, Florida, Georgia, Maine, Massachusetts, Mississippi, New Hampshire, North Carolina, Rhode Island, South Carolina, Tennessee, Vermont
North Pole Engineering	www.npe-inc.com	Illinois, Iowa, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, Wisconsin
Technically Speaking	www.technically-speaking.com	Arizona, British Columbia, Southern California, Northern Idaho, New Mexico, Nevada, Oregon, Washington
VAI Logic	www.vailogic.com	Indiana, Kentucky, Michigan, Ohio, Western Pennsylvania, West Virginia
EUROPE, MIDDLE EAST, & AFRICA (EMEA)	eurotraining@xilinx.com	
Core Vision	www.core-vision.nl	The Netherlands, Belgium, Luxemburg
Doulos	www.doulos.com/xilinx	United Kingdom, Ireland, Norway, Finland, Denmark
Inline Group	www.plis.ru	Russia (North)
Logtel Computer Communications	www.logtel.com	Israel, Turkey
Mindway	www.mindway-design.com	Italy
Multi Video Designs (MVD)	www.mvd-fpga.com	France, Spain, Portugal, Switzerland
Prevas	www.prevas.com/xilinx	Sweden, Norway, Denmark, Finland, Lithuania, Latvia, Estonia
Programmable Logic Competence Center (PLC2)	www.plc2.com/	Germany, Switzerland, Poland, Hungary, Czech Republic, Slovakia, Slovenia, Greece, Cyprus, Turkey, Russia
SO-Logic Consulting	www.so-logic.co.at	Austria, Hungary, Slovakia, Slovenia, Turkey
ASIA PACIFIC	education_ap@xilinx.com	
Activemedia Innovation	www.activemedia.com.sg	Malaysia, Singapore, Thailand
Black Box Consulting	www.blackboxconsulting.com.au	Australia, New Zealand
E-elements	www.e-elements.com	China, Hong Kong, Taiwan
Libertron	www.libertron.com	Korea
OE-Galaxy	www.oegalaxy.com.vn	Vietnam
Sandeepani Programmable Solutions	www.sandeepani-training.com	India
WeDu Solution	www.wedusolution.com	Korea
JAPAN	education_kk@xilinx.com	
Avnet Japan	www.avnet.co.jp/training.aspx	Tokyo
HD Lab	www.hdlab.co.jp	Japan
Paltek	www.paltek.co.jp	Yokohama
Shinko Shoji	xilinx.shinko-sj.co.jp	Tokyo
Tokyo Electron Device	ppg.teldevice.co.jp	Yokohama

ADDITIONAL TRAINING RESOURCES

Curriculum Paths — Curriculum paths illustrate the recommended course sequence to follow based on your design specialization. Because Xilinx courses build on each other, you must meet the prerequisites to gain the full benefit of each course. Prerequisites are outlined in the course descriptions.

Recorded e-Learning — Recorded e-Learnings are currently available at no charge, over the Internet anytime, day or night, worldwide to allow you to get up to speed quickly. New topics each month, such as: Clocking Techniques, Timing Closure, DDR Memory Interface, FPGA vs. ASIC, etc.

www.xilinx.com/training/free-video-courses.htm

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
Web: www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
Web: www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
Web: japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
Web: www.xilinx.com



www.xilinx.com