

Xilinx Training Course Listing



Effective May 1, 2012

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The Design Challenges of Time and Complexity

- System designers are faced with two rapidly growing challenges: shrinking time-to-market product development cycles; and the increasing complexity of product design
- Today's competitive environment demands the timely, efficient delivery of your most innovative solutions
- To beat the competition, you must be on budget, on time, every time

Xilinx Training— Training Solutions that Put You On The Fast Track to Success

Xilinx provides targeted, high-quality training designed by experts in programmable logic design, and delivered by Xilinx qualified trainers. We offer instructor-led classes and recorded e-learning for self-paced training.

Some courses are completely free!

To sign up for a class or to find out more go to www.xilinx.com/training.

Xilinx Productivity Advantage (XPA)— Everything You Need in a Customizable Bundle

The Xilinx Productivity Advantage (XPA) program allows you to create customized bundles of software and services to meet the specific needs of your team. An XPA provides for all of your FPGA design needs up-front through a one stop shopping experience. This solution bundle includes access to:

- Training credits that can be applied towards a comprehensive portfolio of hands-on training led by expert instructors.
- All of your user licenses for the industry-leading ISE™ design tools and development system options.
- Pre-verified and pre-optimized Intellectual Property (IP) cores and reference designs for Xilinx FPGAs.
- Complete suite of development and evaluation boards customized for your team's needs.

To find out how you can benefit from an XPA go to www.xilinx.com/xpa.

XILINX TRAINING COURSE LISTING

Xilinx offers public, private and online training available worldwide so you can be sure to find a training that best fits your needs. See below for a detailed description of all of the courses offered by Xilinx.

INSTRUCTOR-LED TRAINING COURSES	LEARNING LEVEL
FPGA Curriculum	
ISE Design Tool Flow	1
Designing with Verilog	
Designing with VHDL	
FPGA Design for ASIC Users	
Essentials of FPGA Design	2
Design Techniques for Lower Costs	
Debugging Techniques Using the ChipScope Pro Tools	
Essential Design with the PlanAhead Analysis and Design Tool	
Designing for Performance	3
Advanced Design with the PlanAhead Analysis and Design Tool	
Designing with the Spartan-6 and Virtex-6 Families	
Designing with the 7 Series Families	
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Advanced Zynq EPP Embedded System Software Design	4
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Connectivity Curriculum	
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Designing a LogiCORE PCI Express System	3
Designing with Multi-Gigabit Serial I/O	
Designing with Ethernet MAC Controllers	
Serial Integrity and Board Design for Xilinx FPGAs	
How to Design a High-Speed Memory Interface	
DSP Curriculum	
How to Design a Xilinx Digital Signal Processing System in One Day	2
Essentials of DSP Implementation Techniques for Xilinx FPGA	3
DSP Design Using System Generator	4

FPGA CURRICULUM

ISE Design Tool Flow

Level: 1

Duration: 1 day

The ISE Design Tool Flow class provides the overall context and framework for the development cycle of FPGAs. For those uninitiated to FPGA design, this course will arm you with the proper techniques, strategy, and FPGA tool flow to get up and designing an FPGA now! The flow will take you from behavioral specification to tuning specifications for the FPGA, coding, synthesis, verification, and onto implementation and download. Throughout the design cycle, the various tools within the Project Navigator tool are introduced.

Designing with Verilog

Level: 1

Duration: 3 days

This comprehensive course is an effective introduction to the Verilog language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis approach. This course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Designing with VHDL

Level: 1

Duration: 3 days

This comprehensive course is an effective introduction to the VHDL language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis design approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

FPGA Design for ASIC Users

Level: 1

Duration: 1 day

Attending the FPGA Design for ASIC Users course will help you to create fast and efficient FPGA designs by leveraging your ASIC design experience. This course will help you avoid the most common design mistakes of FPGA designers. It will also help you fit your design into a smaller FPGA or a lower speed grade for reducing system costs. In addition, by mastering the design methodologies presented in this course, you will be able to create your design faster, shorten your development time, reduce your debug time, and lower development costs.

Essentials of FPGA Design

Level: 2

Duration: 1 day

Understand Xilinx FPGA architecture and learn to implement a complete design in one day. This course provides you with an introduction to designing with Xilinx FPGAs using Xilinx ISE™ software. Features covered in this course include the Architecture Wizard, pin assignments, design planning, implementation options, and global timing constraints. Reduce your learning curve through several practical labs.

Design Techniques for Lower Cost

Level: 2

Duration: 1 day

This workshop will appeal to engineers who have an interest in developing low-cost products, particularly in high-volume markets. The workshop covers several different design techniques — such as estimating design size, applying design techniques, and exploring creative ways to use FPGA memory resources — all in an effort to reduce design costs. This course features the Spartan™ family of devices.

Debugging Techniques Using the ChipScope Pro Tools

Level: 2

Duration: 2 days

As FPGA designs become increasingly more complex, many Xilinx customers are searching to reduce their design time and debug their designs with powerful yet easy-to-use tools. The Xilinx ChipScope Pro™ tool solution helps minimize the amount of time required for debug and verification, which can often consume a significant amount of total FPGA design time. In this one-day course, you will learn effective ways to debug logic and high-speed designs — thereby decreasing your overall design time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address debugging and verification challenges.

Essential Design with the PlanAhead Analysis and Design Tool

Level: 2

Duration: 1 day

Learn to increase design performance and achieve repeatable results by using the PlanAhead software. Topics include: a product overview, synthesis and project tips, design analysis, creating a floorplan, improving performance, experimenting with implementation options, incremental methodology, block-based IP design, and I/O pin assignment.

FPGA CURRICULUM

Designing for Performance

Level: 3

Duration: 2 days

Learn techniques to help improve your design's performance. This course builds on the principles covered in our Level 1 & 2 of FPGA Design course with an emphasis on achieving timing closure. Topics include FPGA design techniques, HDL coding techniques, the CORE Generator™ system, power estimation, timing analysis, timing constraints, and implementation options.

Advanced Design with the PlanAhead Analysis and Design Tool

Level: 3

Duration: 2 days

Learn to increase design performance and achieve repeatable performance by using the PlanAhead™ software tool. Topics include: synthesis and project tips, design analysis, creating a floorplan, improving performance with area constraints and Pblocks, design debugging with the ChipScope™ Pro tool, and design preservation with partitions.

Designing with the Virtex-5 Family

Level: 3

Duration: 1 day

Interested in learning how to effectively utilize Virtex™-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed Level 2 and 3 Essentials of FPGA Design and Designing for Performance and have a comprehensive knowledge of Virtex-4 FPGAs, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device.

Designing with the Spartan-6 and Virtex-6 Families

Level: 3

Duration: 3 days

Are you interested in learning how to effectively utilize Spartan-6 FPGA or Virtex-6 FPGA architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the Essentials of FPGA Design course. This course focuses on understanding as well as how to properly design for the primary resources found in these popular device families.

Designing with 7 Series Families

Level: 3

Duration: 2 days

Are you interested in learning how to effectively utilize 7 series architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the Essentials of FPGA Design course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family.

Agile Mixed Signal

Level: 3

Duration: 1 day

Learn to utilize Xilinx' Agile Mixed Signal (AMS) solution and the appropriate tools and techniques for HW design engineers and analog engineers to utilize this solution. Covers the various ways to include the XADC in your design and implementation.

FPGA Power Optimization

Level: 3

Duration: 1 day

Covers FPGA power requirements, power management design techniques and software options, power estimation and analysis, as well as solving power issues.

Advanced FPGA Implementation

Level: 4

Duration: 2 days

Push the limits of your design by learning techniques that will increase your overall proficiency. This course builds on the principles covered in our Level 2 and 3 Essentials of FPGA Design and Designing for Performance courses. Some of the concepts that you will learn include incremental and modular design techniques, creating floorplans, using scripting, implementing relationally placed macros, editing and simplifying constraints files, using FPGA Editor for implementation editing, and using clock resources effectively.

Advanced VHDL

Level: 4

Duration: 2 days

Increase your VHDL proficiency by learning techniques to help you write more robust and reusable code. This comprehensive course is targeted towards designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs, as compared to lecture modules.

Xilinx Partial Reconfiguration Tools and Techniques

Level: 4

Duration: 2 days

This course demonstrates how to use the ISE™, PlanAhead™, and Embedded Developers Kit software tools to construct, implement, and download a partially reconfigurable FPGA design. You will gain a firm understanding of Partially Reconfigurable (PR) technology and learn how successful PR designs are completed. You will also learn the best design practices from the pros and understand the subtleties of the PR design flow.

EMBEDDED CURRICULUM

Essentials of Microprocessors

Level: 1

Duration: 2 days

Learn what makes microprocessors tick! This class offers insights into all major aspects of microprocessors, from registers through coprocessors and everything in between. Differences between RISC and CISC architectures are explored as well as the concept of interrupts. A generic microprocessor is programmed and run in simulation to reinforce the principles learned in the lecture modules. The student will leave the class well prepared for the Xilinx Zynq training curriculum.

C-Programming with Xilinx SDK

Level: 1

Duration: 2 days

Looking for a hands-on approach to developing embedded systems? Attend this training to gain a better understanding of developing a PowerPC™ and MicroBlaze™ embedded system by using the Embedded Development Kit (EDK). This course will provide hands-on labs regarding the development, debug, and simulation of the embedded system. Labs provide users with a choice of targeting either PowerPC or MicroBlaze systems.

How to Design Xilinx Embedded Systems in One Day

Level: 2

Duration: 1 day

The workshop introduces you to fundamental embedded design concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of Xilinx embedded tools, IP, and the Embedded Targeted Reference Design (TRD). Design examples and labs are drawn from the Embedded TRD.

Zynq-7000 EPP Architecture Details

Level: 3

Duration: 1 day

Covers the internal architecture of the ARM subsystem, as implemented in the Zynq Architecture. Enables a software designer, writing in 'C', to successfully and effectively utilize the ARM subsystem. Enables the HW designer to effectively bridge the processor to FPGA fabric. Details of the ZynqPS peripherals along with PS architecture are covered.

Zynq-7000 EPP Systems Architect

Level: 3

Duration: 1 day

Learn how to effectively architect a Zynq processor based FPGA design. Utilize Zynq architecture features and processor sub-system effectively while coordinating and balancing with the design in FPGA fabric. Explanation and implementation of the various architecture options for AXI interfaces and PS pipelining are included, along with options for system boot and FPGA configuration.

Embedded Systems Development

Level: 3

Duration: 2 days

This course introduces you to software design and development for Xilinx embedded processor systems. You will learn the basic tool use and concepts required for the software phase of the design cycle, after the hardware design is completed. You will have enough practical information to get started developing the software platform for a Xilinx embedded system based on a PowerPC® 440 or MicroBlaze™ processor. Hardware design concepts and procedures are not covered.

SDK Embedded Systems Software Development

Level: 3

Duration: 2 days

Looking for a hands-on approach to developing embedded systems? Attend this training to gain a better understanding of developing a PowerPC™ and MicroBlaze™ embedded system by using the Embedded Development Kit (EDK). This course will provide hands-on labs regarding the development, debug, and simulation of the embedded system. Labs provide users with a choice of targeting either PowerPC or MicroBlaze systems.

Advanced Embedded Systems Development

Level: 4

Duration: 2 days

Understand and utilize components of embedded systems design in order to architect a complex system. This course builds on the skills learned in the Embedded Systems Development course. Topics include external memory interfacing using various memory interface cores; enhancing performance through profiling, caching, and dedicated links; hardware and software debugging using the Xilinx software debugger and ChipScope Pro; bus functional models and simulation; interrupts, setting counter timer facilities and the PPC core clock; OCM; board support package using Xilinx lightweight kernel and Linux; and debugging techniques. The majority of this course is spent on practical hands-on lab work such as external memory interfacing, hardware and software debugging using ChipScope Pro, bootloader, simulation using bus functional model, and profiling.

Advanced SDK Zynq Embedded Systems Software

Level: 4

Duration: 1 day

Covers the details of utilizing the Zynq processor, including advanced boot methodologies, boot memory options, Cortex A9 processor services, advanced DMA controller configuration, and high and low speed peripheral configurations.

Embedded Design with PetaLinux SDK

Level: 4

Duration: 2 days

This course provides embedded systems developers with experience in creating an embedded open-source Linux operating system on a Xilinx development board for the MicroBlaze processor. The course offers students hands-on experience from building the environment to booting the system using a basic, single-processor System on Chip (SoC) design with PetaLinux. The primary focus is on embedded Linux development in conjunction with the Xilinx tool flow.

CONNECTIVITY CURRICULUM

PCIe Protocol Overview

Level: 2

Duration: 1 day

This course focuses on the fundamentals of the PCI Express® protocol specification. The typical PCIe architecture, including data space, data movement, and the most commonly used Transaction Layer Packets (TLPs) are covered. Interrupts and error handling are also discussed.

How to Design a Xilinx Connectivity System in One Day

Level: 2

Duration: 1 day

This workshop introduces you to fundamental connectivity concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of transceivers, PCIe® technology, memory interfaces, and Ethernet MACs.

Designing a LogiCORE PCI Express System

Level: 3

Duration: 2 days

By learning PCI Express core protocol, designers can gain a working knowledge of how PCI Express can be used in their systems. This course focuses on the PCI Express protocol subjects that designers, using the Xilinx PCI Express core should understand to complete their designs faster and easier. Students will also be introduced to each Xilinx PCI Express core product and will gain intimate knowledge of how the PCI Express core operates.

Designing with Multi-Gigabit Serial I/O

Level: 3

Duration: 2 days

Learn how to employ RocketIO™ in your Virtex-II Pro design. Understand and utilize the features of the RocketIO transceiver blocks, such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, synthesis and implementation considerations, and standards compliance. This comprehensive course equally balances lecture modules with practical hands-on lab work.

Designing with Ethernet MAC Controllers

Level: 3

Duration: 2 days

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements.

Signal Integrity and Board Design for Xilinx FPGAs

Level: 3

Duration: 3 days

Learn how signal integrity techniques are applicable to high-speed interfaces between Xilinx FPGAs and semiconductor memories. This course teaches you about high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using CAD packages. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules and practical hands-on labs.

How to Design a High-Speed Memory Interface

Level: 3

Duration: 2 days

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debugging using Spartan®-6 and Virtex®-6 FPGAs. Additionally, you will learn about the tools available for high-speed memory interface design, implementation, and debugging. The major memory types covered are DDR, DDR2, DDR3, RLDRAMII, LPDDR, QDRII, and QDRII+. Labs are available for DDR2 on the SP601, DDR3 on the ML605, or DDR3 on the SP605 demo board.

DSP CURRICULUM

How to Design a Xilinx Digital Signal Processing System in One Day

Level: 2

Duration: 1 day

The workshop introduces you to fundamental DSP concepts, algorithms, and techniques for implementation in Xilinx FPGAs. Design examples and labs are drawn from several common applications spaces, including wireless communications, video, and imaging.

Essential DSP Techniques for Xilinx FPGAs

Level: 3

Duration: 2 days

This course shows you how to take advantage of the features available in the Xilinx FPGA architecture, including the Virtex™-6 & Spartan-6 FPGAs, and describes how DSP algorithms can be implemented efficiently. The techniques also demonstrate which decisions at the system level have the greatest impact on the implementation process and product costs.

DSP Design Using System Generator

Level: 4

Duration: 2 days

This course allows you to explore the System Generator tool and to gain the expertise you need to develop Level 3, low-cost DSP designs. This Level 3 course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

XILINX WORLDWIDE TRAINING

Xilinx training courses are offered by Authorized Training Providers (ATPs) in most regions of the world, providing you expert training opportunities. Customer courses offered by our ATPs use high-quality training materials developed by Xilinx, and leverage the specialized knowledge and extensive network of our ATPs. Pricing and availability of classes varies by region.

AUTHORIZED TRAINING PARTNER	CONTACT	COUNTRY/REGION(S) SUPPORTED
Xilinx Training Worldwide	www.xilinx.com/training	Worldwide
AMERICAS		
Anacom Eletrônica	www.anacom.com.br	Brazil
Bottom Line Technologies	www.bltinc.com	Delaware, District of Columbia, Maryland, New Jersey, New York, Eastern Pennsylvania, Virginia
Doulos	www.doulos.com/XilinxNC	Northern California
Faster Technology	www.fastertechnology.com	Arkansas, Colorado, Louisiana, Montana, Oklahoma, Southern Idaho, Texas, Utah, Wyoming
Hardent	www.hardent.com	Alabama, Connecticut, Eastern Canada, Florida, Georgia, Maine, Massachusetts, Mississippi, New Hampshire, North Carolina, Rhode Island, South Carolina, Tennessee, Vermont
North Pole Engineering	www.npe-inc.com	Illinois, Iowa, Kansas, Minnesota, Missouri, Nebraska, North Dakota, South Dakota, Wisconsin
Technically Speaking	www.technically-speaking.com	Arizona, British Columbia, Southern California, Northern Idaho, New Mexico, Nevada, Oregon, Washington
VAI Logic	www.vaitechnology.com	Indiana, Kentucky, Michigan, Ohio, Western Pennsylvania, West Virginia
EUROPE, MIDDLE EAST, & AFRICA (EMEA)		
eurotraining@xilinx.com		
Core Vision	www.core-vision.nl	The Netherlands, Belgium, Luxemburg
Doulos	www.doulos.com/xilinx	United Kingdom, Ireland
Inline Group	www.plis.ru	Moscow Region
Logtel Computer Communications	www.logtel.com	Israel, Turkey
Magnetic Digital Systems	www.magneticgroup.ru	Urals Region
Mindway	www.mindway-design.com	Italy
Multi Video Designs (MVD)	www.mvd-fpga.com	France, Spain, Portugal, Switzerland
Prevas	www.prevas.com/xilinx	Sweden, Norway, Denmark, Finland, Lithuania, Latvia, Estonia
Pulsar	www.pulsar.co.ua	Ukraine
Programmable Logic Competence Center (PLC2)	www.plc2.de	Germany, Switzerland, Poland, Hungary, Czech Republic, Slovakia, Slovenia, Greece, Cyprus, Turkey, Russia
SO-Logic Consulting	www.so-logic.co.at	Austria, Brazil, Czech Republic, Hungary, Slovakia, Slovenia
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Activemedia Innovation	www.activemedia.com.sg	Malaysia, Singapore, Thailand
Black Box Consulting	www.blackboxconsulting.com.au	Australia, New Zealand
E-elements	www.e-elements.com	China, Hong Kong, Taiwan
HKPC	www.hkpc.org	Hong Kong
Libertron	www.libertron.com	Korea
OE-Galaxy	www.oegalaxy.com.vn	Vietnam
Sandepani Programmable Solutions	www.sandepani-vlsi.com	India
SymmId	www.symmid.com	Malaysia
Ultrawise	ultrawise.com.cn	China
WeDu Solution	www.wedusolution.com	Korea
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Avnet Japan	www.jp.avnet.com	Japan
Fujitsu Electronics	jp.fujitsu.com/fei/services/maker/xilinx	Japan
Paltek	www.paltek.co.jp	Japan
Shinko Shoji	xilinx.shinko-sj.co.jp	Japan
Tokyo Electron Device	ppg.teldevice.co.jp	Japan

ADDITIONAL TRAINING RESOURCES

Curriculum Paths — Curriculum paths illustrate the recommended course sequence to follow based on your design specialization. Because Xilinx courses build on each other, you must meet the prerequisites to gain the full benefit of each course. Prerequisites are outlined in the course descriptions. **Test Your Knowledge** of the material covered in each course by selecting the appropriate link next to your course of interest.

www.xilinx.com/training/courses.htm

Recorded e-Learning — Recorded e-Learnings are currently available at no charge, over the Internet anytime, day or night, worldwide to allow you to get up to speed quickly. New topics each month, such as: Clocking Techniques, Timing Closure, DDR Memory Interface, FPGA vs. ASIC, etc.

www.xilinx.com/training/free-video-courses.htm

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