Synplify and Synplify Pro synthesis and Options

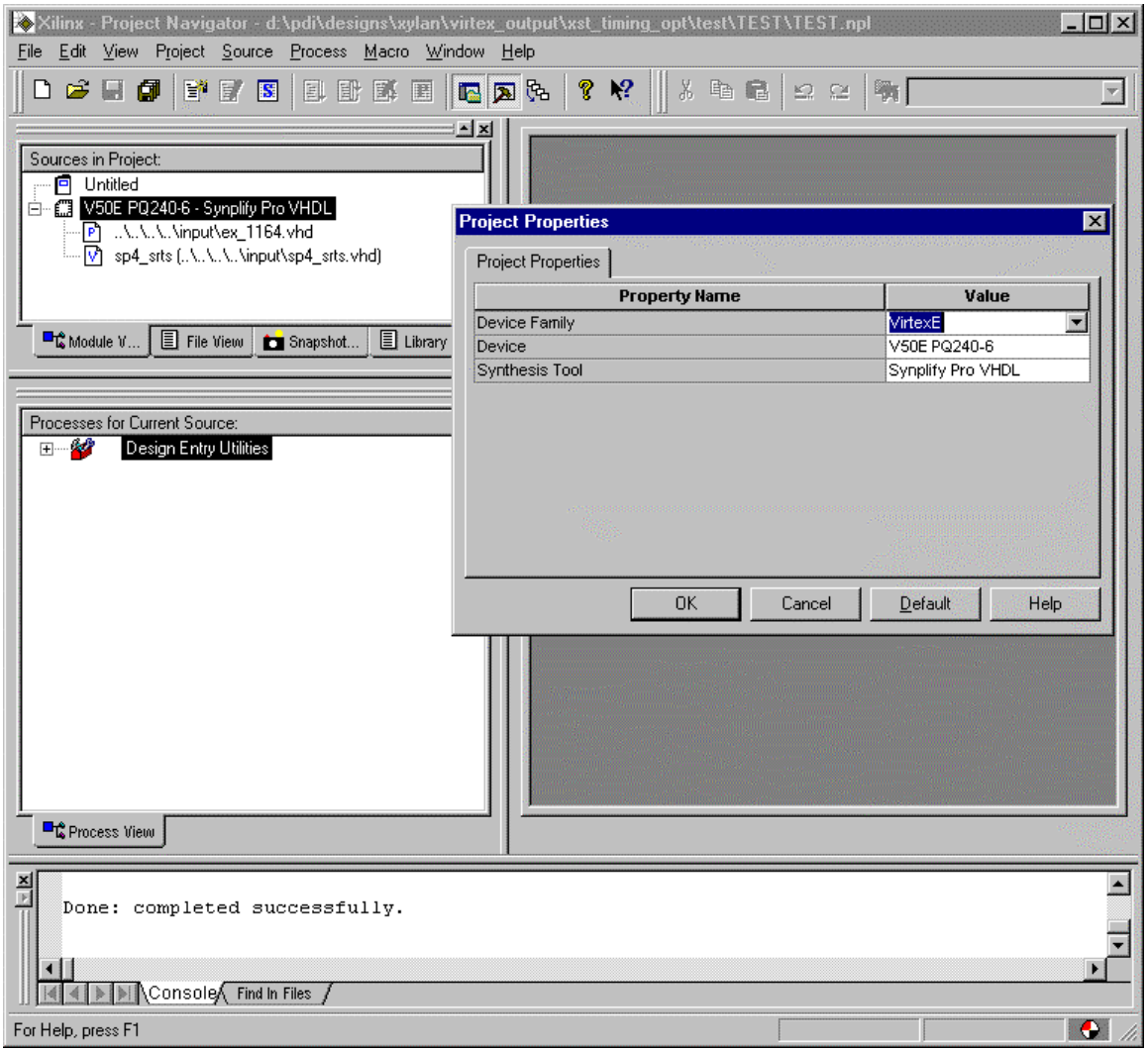
Synplify is a synthesis tool that can effectively synthesize VHDL, Verilog and Mixed language designs to create EDIF netlists. For detailed information about using Synplify tool to get best results, please refer to the Synplify and Synplify Pro user guide or Synplify On Line Help

ISE works with Synplify / Synplify Pro 6.1 and onward. When Synplify is installed, it sets proper values in the windows registry. ISE makes use of these values in the registry to invoke the latest version of Synplify. Also ISE needs Synplify to have a floating license in order to make use of Synplify's batch mode capability.

Following Xilinx device families are supported by Synplify and ISE package - Spartan, Spartan-II, SpartanXL, Virtex, Virtex-E, Virtex2, XC4000E, XC4000EX, XC4000L, XC4000XL, XC4000XLA

A. Setting Synplify/Synplify Pro as your synthesis tool

1. Create an ISE project using File->New menu button or open an existing ISE project.
2. Select your project in the source window of project navigator.
3. Right click and choose "Properties…" option to set Synplify/Synplify Pro as your synthesis tool.
4. Also choose the family and the device to be used for implementation in this option.

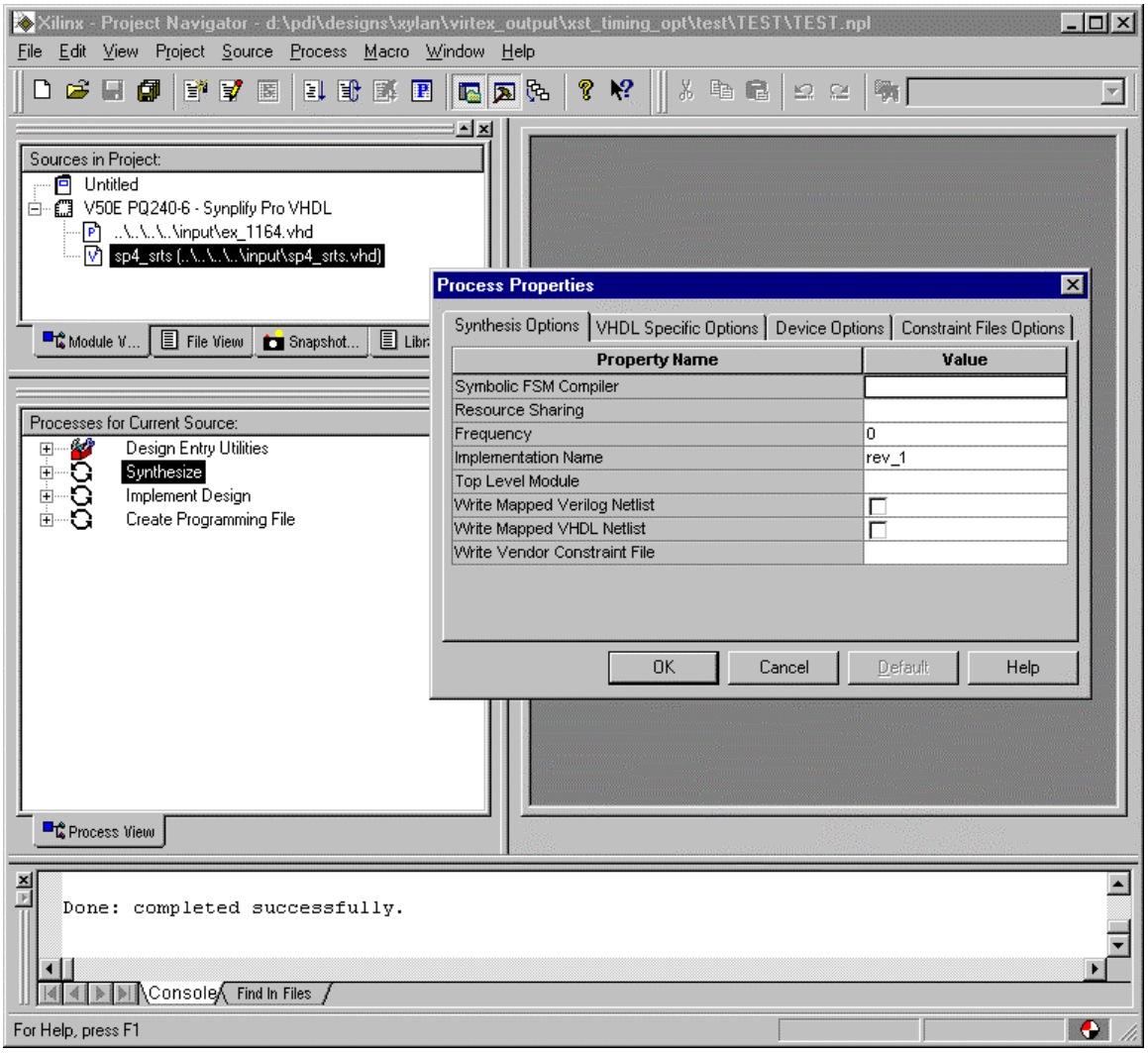


B. Setting Synplify and Synplify Pro options

Before you synthesize your design, you can set a variety of options for Synplify/Synplify Pro.

For complete description of these options, please refer to the design constraints section in the Synplify / Synplify Pro user guide or Synplify On Line Help.

1. Select your top-level design in the source window of project navigator.
2. To set the options, right click on "Synthesize" in the process window of Project Navigator.
3. Select "Properties…" to display synthesis options in the process properties dialog box.
4. Set the desired synthesis, VHDL specific, Device and Constraint file options.



Following is a list of options:

Synthesis Options

- Symbolic FSM compiler - Default value is ON.

The Symbolic FSM Compiler is an advanced state machine optimizer, which automatically recognizes state machines in your design and optimizes them. Unlike other synthesis tools that treat state machines as regular logic, the FSM Compiler extracts the state machines as symbolic graphs, and then optimizes them by re-encoding the state representations and generating a better logic optimization starting point for the state machines. The FSM Explorer uses the state machines extracted by the FSM Compiler when it explores different encoding styles.

- Resource sharing - Default value is ON.

Check the resource sharing option when you set implementation options. With this option checked, the software shares hardware resources like adders, multipliers, and counters wherever possible, and minimizes area.

- Frequency - Default value is 0 indicating area optimization.

For timing-driven synthesis, explicitly define the clock frequency. The software will use the global clock frequency for timing-driven synthesis.

- Implementation Name

An implementation is one version of a project, run with a certain set of options. You can synthesize again with another set of options to get another implementation. Synplify allows you to display multiple implementations in the same Project view.

- Top Level Module

This is the name of the top-level module being synthesized.

- Write Mapped Verilog Netlist - Default value is OFF.

Set this option to create a verilog netlist for the mapped design.

- Write Mapped VHDL Netlist - Default value is OFF.

Set this option to create a VHDL netlist for the mapped design.

- Write Vendor Constraint File - Default value is ON.

Synplify/Synplify Pro forward annotates user specified design constraints through a vendor constraint file. Set this option to enable/disable creation of this (NCF) file.

VHDL Specific Options

- Default Enum Encoding Goal - Default value is 'Default'.

You can set the default enumeration encoding. This is only for enumerated types; state-machine encoding is selected by the FSM compiler or specified using the syn_encoding attribute. Synplify selects the encoding style based on the number of values of the enumerated type. It can be onehot, gray or sequential encoding. Setting a value of 'default' for this option will enable Synplify to choose this automatically. Otherwise the specified value is used.

- Set Library

You can specify the VHDL library name. This command is used primarily for compatibility with VHDL simulators.

Device Options

- Modular flow (Synplify Pro Only) - Default value is OFF.

Synplify Pro supports the Xilinx modular design through different attributes. You can enable this capability by setting the "Modular flow" option.

- Use FSM Explorer data (Synplify Pro Only) - Default value is OFF.

Synplify Pro provides a powerful capability called FSM explorer. It explores various state encodings for the state machines in your design and then chooses the best encoding based on the design constraints. You can enable this capability by setting the "Use FSM explorer data" option.

- Pipelining (Synplify Pro Only) - Default value is OFF.

Synplify Pro can perform pipelining for multipliers and ROMs. It can move registers in to the logic for these blocks to reduce the critical path delay. This can improve results significantly for your designs.

- Disable I/O insertion - Default value is OFF.

You can enable/disable insertion of IO pads in your design through this option.

- Fanout Guide - Default value is 100.

You can specify a global fanout constraint on all the nets in your design. This is useful in keeping net fanout from becoming too large and causing any problems in the routing.

- Result File Name

You can specify the name of the file in which Synplify/Synplify Pro will write the design netlist to be used for implementation.

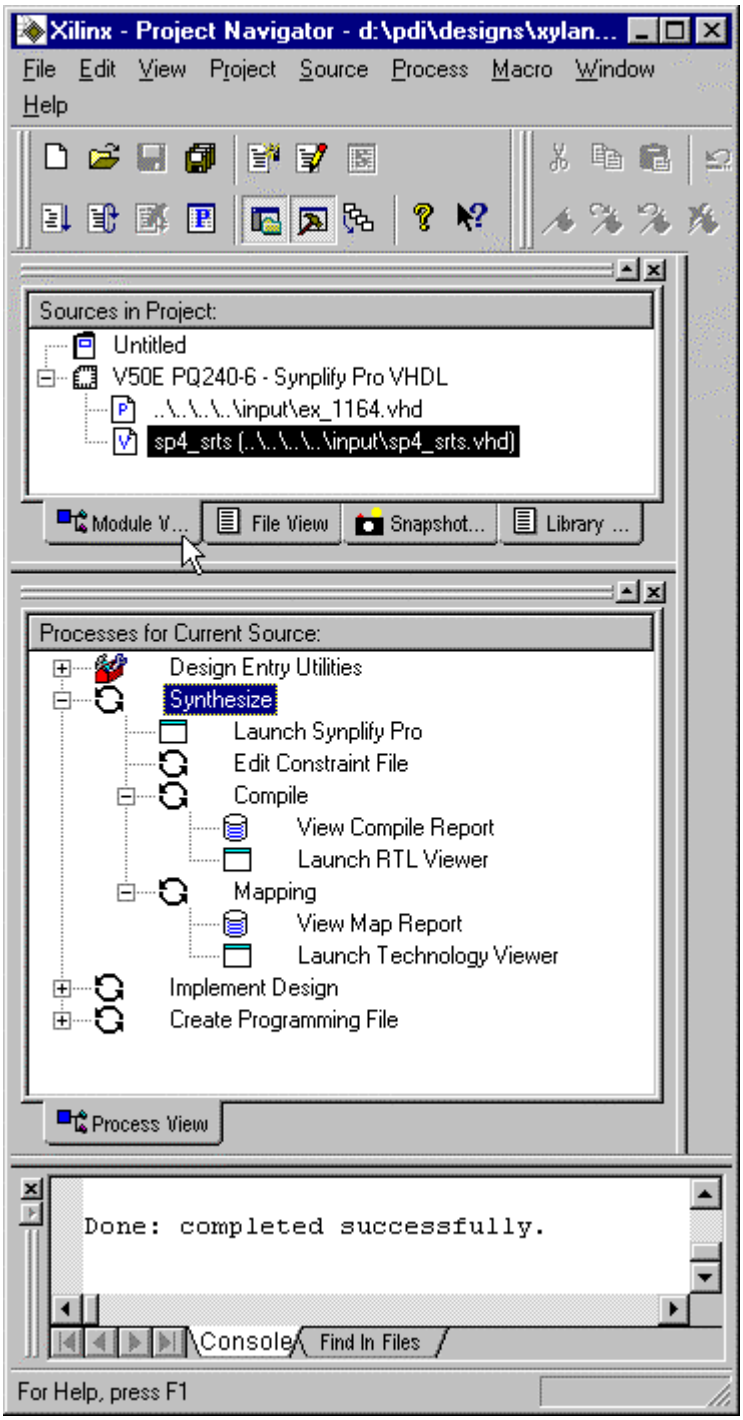
- Result Format - Default is edif.

You can specify the design netlist format. It can be either edif or xnf.

Constraint Files Options

- Constraints File Name

Synplify/Synplify Pro provides a very easy to use and powerful constraint editor. You can specify a constraint file name to be used for saving the design constraints. If a file with the specified name exists then it will be opened when 'Edit Constraints' option is chosen.



C. Editing a Constraint File

You can make use of powerful constraint editor (SCOPE) provided with Synplify/Synplify Pro to edit or add constraints for your design. Double click on "Edit Constraints…" option in the process window to bring up the Constraint Editor.

D. Synthesizing a Design

When a design is ready to synthesize, you can invoke Synplify or Synplify Pro within the Project Navigator by choosing "Launch Synplify" option under the Synthesis Folder.

To synthesize a design:

1. Select a source file in the source window.
2. Double click "Synthesize" in the process window.

E. Viewing a Schematic representation of your design

HDL Analyst is a high quality schematic viewer option provided with Synplify/Synplify Pro. You can view the RTL representation created after compilation and Technology representation created after mapping process using this. Double click on the "Launch RTL viewer" or "Launch Technology Viewer" options to achieve this.

F. Viewing a Synthesis Report

When synthesis is complete, you can view the results by double clicking "View Compile Report" or "View Map Report" in the Process window.

G. Known issues/problems

1. In Synplify's case view compile report and view rtl view both depends on the compile process. The same way view map report and view tech view depends on map process. Due to which when the compile/map process fails the user has to manually open the *.srr file outside of projnav.
2. The constraint file "module_name".sdc gets included if it is present in the project directory. This can sometimes make the frquency value specified in the properties section to be not used by Synplify.
3. Presently compile and mapping in the batch mode is not separate. So when the user tries to compile in Projnav, it goes through compile and mapping process. That is why when you try to run mapping, it finds all the files up-to-date and puts just the checkmark.