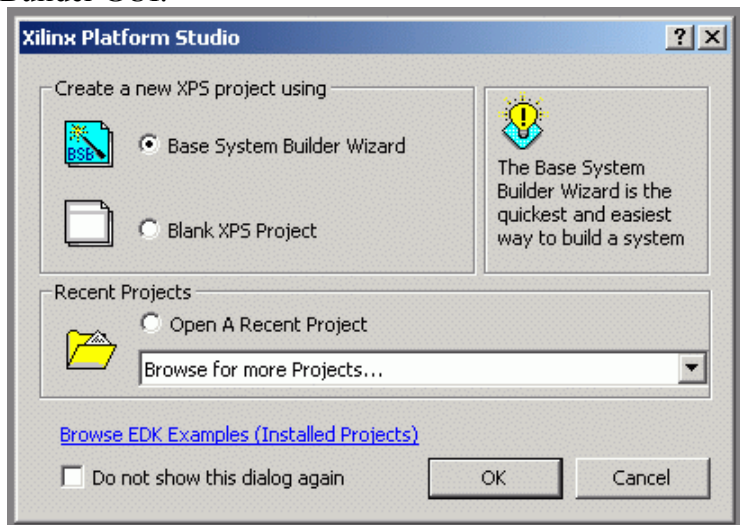


# Base System Builder support for the XUP Virtex-II Pro Development Board

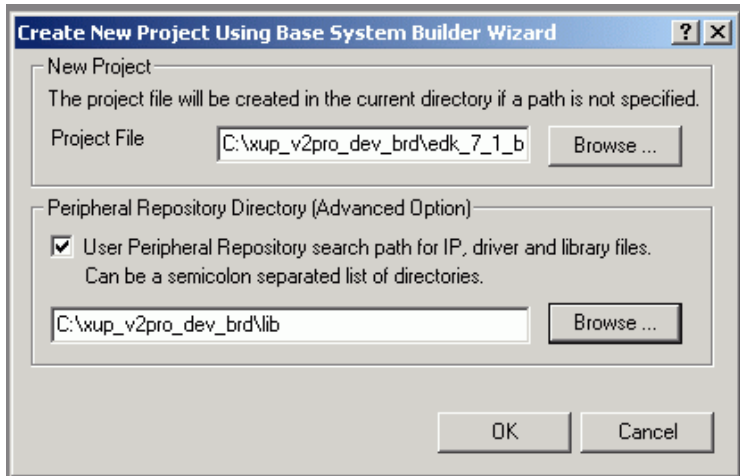
These reference designs are compatible with EDK 7.1 SP2 (or later) and ISE 7.1 SP3 (or later).

Xilinx Platform Studio Base System Builder uses a definition file that requires that you point to it along with several dedicated libraries specially created for the XUP Virtex-II Pro Development Board.

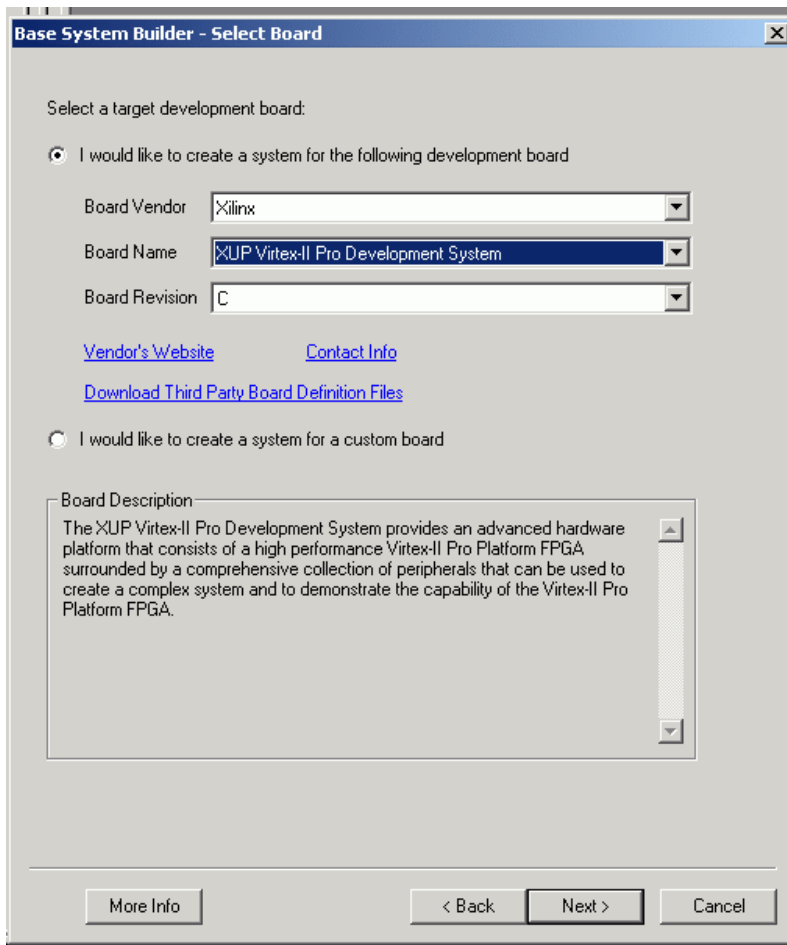
Start building your system in Xilinx Platform Studio by launching the Base System Builder GUI.



After selecting OK, the user needs to select the working directory and most importantly, the peripheral repository directory. This will add to the Base System Builder software the XUP Virtex-II Pro Development Board profile and supported peripherals, including the correct device I/O placement and timing settings.



Once this menu is correctly set, you will be able to select the XUP Virtex-II Pro Development Board profile.



Select next, then check the supported peripherals you want in you system.

# Base System Builder Limitations

There are a couple of limitations with the Xilinx Platform Studio, Base System Builder release 7.1 related to the support of DDR SDRAM DIMM memory and the VGA /TFT display interfaces provided in the release.

## IMPORTANT: DDR SDRAM DIMM Module Support

There are a few issues of related to complete support of the DDR DIMM memory module use with EDK.

Rev 1\_1 of the BSB support files automatically set the correct DDR DIMM DCM phase shift and correctly utilize 64 bit DIMMs.

Some DDR SDRAM DIMM memory modules utilize both sides of the PCB. These are considered “dual rank” modules. The dual rank modules can be supported with the DDR memory controller parameter defining multiple “banks”. The current released builder will automatically assign non-contiguous addressing for the two “banks” of memory. You can use the following settings for the 512MB dual rank memory module if you need contiguous memory to support Linux, for example.

```
PARAMETER C_NUM_BANKS_MEM = 2
PARAMETER C_MEM0_BASEADDR = 0x00000000
PARAMETER C_MEM0_HIGHADDR = 0x0ffffff
PARAMETER C_MEM1_BASEADDR = 0x10000000
PARAMETER C_MEM1_HIGHADDR = 0x1ffffff
```

## VGA/TFT Controller Support

The base system builder generator support for the VGA interface “plb\_tft\_cntlr\_ref” does not implement the DCR bus interface. The DCR bus interface allows the driver software to set the PLB bus display memory starting address from software control, as well as turning on and off the display blanking and direction of access of the display memory. The base system builder generated implantation will have the base address fixed and the display defaulted to the “ON” state.

The DCR control feature can be manually enabled by adding the necessary parameters to the system.mhs file. You can add the following parameters to the plb\_tft\_cntlr\_ref definition in the system.mhs file.

```
BUS_INTERFACE SDCR = dcr_v29_0
PARAMETER C_DCR_BASEADDR = 0b0000010000
PARAMETER C_DCR_HIGHADDR = 0b0000010001
```

The ‘Slideshow\_128MB’ reference project can be used as an example.

[Add link here](#)

