



XUPV5-LX110T GTP Aurora

Design Simulation and Synthesis

Using ISE 10.1i SP3

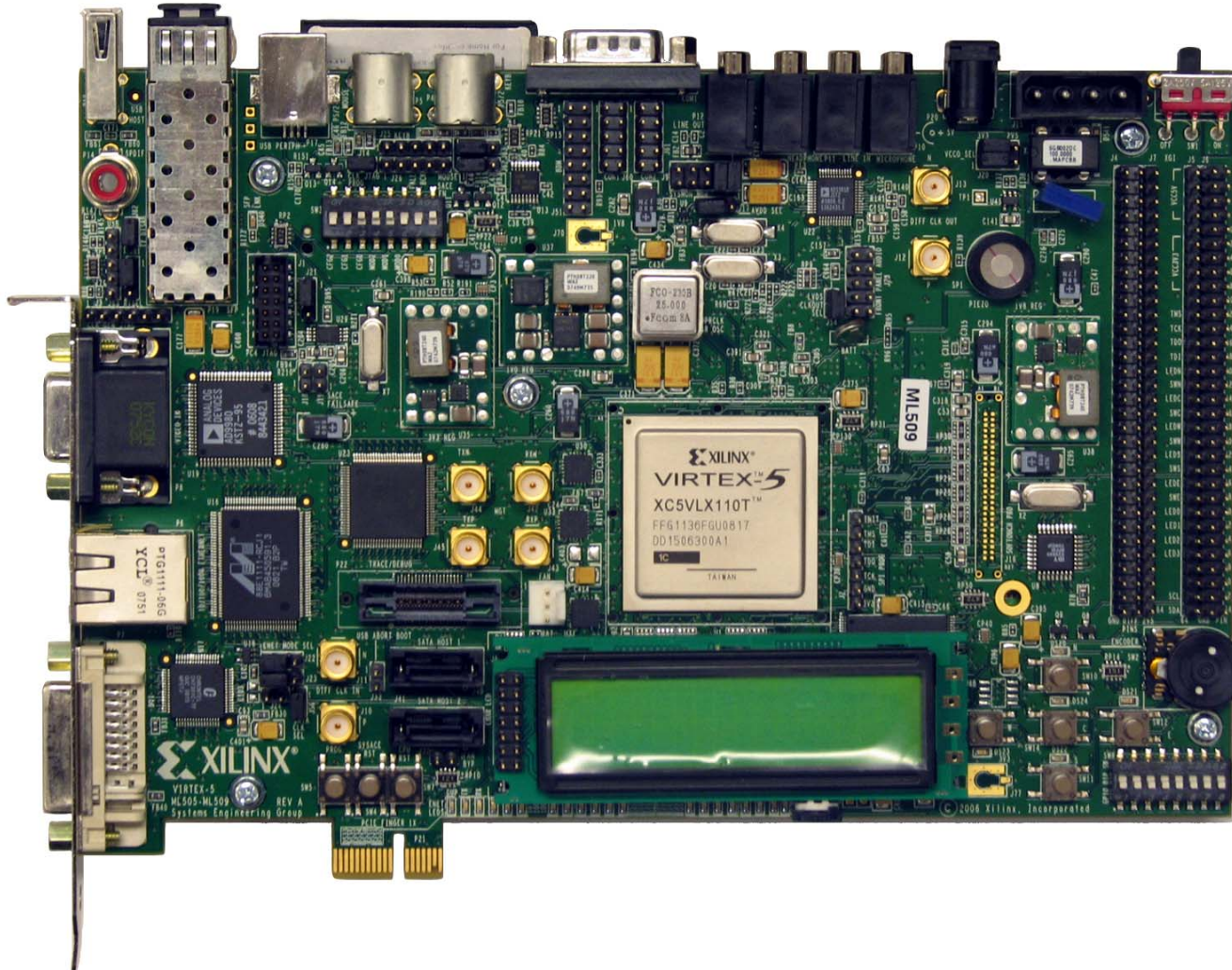


XUPV5-LX110T GTP Aurora Overview

- XUPV5-LX110T GTP Aurora reference design demonstrates the usage of a 2 byte, single lane aurora design interfaced with GTP transceiver. This reference design can be demonstrated on a XUPV5-LX110T board.
- This demo comprises of :
 - Hardware Setup
 - Design -Simulation and Synthesis
 - Testing the Design



XUPV5-LX110T Board



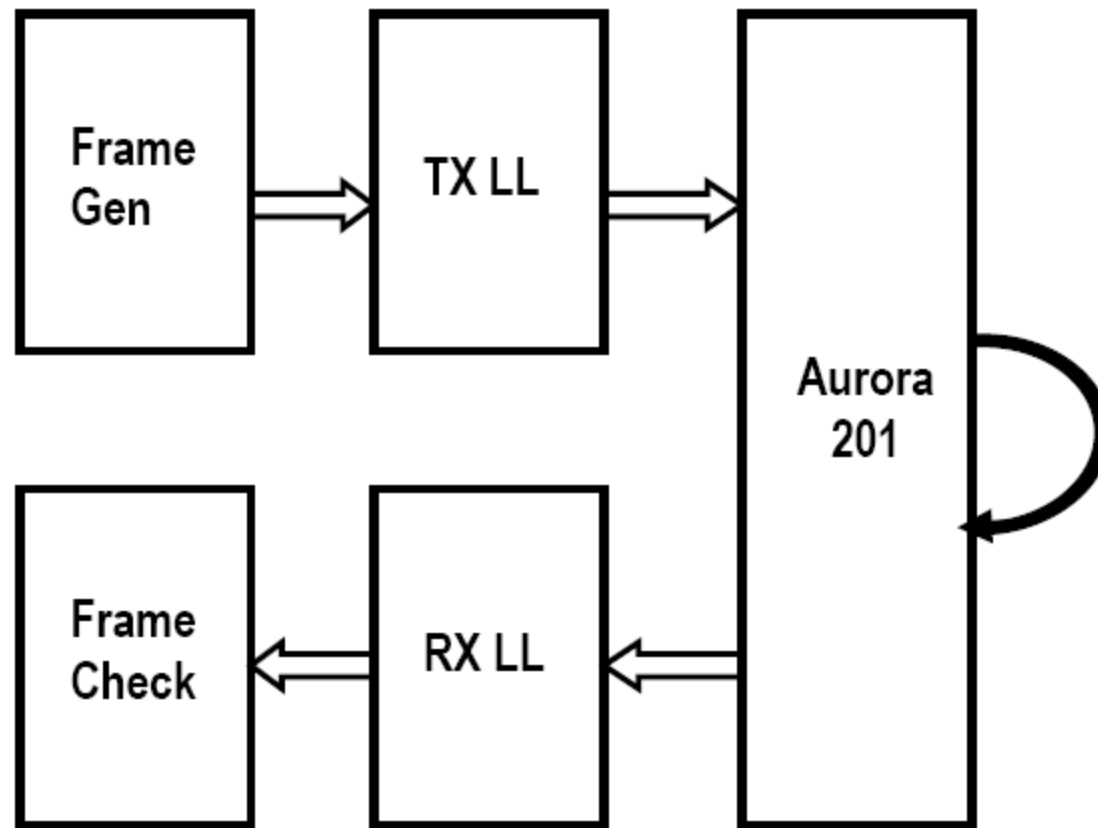
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Design Configuration

- Aurora 201 :
 - 16 bit Protocol Data Unit interface
 - Single lane
 - Consists of User flow control and Native flow control interfaces
 - UCF modified to suit XUPV5-LX110T board
 - Target device is Virtex-5 XC5VLX110T
 - Line rate is 3.125 Gbps & Reference Clock is 156.25 MHz
 - Note: If using CORE Generator for Aurora designs, an XUPV5-LX110T UCF must be added



Block diagram of Aurora Interface



Aurora 201-Example design

- The pre-built design is available in Verilog
- Unzip the xupv5-lx110t_aurora_sma.zip file to your project directory
- These files have been prepared for your convenience and it will add several required files and a pre-built design with a bitstream



Simulating the Example Design

- The design includes several scripts to assist the user in running the Xilinx ISE software.
- The GTP Aurora core provides a command line script to simulate the example design. To run the Verilog ModelSim simulation of the Aurora core, use the following instructions:
 1. For simulating the Verilog design, launch the ModelSim simulator and set the current directory to: <project directory>/xupv5-lx110t_aurora_sma
 2. Set the MTI_LIBS variable:

```
modelsim> setenv MTI_LIBS <path to compiled libraries>
```
 1. Launch the simulation script:

```
modelsim> do aurora.do
```



Simulating the Example Design

- The GTP Aurora core provides a quick way to simulate and observe the behavior of the core using the provided example design.
 - Prior to simulating the core, the functional (gate-level) simulation models must be generated.
 - You must compile all source files in the following directories to a single library as shown in table below:
 - Verilog → Library → <Xilinx dir>/verilog/src/unisims
<Xilinx dir>/smartmodel/<OS>/wrappers/mtiverilog



Simulating the Example Design

- The ModelSim script compiles the example design and testbench, and adds the relevant signals to the wave window.
- After the design is compiled and the wave window is displayed, run the simulation for about 20 μ s.
- The design is reset, followed by Aurora channel initialization and data transfer.
- Data transfer begins after the CHANNEL_UP signal goes high.
- The error_count should not increment for normal operation



Implementing the Verilog Design

- The design includes several scripts to assist the user in running the Xilinx ISE software.
- From the command prompt, navigate to the project directory and type the following:
 - For Windows:

```
ms-dos> cd xupv5-lx110t_aurora_sma/scripts  
ms-dos> xilperl make_aurora.pl -m -p -b -example
```
 - For UNIX:

```
unix-shell% cd xupv5-lx110t_aurora_sma/scripts  
unix-shell% xilperl make_aurora.pl -m -p -b -example
```
- These commands execute a script that synthesizes, builds, maps, place-and-routes the example design and produces a bitmap file. The resulting files are placed in the scripts directory.



Example Design Hierarchy

```
example_tb
|__ aurora_example
|   |__ aurora_201
|   |   |__ aurora_lane
|   |   |   |__ lane_init_sm
|   |   |   |__ chbond_count_dec
|   |   |   |__ sym_gen
|   |   |   |__ sym_dec
|   |   |   |__ error_detect
|   |   |__ phase_align
|   |   |__ global_logic
|   |   |   |__ channel_init_sm
|   |   |   |__ idle_and_ver_gen
|   |   |   |__ channel_error_detect
|   |   |__ tx_ll
|   |   |   |__ tx_ll_datapath
|   |   |   |__ tx_ll_control
|   |   |__ rx_ll
|   |   |   |__ rx_ll_nfc
|   |   |   |__ ufc_filter
|   |   |   |__ rx_ll_pdu_datapath
|   |   |   |__ rx_ll_ufc_datapath
|   |__ standard_cc_module
|   |__ frame_gen
|   |__ frame_check
```



Documentation

- GTP Aurora
 - LogiCORE GTP Aurora Getting Started Guide
 - http://www.xilinx.com/aurora/aurora_member/aurora_gs_ug223.pdf
 - LogiCORE GTP Aurora User Guide
 - http://www.xilinx.com/aurora/aurora_member/ug224.pdf
 - LogiCORE GTP Aurora Data Sheet
 - <http://www.xilinx.com/aurora/aurorads538.pdf>

