



XUPV5-LX110T SATA GTP IBERT Design Using 10.1i SP3 ChipScope™ Pro

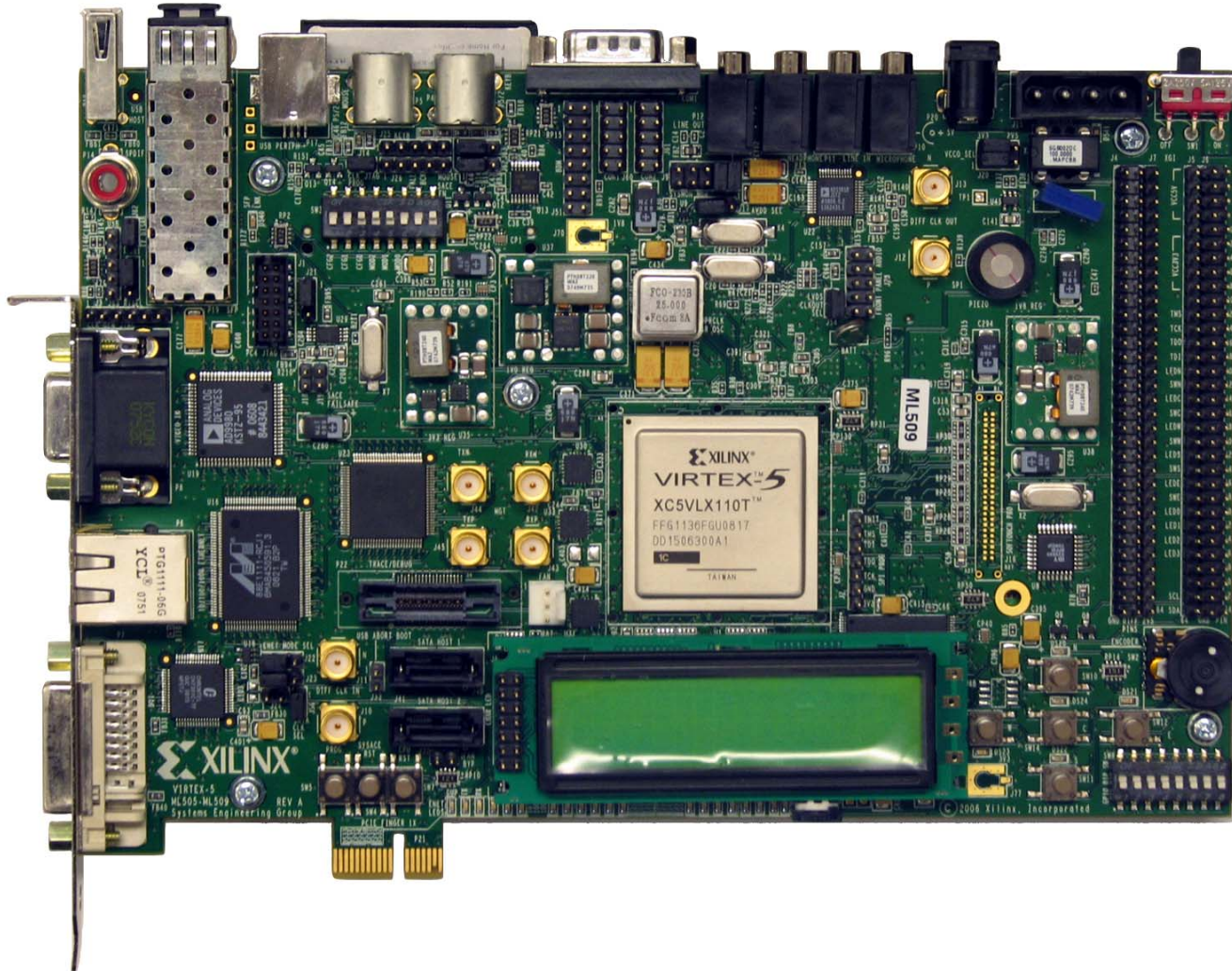


XUPV5-LX110T IBERT Overview

- Software Requirements
- Hardware Setup
 - SATA Loopback Cable (included in kit)
- ChipScope Setup
- Running IBERT
 - Highlighting the Virtex-5 RocketIO™ GTP Transceivers
- Design Creation



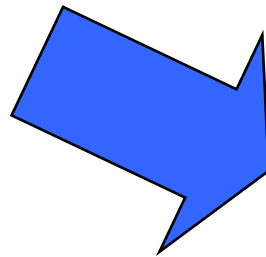
XUPV5-LX110T Board



XILINX

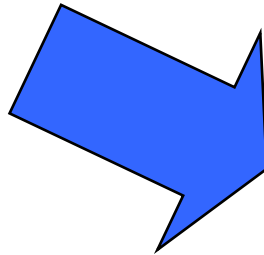
ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i SP3



ChipScope Pro Analyzer

Release Version: 10.1.03
Application Version: K.39 (Build 10103.8.234.834)
Copyright (c) 1995-2008 Xilinx, Inc.
All rights reserved.



Setting Up the Hardware

- Connect SATA “Crossover” Cable (included with XUPV5-LX110T kit)
 - Connect J40 to J41



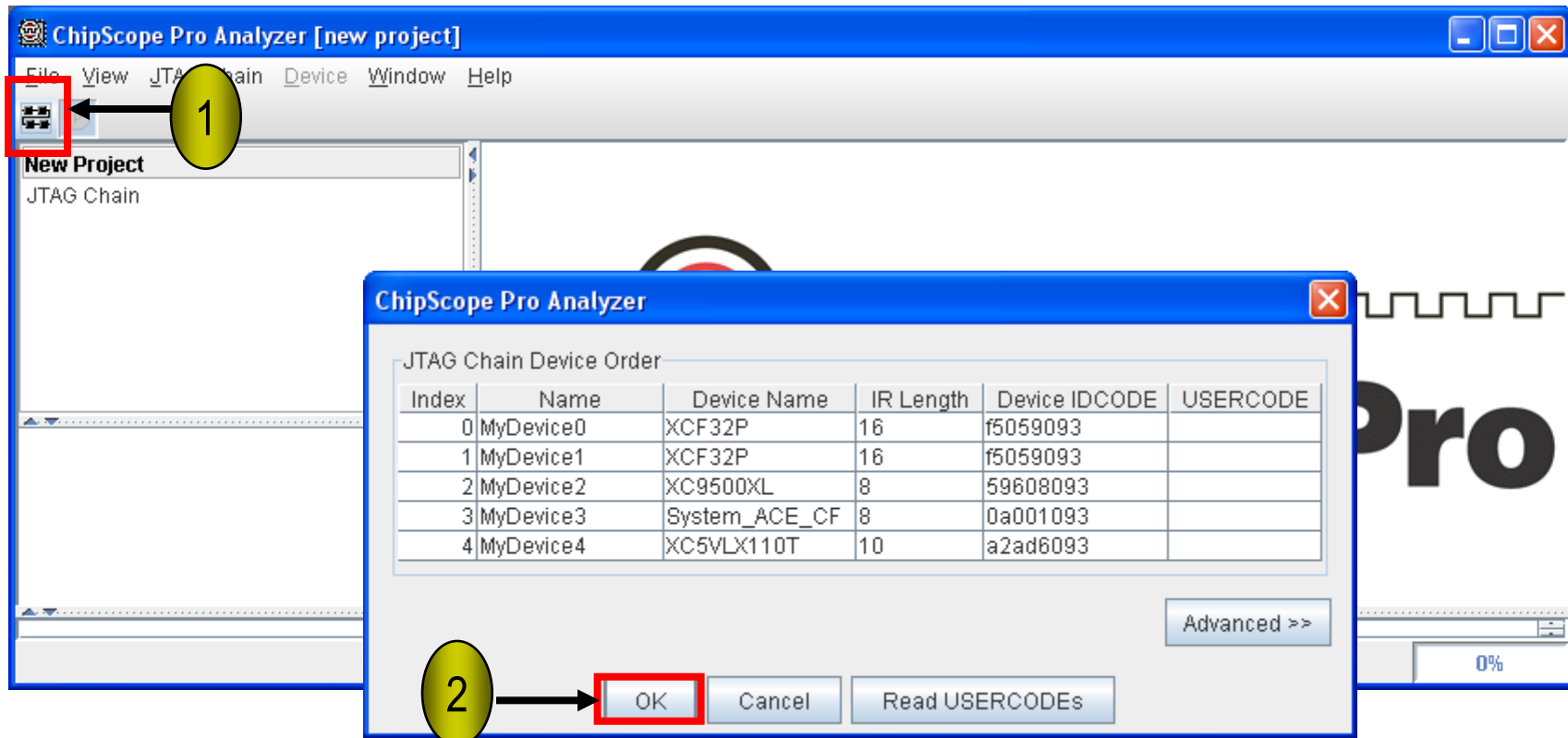
Setting Up the Hardware

- Connect SATA Frequency jumper J56
 - Provides 150 MHz clock source for MGT114 (X0Y3)
- See the User's Guide more details



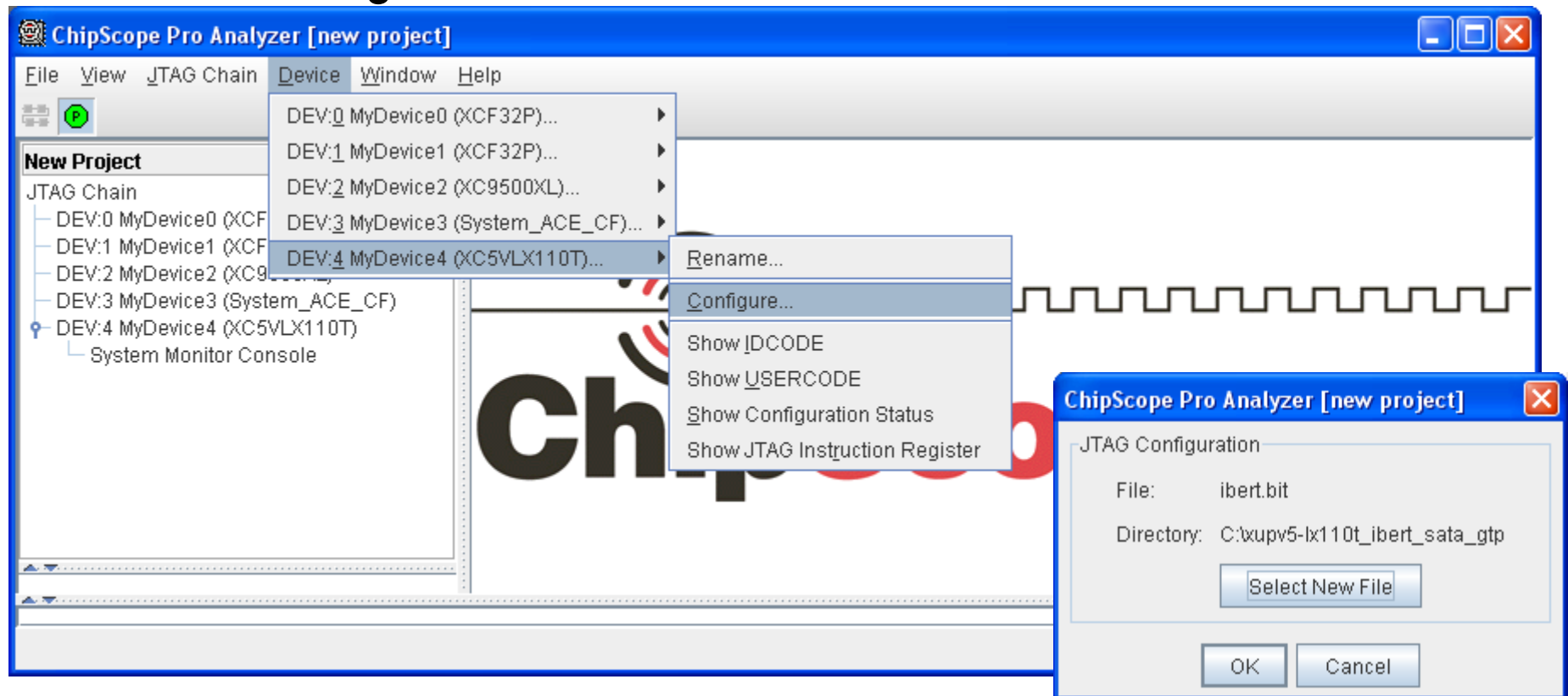
ChipScope Setup

- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



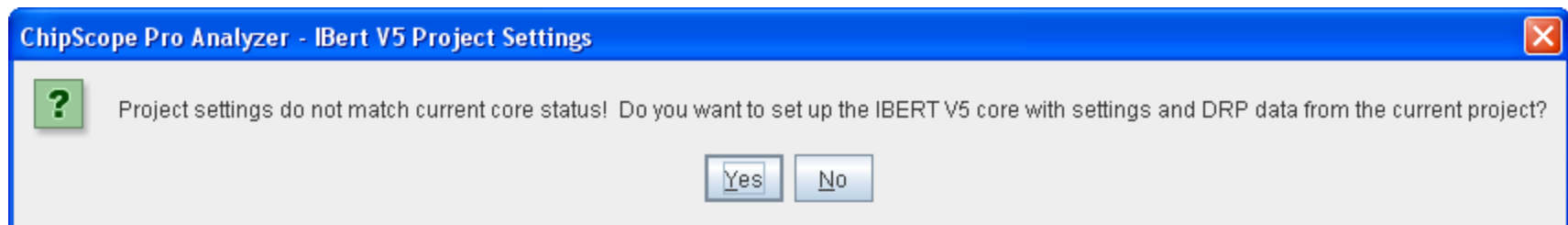
ChipScope Setup

- Select Device → DEV:4 MyDevice4 (XC5VLX110T) → Configure
- Select <Design Path>\ibert.bit



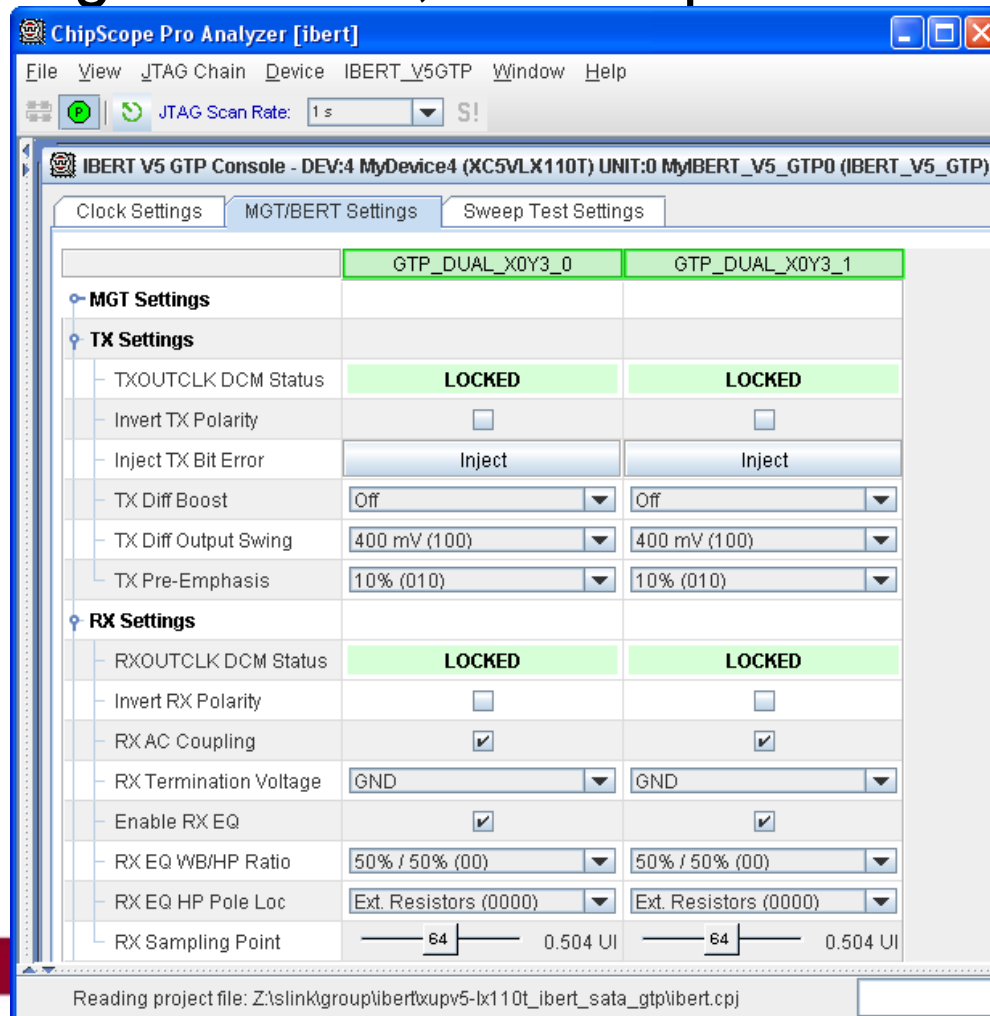
Running IBERT

- Select File → Open Project...
- Select <Design Path>\ibert.cpj
- Click Yes on this dialog box



IBERT ChipScope TX Settings

- Diff Swing = 400mV; Pre-emphasis = 10%



The screenshot displays the ChipScope Pro Analyzer interface for the IBERT V5 GTP Console. The window title is "ChipScope Pro Analyzer [ibert]". The main console area shows "IBERT V5 GTP Console - DEV:4 MyDevice4 (XC5VLX110T) UNIT:0 MyIBERT_V5_GTP0 (IBERT_V5_GTP)". The "MGT/BERT Settings" tab is selected, showing a table of settings for two GTP channels: GTP_DUAL_X0Y3_0 and GTP_DUAL_X0Y3_1.

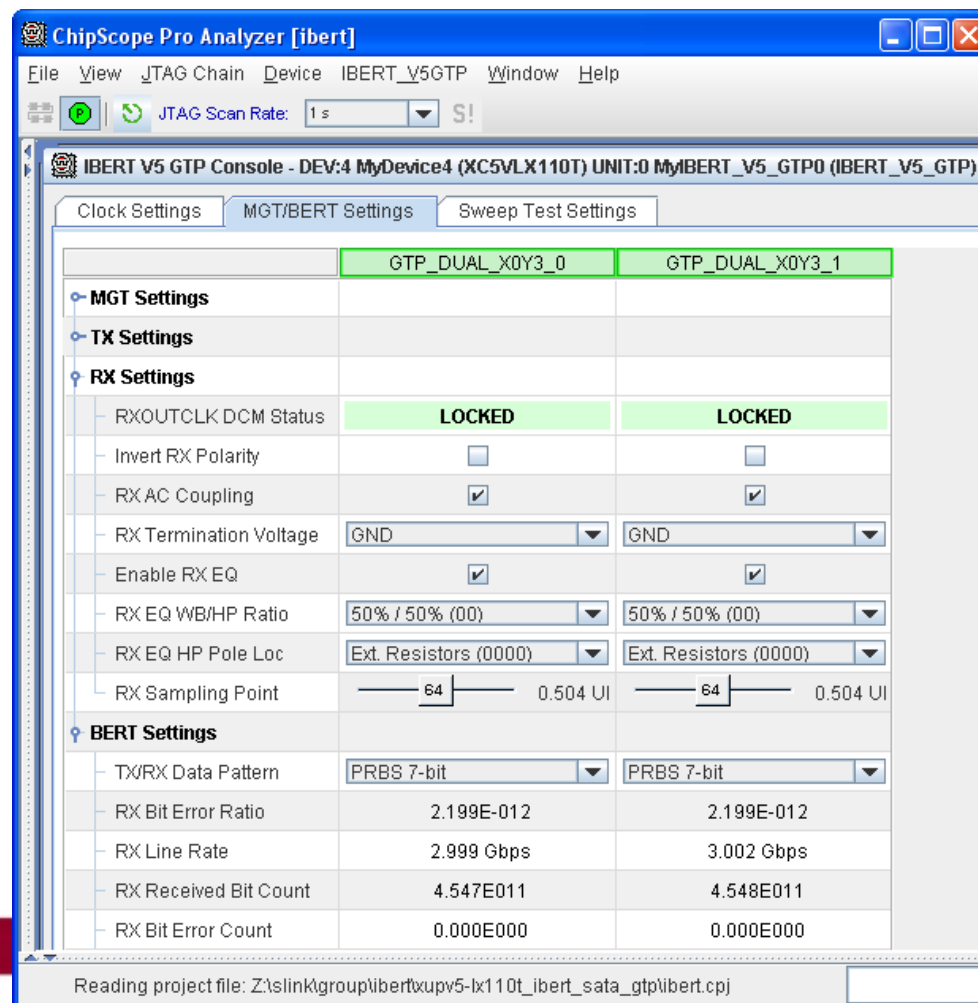
	GTP_DUAL_X0Y3_0	GTP_DUAL_X0Y3_1
MGT Settings		
TX Settings		
TXOUTCLK DCM Status	LOCKED	LOCKED
Invert TX Polarity	<input type="checkbox"/>	<input type="checkbox"/>
Inject TX Bit Error	Inject	Inject
TX Diff Boost	Off	Off
TX Diff Output Swing	400 mV (100)	400 mV (100)
TX Pre-Emphasis	10% (010)	10% (010)
RX Settings		
RXOUTCLK DCM Status	LOCKED	LOCKED
Invert RX Polarity	<input type="checkbox"/>	<input type="checkbox"/>
RX AC Coupling	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
RX Termination Voltage	GND	GND
Enable RX EQ	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
RX EQ WB/HP Ratio	50% / 50% (00)	50% / 50% (00)
RX EQ HP Pole Loc	Ext. Resistors (0000)	Ext. Resistors (0000)
RX Sampling Point	64 0.504 UI	64 0.504 UI

Reading project file: Z:\slink\group\ibert\txupv5-lx110t_ibert_sata_gtp\ibert.cpj



IBERT ChipScope RX Settings

- Enable RX EQ Checked



The screenshot shows the ChipScope Pro Analyzer interface for the IBERT V5 GTP Console. The 'RX Settings' section is expanded, showing configurations for two channels: GTP_DUAL_X0Y3_0 and GTP_DUAL_X0Y3_1. The 'Enable RX EQ' checkbox is checked for both channels.

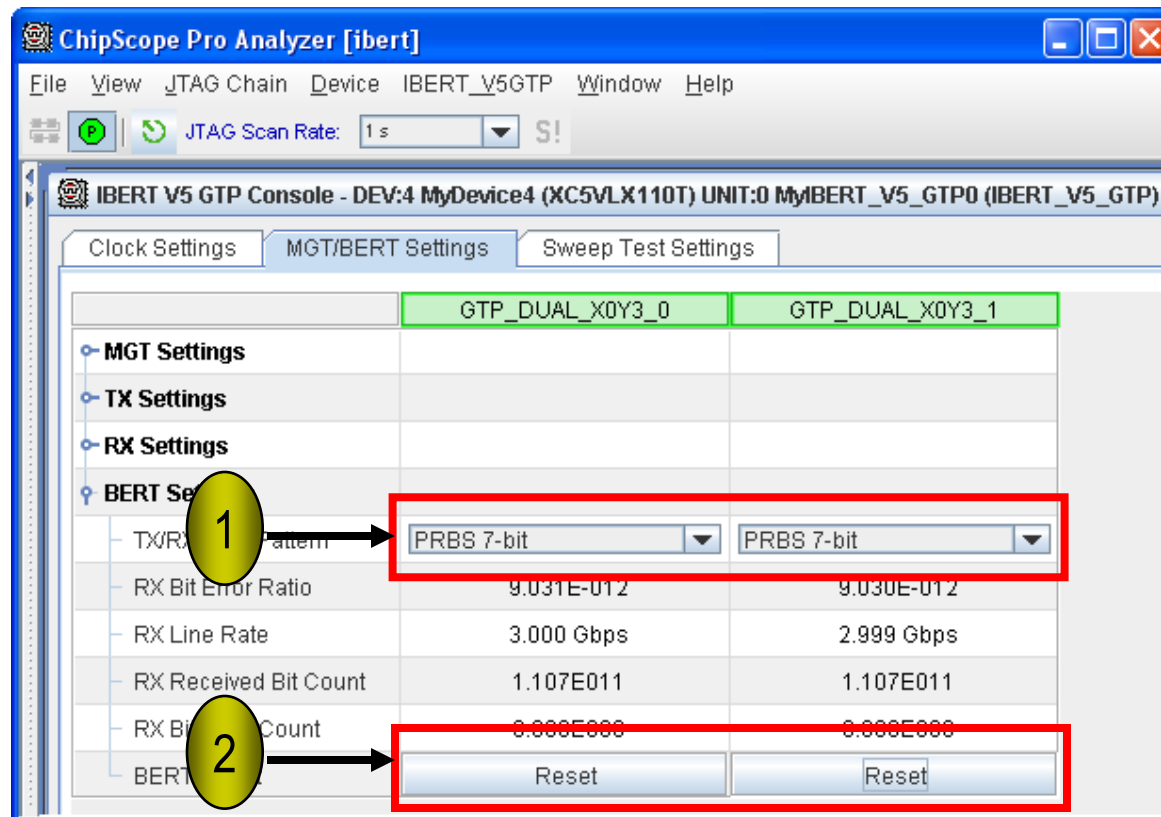
	GTP_DUAL_X0Y3_0	GTP_DUAL_X0Y3_1
MGT Settings		
TX Settings		
RX Settings		
- RXOUTCLK DCM Status	LOCKED	LOCKED
- Invert RX Polarity	<input type="checkbox"/>	<input type="checkbox"/>
- RX AC Coupling	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
- RX Termination Voltage	GND	GND
- Enable RX EQ	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
- RX EQ WB/HP Ratio	50% / 50% (00)	50% / 50% (00)
- RX EQ HP Pole Loc	Ext. Resistors (0000)	Ext. Resistors (0000)
- RX Sampling Point	64 0.504 UI	64 0.504 UI
BERT Settings		
- TX/RX Data Pattern	PRBS 7-bit	PRBS 7-bit
- RX Bit Error Ratio	2.199E-012	2.199E-012
- RX Line Rate	2.999 Gbps	3.002 Gbps
- RX Received Bit Count	4.547E011	4.548E011
- RX Bit Error Count	0.000E000	0.000E000

Reading project file: Z:\slink\group\ibertxupv5-lx110t_ibert_sata_gtp\ibert.cpj



IBERT ChipScope BERT Settings

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)



Running IBERT

- View the RX Line Rate (1) and the RX Bit Error Count (2)

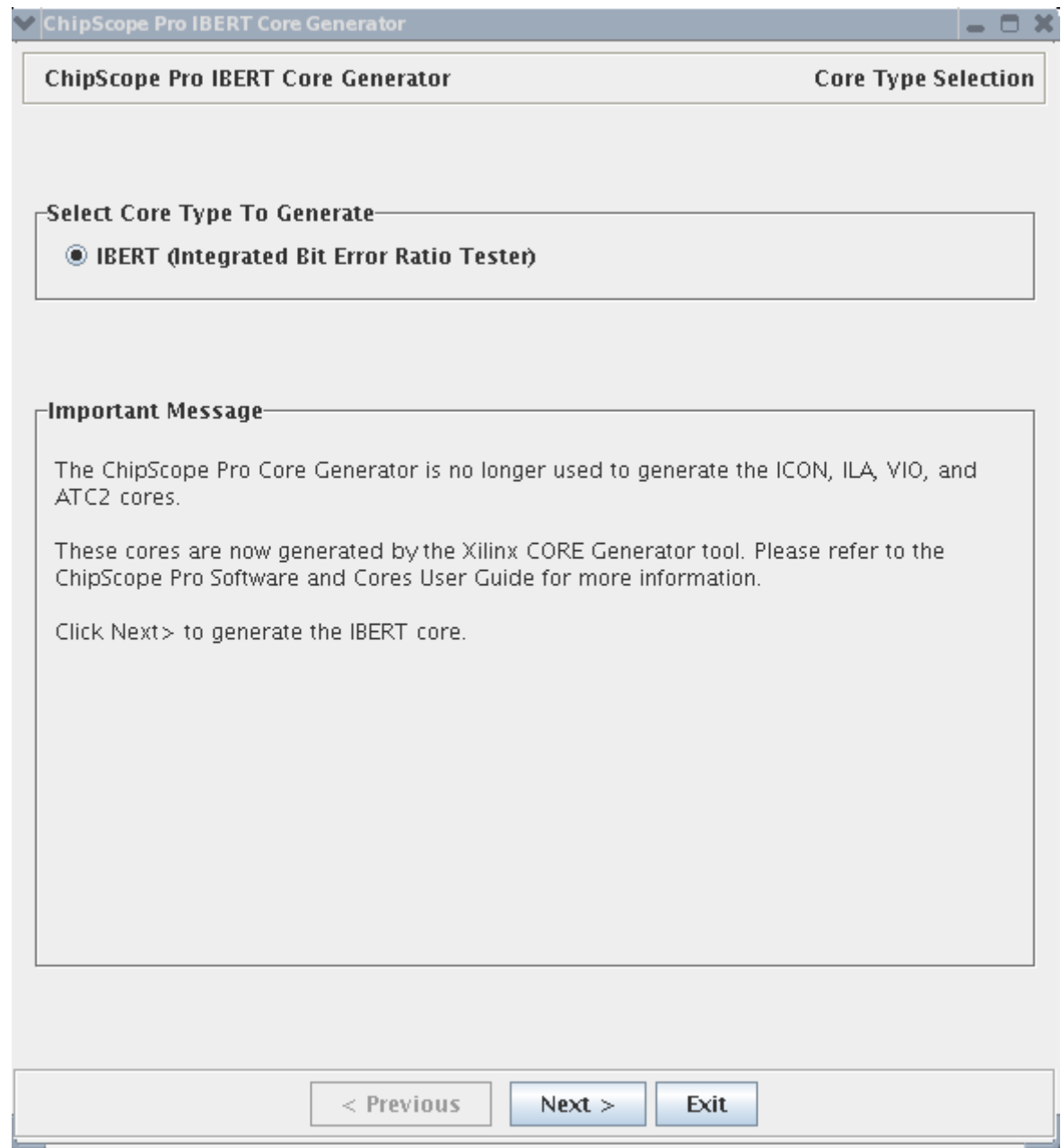
The screenshot shows the ChipScope Pro Analyzer interface for the IBERT V5 GTP Console. The console is configured for two GTP lanes: GTP_DUAL_X0Y3_0 and GTP_DUAL_X0Y3_1. The RX Settings are expanded, showing the RX Line Rate and RX Bit Error Count for both lanes. The RX Line Rate is 3.000 Gbps for lane 0 and 2.999 Gbps for lane 1. The RX Bit Error Count is 0.000E000 for both lanes. The RX Line Rate is labeled 1 and the RX Bit Error Count is labeled 2.

	GTP_DUAL_X0Y3_0	GTP_DUAL_X0Y3_1
TX/RX Data Pattern	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	9.031E-012	9.030E-012
RX Line Rate	3.000 Gbps	2.999 Gbps
RX Received Bit Count	1.107E011	1.107E011
RX Bit Error Count	0.000E000	0.000E000
BERT Test	Reset	Reset



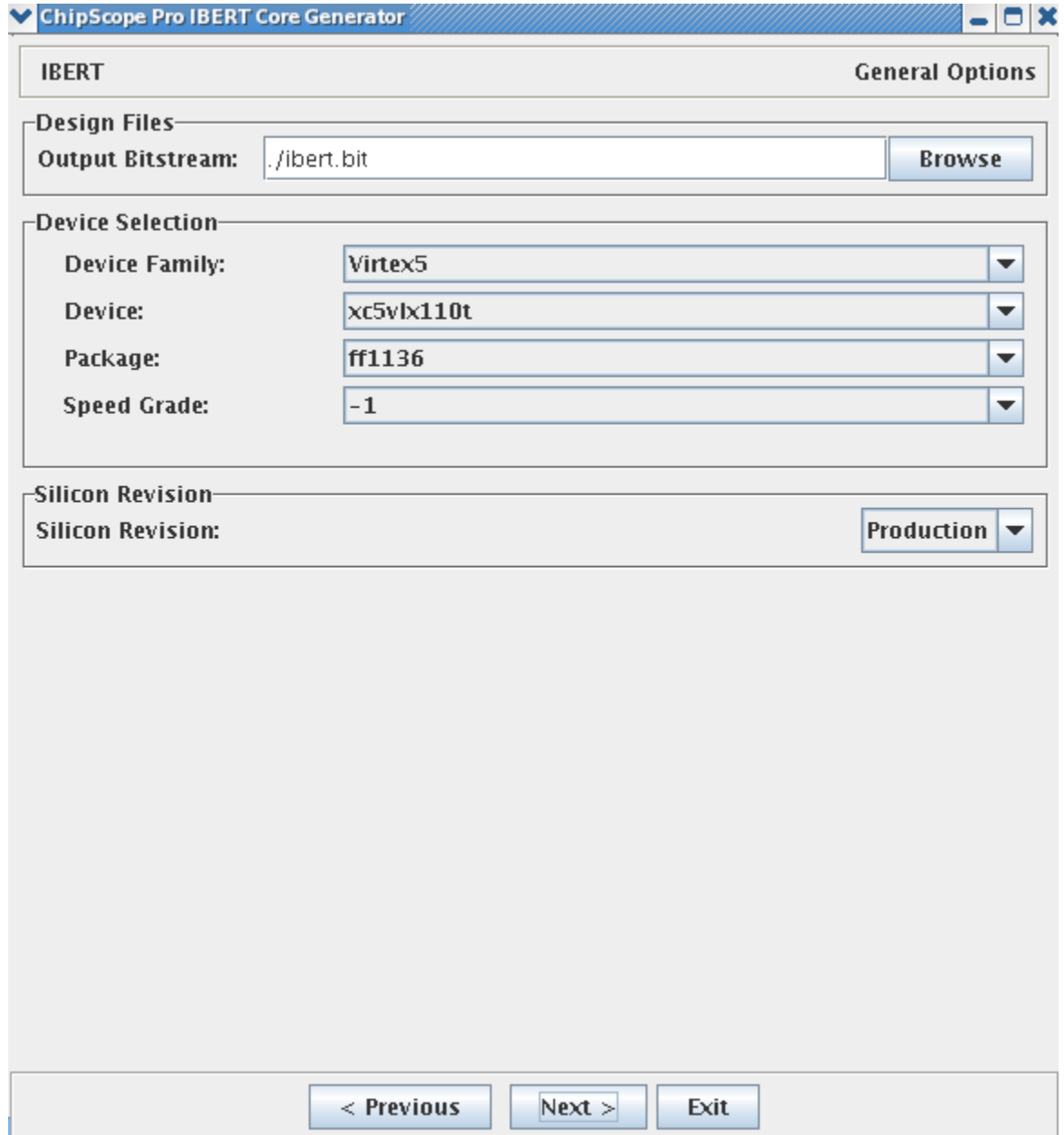
IBERT Generation

- Open the ChipScope Pro IBERT Core Generator



IBERT Generation

- Set the output to your design directory
- Make these settings:
 - Virtex5
 - xc5v1x110t
 - ff1136
 - -1



The screenshot shows the 'General Options' dialog box for the 'IBERT' core generator. The 'Design Files' section has 'Output Bitstream' set to './ibert.bit' with a 'Browse' button. The 'Device Selection' section has four dropdown menus: 'Device Family' (Virtex5), 'Device' (xc5v1x110t), 'Package' (ff1136), and 'Speed Grade' (-1). The 'Silicon Revision' section has a 'Silicon Revision' dropdown set to 'Production'. At the bottom are buttons for '< Previous', 'Next >', and 'Exit'.

Section	Field	Value
Design Files	Output Bitstream	./ibert.bit
	Device Selection	
Device Selection	Device Family	Virtex5
	Device	xc5v1x110t
	Package	ff1136
	Speed Grade	-1
Silicon Revision	Silicon Revision	Production



IBERT Generation

- System Clock Settings:
 - I/O Std: LVCMOS33
 - P Source Pin: AH15
 - Set Freq: 100

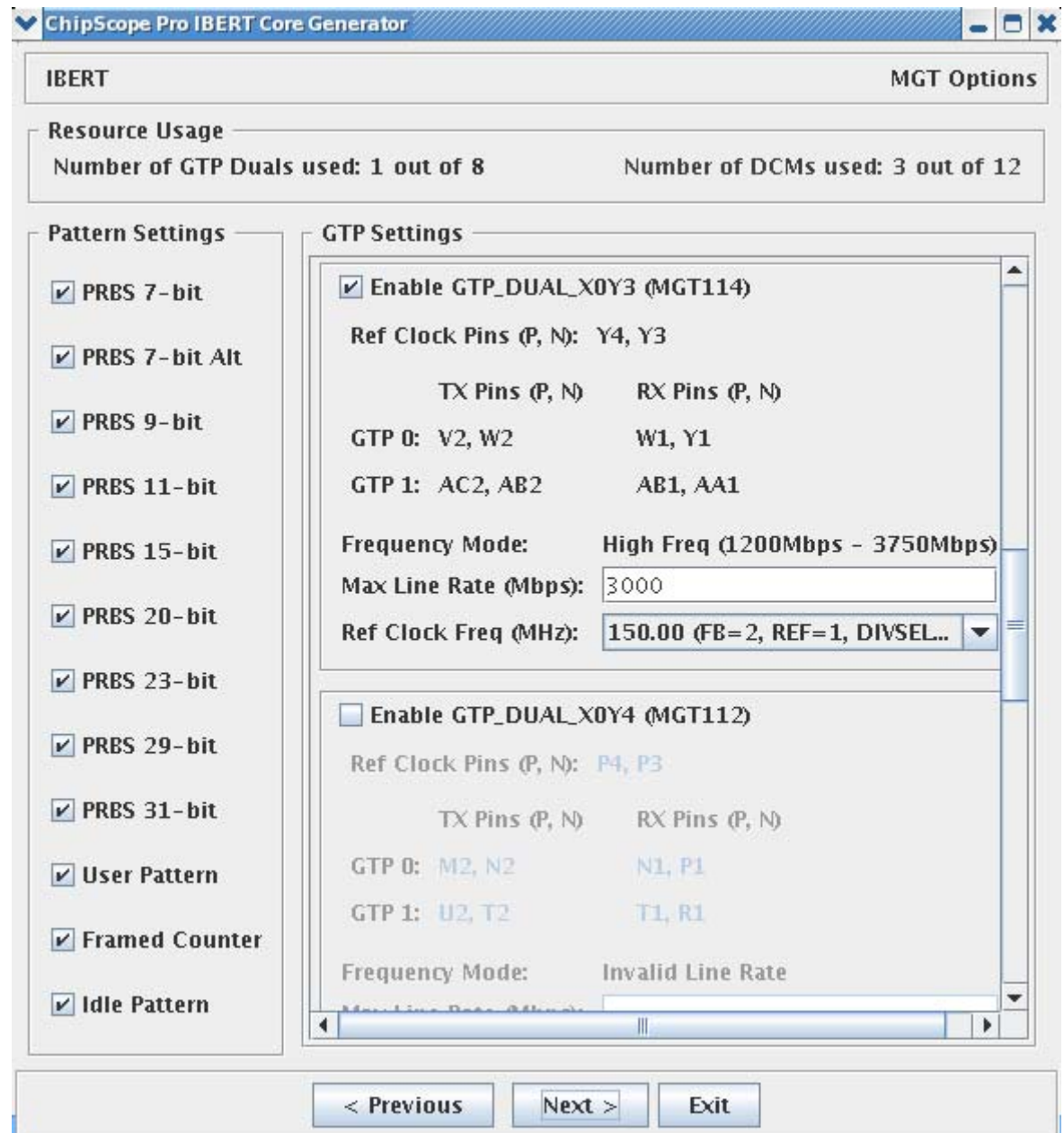


The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar reads 'ChipScope Pro IBERT Core Generator'. The window has a tab labeled 'IBERT' and a 'Clock Options' button in the top right corner. The main area is titled 'System Clock Settings' and contains three input fields: 'I/O Standard' is a dropdown menu set to 'LVCMOS33', 'P Source Pin' is a text box containing 'AH15', and 'Frequency (MHz)' is a text box containing '100'. At the bottom of the window, there are three buttons: '< Previous', 'Next >', and 'Exit'.



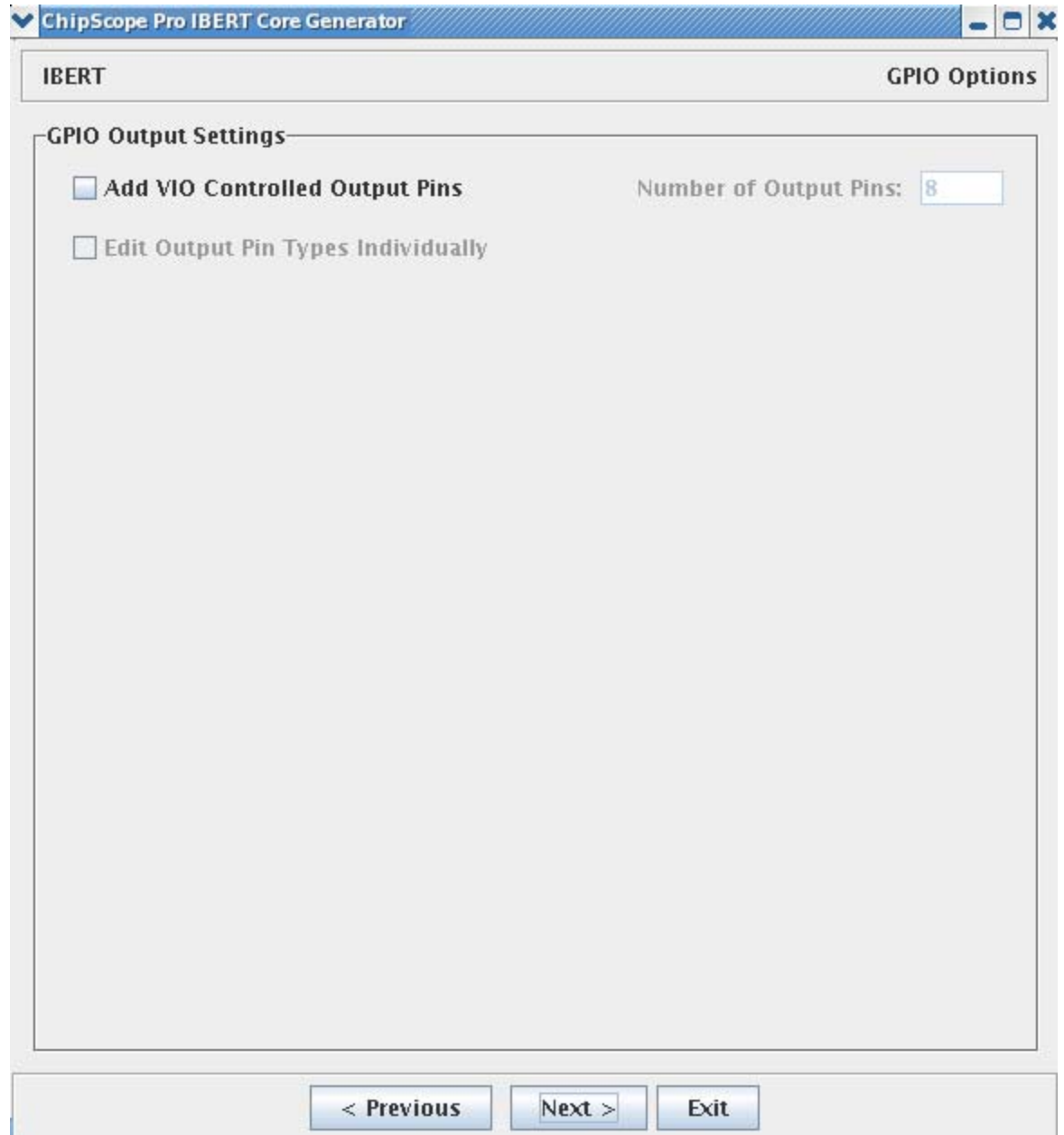
IBERT Generation

- Set the Pattern Settings as shown
- Select Enable GTP_DUAL_X0Y3
 - Set Max Line Rate to 3000
 - Set Ref Clock Frequency to 150



IBERT Generation

- Leave this screen as is



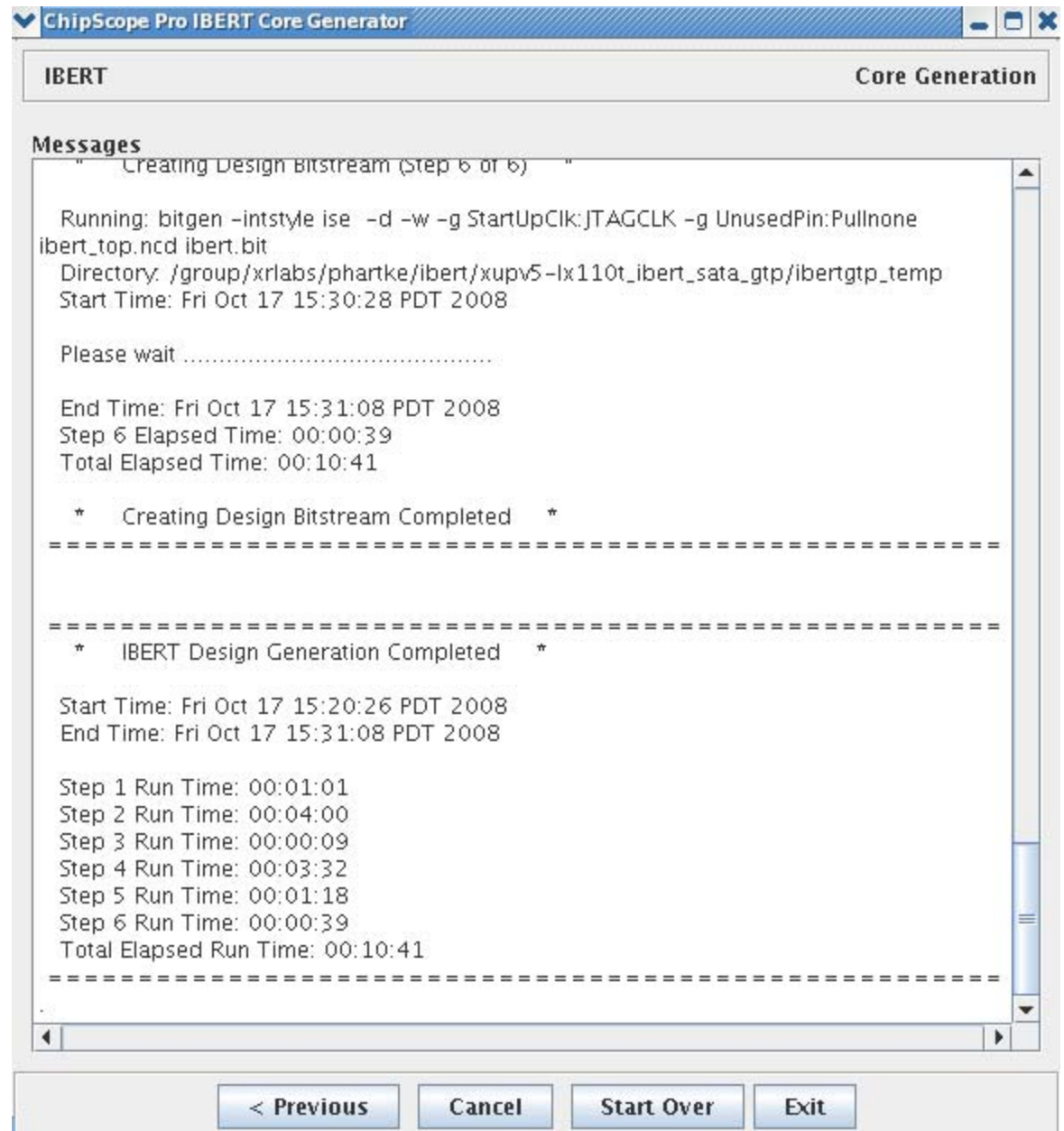
IBERT Generation

- Click Generate Design



IBERT Generation

- Bitstream is compiled and ready to use



The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar reads 'ChipScope Pro IBERT Core Generator'. The window has a header with 'IBERT' on the left and 'Core Generation' on the right. Below the header is a 'Messages' section containing the following text:

```
Creating Design Bitstream (Step 6 of 6)

Running: bitgen -intstyle ise -d -w -g StartUpClk:JTAGCLK -g UnusedPin:Pullnone
ibert_top.ncd ibert.bit
Directory: /group/xrlabs/phartke/ibert/xupv5-1x110t_ibert_sata_gtp/ibertgtp_temp
Start Time: Fri Oct 17 15:30:28 PDT 2008

Please wait .....

End Time: Fri Oct 17 15:31:08 PDT 2008
Step 6 Elapsed Time: 00:00:39
Total Elapsed Time: 00:10:41

* Creating Design Bitstream Completed *
```

Below this, there are two dashed lines, followed by another message:

```
* IBERT Design Generation Completed *
```

Start Time: Fri Oct 17 15:20:26 PDT 2008
End Time: Fri Oct 17 15:31:08 PDT 2008

```
Step 1 Run Time: 00:01:01
Step 2 Run Time: 00:04:00
Step 3 Run Time: 00:00:09
Step 4 Run Time: 00:03:32
Step 5 Run Time: 00:01:18
Step 6 Run Time: 00:00:39
Total Elapsed Run Time: 00:10:41
```

At the bottom of the window, there are four buttons: '< Previous', 'Cancel', 'Start Over', and 'Exit'.

