

A Anacom e a UNISINOS convidam para participar do Workshop do Programa Universitário Xilinx

FPGA Design Flow Workshop

Data: 19-20 Março 2012

Local: Campus UNISINOS Bento Goncalves (RS)



Course Description	This course provides professors with an introduction to designing with Xilinx FPGAs using ISE® Foundation™ software.
Level	Introduction
Training Duration	2 days
Who Should Attend	Professors who are new to FPGAs or Xilinx technology and wish to use Xilinx FPGAs in digital design.
Prerequisites	Digital design experience Basic HDL knowledge (VHDL or Verilog) Basic understanding of C programming

**Inscrição
Gratuita!**

Course Overview

Day 1

Basic FPGA Architecture

Lab 1: Xilinx Tool Flow

An introduction to FPGA design flow. Open a project containing the PicoBlaze 8-bit microcontroller and simulate the design using the ISim HDL simulator provided with the ISE Foundation Software.

Lab 2: Architecture Wizard and Pinout and Area Constraints Editor (PACE)

Use the Architecture Wizard to configure and instantiate a DCM into a PicoBlaze design. Assign pin locations with PACE. Implement design to generate a bitstream file. Download and test in hardware using hyperterminal.

Lab 3: Global Timing Constraints

Enter and analyze the effects of global timing constraints on a simple PicoBlaze design. Download and test the design in hardware using hyperterminal.

Day 2

FPGA Design Techniques

Synchronous Design Techniques

Lab 4: Synthesis Techniques with Xilinx Synthesis Technology (XST)

Set various synthesis options to improve results for a simple PicoBlaze design. Download the design and test in hardware using hyperterminal.

Implementation Options

Lab 5: CORE Generator Software

Generate the instruction ROM for a PicoBlaze design using CORE Generator, initialized with instructions generated from the PicoBlaze assembler. Download and test in hardware.

Lab 6: ChipScope Pro Tool

Use the ChipScope Pro tool to debug a simple PicoBlaze design using an Integrated Logic Analyzer (ILA) core.

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