**SKIP CALIBRATION and RELOAD TAP VALUES**

To reduce the time it takes for memory interfaces to complete calibration and resume normal operation, a proposed option is to perform full calibration in the factory and store the calibration tap values.

In the field this board can skip calibration and simply reload these calibration tap values, thereby reducing calibration time.

The required stages of calibration in the skip calibration mode are as follows:

Figure 1 shows the flow diagram of the skip calibration sequence.

- Memory Initialization
- Phaser_In Phaselocked
- Phaser_In DQSFOUND
- Load Phaser_In and Phaser_Out calibration tap values
- Sanity Check
- Temperature Monitor adjustments

Please refer to (UG 586) for details on Memory Initialization, Phaser_In Phaselocked, Phaser_In DQSFOUND, and sanity check stages of calibration.

Temperature monitor adjustments are required because calibration can be performed at a different temperature from when the calibration tap values are loaded in the field.

The user interface to recover the stored calibration tap values comprises a 7-bit address bus, an 8-bit data bus, and a few control signals. The SKIP_CALIB parameter when set to “TRUE” will put the MIG design in the skip calibration mode. Figure 2 shows the user interface signals required during skip calibration to retrieve the stored tap values.

The timing waveform for these user interface signals is shown in figure 3.

MIG calibration logic will assert ‘calib_tap_req’ indicating that it is ready to accept the stored calibration tap values. The user will assert ‘calib_tap_load’ to validate the contents of the ‘calib_tap_val’ and the ‘calib_tap_addr’ buses.

When all of the tap values have been sent, the user will assert the ‘calib_tap_load_done’ signal.

Table 1 shows the address mapping for the different calibration tap values per byte. In order to store the calibration tap values, the following debug signals in ILA need to be stored after init_calib_complete is asserted with SKIP_CALIB=“FALSE”.

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1. Use `dbg_prbs_final_dqs_tap_cnt_r` if PRBS read level is enabled \((nCK\_PER\_CLK == 4) \&\& (BYPASS\_COMPLEX\_RDLVL=="FALSE")) otherwise use `dbg_cpt_tap_cnt` and store as Phaser_in stage 2 taps. The debug bus `dbg_prbs_final_dqs_tap_cnt_r[5:0]` is the Phaser_in Stage2 calibration tap value for byte 0, `dbg_prbs_final_dqs_tap_cnt_r[11:6]` is the Phaser_in Stage2 calibration tap value for byte 1 and so on. Similarly if PRBS read level is disabled `dbg_cpt_tap_cnt[5:0]` is the Phaser_in Stage2 calibration tap value for byte 0 and so on.

2. Use `dbg_dq_idelay_tap_cnt` bus and store as Idelay taps. The debug bus `dbg_dq_idelay_tap_cnt[4:0]` is the Idelay calibration tap value for byte 0, `dbg_dq_idelay_tap_cnt[9:5]` is the Idelay calibration tap value for byte 1 and so on.

3. Use `dbg_phy_oclkdelay_cal_taps` and store as Phaser_Out Stage3 taps. The debug bus `dbg_phy_oclkdelay_cal_taps[5:0]` is the Phaser_Out Stage3 calibration tap value for byte 0, `dbg_phy_oclkdelay_cal_taps[11:6]` is the Phaser_Out Stage3 calibration tap value for byte 1 and so on.

4. Use `dbg_phy_wrlvl_128_75` and store as Phaser_Out Stage2 taps. The debug bus `dbg_phy_wrlvl_128_75[5:0]` is the Phaser_Out Stage2 calibration tap value for byte 0, `dbg_phy_wrlvl_128_75[11:6]` is the Phaser_Out Stage2 calibration tap value for byte 1 and so on.

5. Use `dbg_phy_wrlvl_155_129` and store as Phaser_Out Coarse taps. The debug bus `dbg_phy_wrlvl_155_129[2:0]` is the Phaser_Out Coarse calibration tap value for byte 0, `dbg_phy_wrlvl_155_129[5:3]` is the Phaser_Out Coarse calibration tap value for byte 1 and so on.

6. Store `device_temp[11:0]` from `mig_7series_0_mig.v` (top level MIG file). Since this is a 12-bit value it has to be sent over two cycles and uses two addresses as listed in Table 1. If the parameter `TEMP_MON_EN = “OFF”`, the `device_temp[11:0]` must be set to `11’h0` when loading the temperature value.
Figure 1: Skip Calibration Sequence

- System Reset
- DDR2/DDR3 SDRAM Initialization
- Phaser_IN Phase Lock (Phase locks Read DQS to internal, free-running Frequency Reference clock)
- Phaser_In DQSFOUND calibration
- Phaser_Out, Phaser_In, IDELAY inc/dec
- Sanity Check
- Temp monitor adjustments
- PHY Initialization and Calibration Complete

Figure 2: Skip Calibration User Interface signals

- calib_tap_load
- calib_tap_addr (7-bit)
- calib_tap_val (8-bit)
- calib_tap_load_done
- mig_top
- calib_tap_req

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Figure 3: Skip Calibration User Interface Signal Timing

Table 1: Address map for a 7 Series 32-bit interface

<table>
<thead>
<tr>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>DQS count or Byte count</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>calibration tap address</th>
<th>7 series Calibration Tap Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Phaser_Out Coarse</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Phaser_Out Stage3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Phaser_Out Stage2</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>0</td>
<td>Idelay</td>
<td></td>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Phaser_Out Coarse</td>
<td></td>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Phaser_Out Stage3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Phaser_In Stage2</td>
<td></td>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>Idelay</td>
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<td>0</td>
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<td>1</td>
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<td>0</td>
<td>Phaser_Out Coarse</td>
<td></td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>Phaser_Out Stage3</td>
<td></td>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Phaser_In Stage2</td>
<td></td>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Idelay</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>device temp [11:8]</th>
<th>device temp [7:0]</th>
</tr>
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<tbody>
<tr>
<td>1 1 1 1 1 1 1 1 0</td>
<td>1 1 1 1 1 1 1 1 0</td>
</tr>
</tbody>
</table>