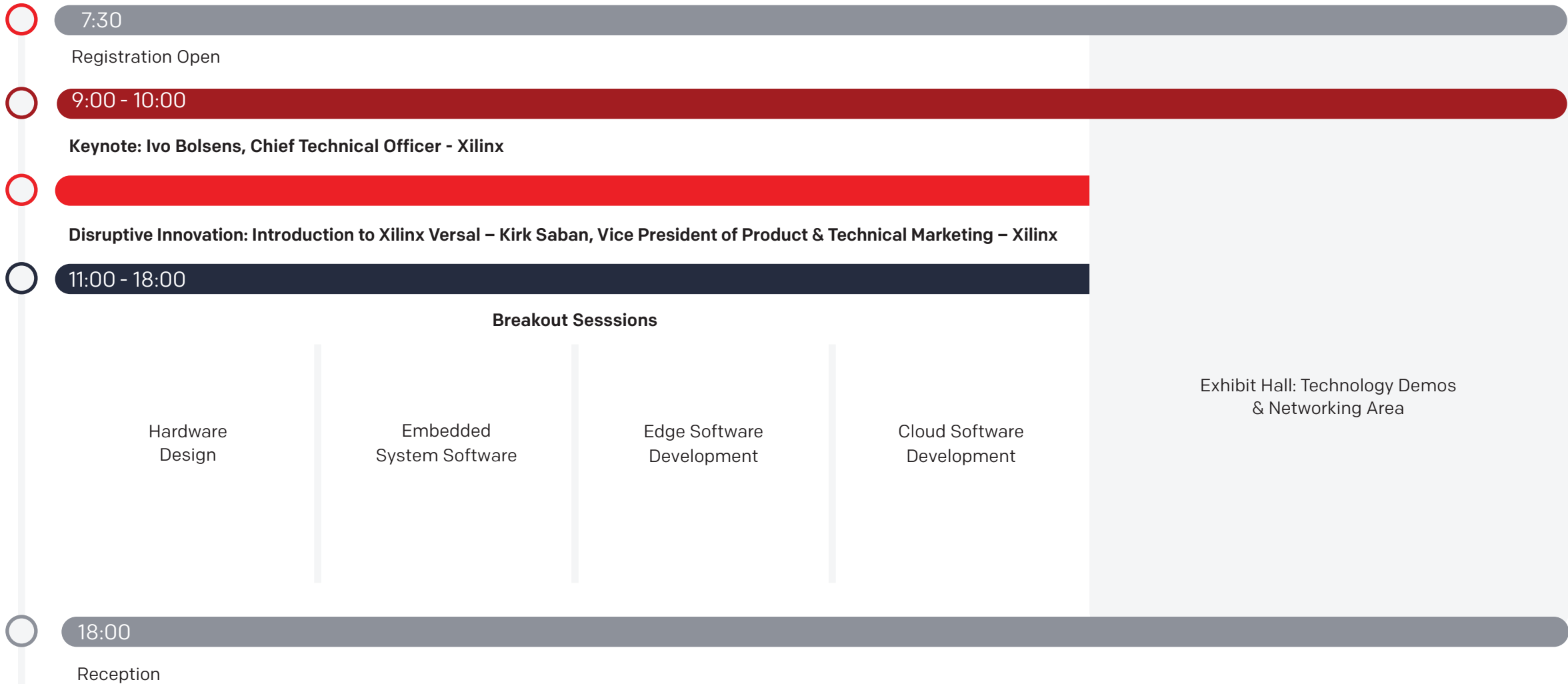


December 10th



**Updated 11/29 (Subject to change)

Hardware Design - Platinum Ballroom 1

This track is intended for hardware designers and system architects who want to learn best practices in using Vivado (timing, synthesis, partial reconfiguration), HLS/IPI, Model Composer and other tools. It will consist of sessions conducted by Xilinx technologists, guest speakers, and conclude with an expert panel discussion and Q&A. This popular track is suited for hardware designers using FPGAs for a wide variety of traditional FPGA applications.

11:00 - 18:00

- > Session: IPI Methodology
Speaker: Dan Michek
Xilinx
Time: 11:15 - 12:00
- > Session: Revision Control Methodology
Speaker: Brian Lay
Xilinx
Time: 12:15 - 13:00
- > Session: HLS Methodology
Speaker: Frederic Rivoallon
Xilinx
Time: 13:45 - 14:30
- > Session: RTL Synthesis Methodology
Speaker: Bala Krishnamurthy
Xilinx
Time: 14:30 - 15:00
- > Session: Timing Closure Tips and Tricks
Speaker: Ron Plyler
Xilinx
Time: 15:00 - 15:45
- > Session: Partial Reconfiguration: An Evolution of Reconfigurable Platforms
Speaker: David Dye
Xilinx
Time: 16:00 - 16:45
- > Session: Expert Panel
Speaker: Premduth Vidyanandan
Xilinx
Time: 16:45 - 17:30

Embedded System Software - Gold 2

This track is intended for developers of software for embedded systems who want to hear about best practices for heterogeneous runtime design. Technical content in this track will cover open source OS and hypervisor considerations as well as multimedia and platform management. Discussions in this track will focus on ARM-based Xilinx SoC and RFSoc platforms.

11:00 - 18:00

- > Session: Xilinx Software Strategy & Development Introduction
Speaker: Tony McDowell
Xilinx
Time: 11:15 - 12:00
- > Session: SoC Platform Management
Speaker: Aniket Kolarkar
Xilinx
Time: 12:15 - 13:00
- > Session: Heterogenous Realtime Software Architecture
Speaker: Edgar Igesias
Xilinx
Time: 13:45 - 14:30
- > Session: From DC to Daylight, Xilinx RF Solutions for Wired, Wireless and High Frequency Applications
Speaker: Glenn Steiner
Xilinx
Time: 13:45 - 15:15
- > Session: ENEA: High-Performance Real-Time Linux Solution for Xilinx Ultrascale+
Speaker: Patrik Strömblad
ENEA
Time: 14:30 - 15:00
- > Session: Multimedia SoC System Solutions Speaker: Forrest Pickett
Xilinx
Time: 15:00 - 15:45
- > Session: EBV
Speaker: Ian Greenshields
EBV
Time: 15:15 - 15:45
- > Session: Cortex-M1 for Xilinx Programmable Platforms
Speaker: Simon George & Phil Burr
Xilinx & ARM
Time: 16:00 - 17:00
- > Session: Silica
Speaker: Michaël Uyttersprot
Silica
Time: 17:15 - 17:45

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> Šæà: Design Accelerators for Vision Systems using Simulink®, Xilinx Model Composer and SDSoc

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Room: Lux

: Uttara Kumar, Xilinx

Time: 11:15 - 13:15 and 14:00 - 16:00

Cloud Software Development - Gold 3

This track is intended for application developers and system architects who are designing accelerated applications in the data center or cloud – for data analytics, financial, genomics, video streaming and more. Emphasis will be on development and deployment with SDAccel and compute acceleration libraries that form the software acceleration stack for high performance Xilinx Virtex FPGAs used in cloud and on-premise data centers. Cloud FPGA computing services like AWS F1 as well as data center hardware accelerator platforms will be covered.

11:00 - 18:00

- > **Session:** State of FPGA Based Acceleration
Speaker: Vinay Singh
Xilinx
Time: 11:15 - 11:45
- > **Session:** Scaleflux - Computational Storage: Acceleration Through Intelligence & Agility
Speaker: Thad Omura
Scaleflux - EVP Marketing
Time: 14:15 - 14:45
- > **Session:** Accelerating AI in Datacenters: Xilinx ML Suite
Room - Basalt
Speaker: Kamran Khan, Xilinx
Time: 16:00 - 17:00
- > **Session:** Fundamentals of FPGA Based Acceleration
Speaker: Sergei Storojev
Xilinx
Time: 11:45 - 12:30
- > **Session:** Maxeler: Amplifying the Power of Xilinx Datacenter Solutions in Finance and HPC
Speaker: Georgi Gaydadjiev
Maxeler
Time: 14:45 - 15:15
- > **Session:** InAccel: Cloud FPGA-Acceleration of Spark ML using Containers
Speaker: Chris Kachris
InAccel - CEO, Co-Founder
Time: 16:30 - 17:00
- > **Session:** NGCodec
Speaker: Ian Jefferson
NGCodec
Time: 12:30 - 13:00
- > **Session:** Politecnico Di Torino: F1 Acceleration for Montecarlo: Financial Algorithms on FPGAs
Speaker: Liang Ma
Politecnico Di Torino
Time: 15:15 - 15:45
- > **Session:** Accelerating Databases with FPGA
Speaker: Prasanna Sukumar
Reniac - Head of Engineering
Time: 17:00 - 17:30
- > **Session:** V-Nova
Speaker: Fabio Murra
V-Nova
Time: 13:45 - 14:15
- > **Session:** Xelera
Speaker: Felix Winterstein
Xelera - CEO
Time: 16:00 - 16:30
- > Session: Omnitek
Room - Basalt
Speaker: Roger Fawcett, Omnitek
Time: 17:00 - 17:30
- > **Session:** Accelerating Memcached on Cloud FPGAs
Speaker: Andrew Canis & Ruolong Lian
LegUp Computing - CEO & COO
Time: 17:30 - 18:00

A Look into Versal - Basalt

In addition to the other tracks, we will be holding two sessions that take a deep dive into Versal, the industry's first ACAP. These sessions will include an overview of the architecture of the Versal Platform as well as deep dive into the Software Programmable Engine and Programming Environment.

11:00 - 18:00

> **Session:** Project Everest: A Look Inside the First ACAP

Speaker: Sumit Shah

Xilinx

Time: 11:15 - 12:00

> **Session:** Project Everest: Software Programmable Engine
and Programming Environment

Speaker: Ambrose Finnerty

Xilinx

Time: 12:00 - 13:00