32 to 56 Gbps Serial Link Analysis and Optimization Methods for Pathological Channels

Al Neves, Tim Wang Lee (Wild River Technology)
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Abstract

For many SerDes applications, when there is a channel that is proving difficult to achieve the required BER performance, the question of where and what to apply to the effort must be answered. The key focus of this tutorial is to unite a concerted channel analysis approach implementing both measurement hardware and EDA tools with contemporary SERDES internal tools (internal eye scan) for the purpose of optimizing BER for highly pathological channels (crosstalk, loss, return loss degradation, etc.,).

Speakers

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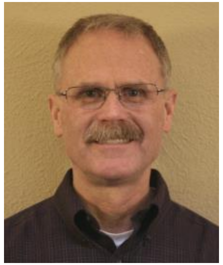

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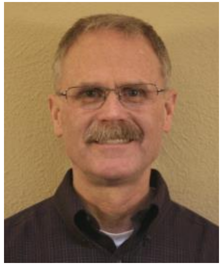
Agenda



Jack Carrel

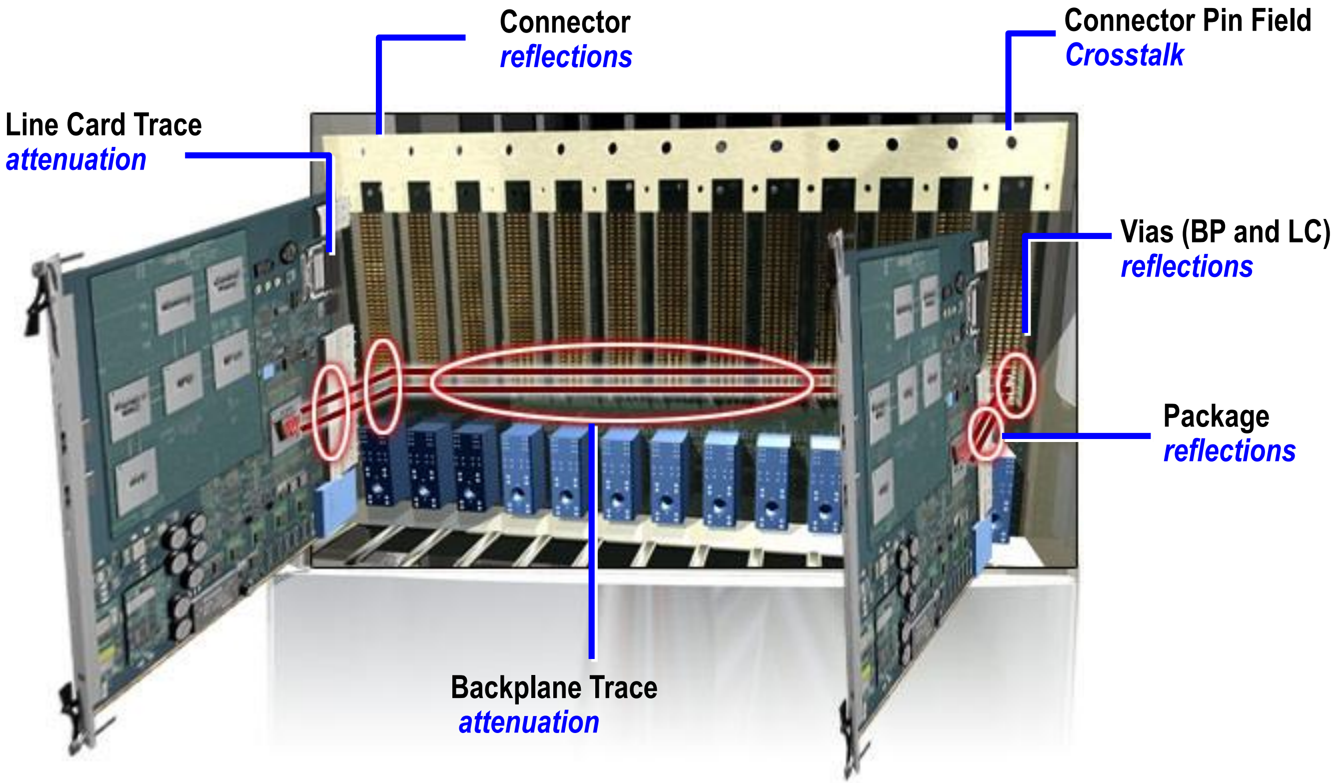
SerDes Apps. Engineer, Xilinx

- Full-Link KR Example
- What is a "Pathological Channel"
- Measuring Pathological Channels
- Band Limited S-Parameters
- Using the Pulse Response to Gain Insight

▪ BREAK

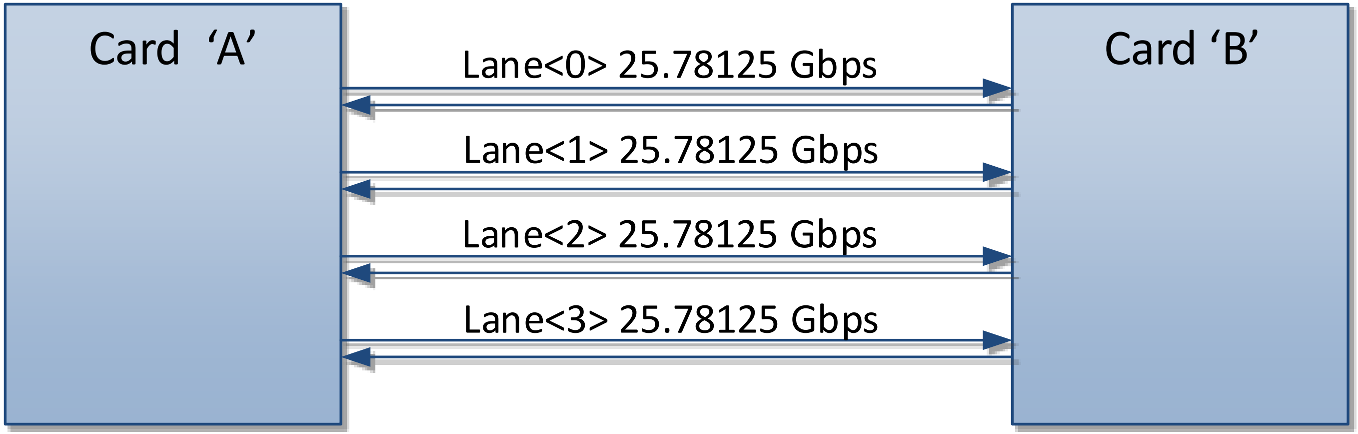
- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- Summary

Serial I/O Channel – Backplane Channel

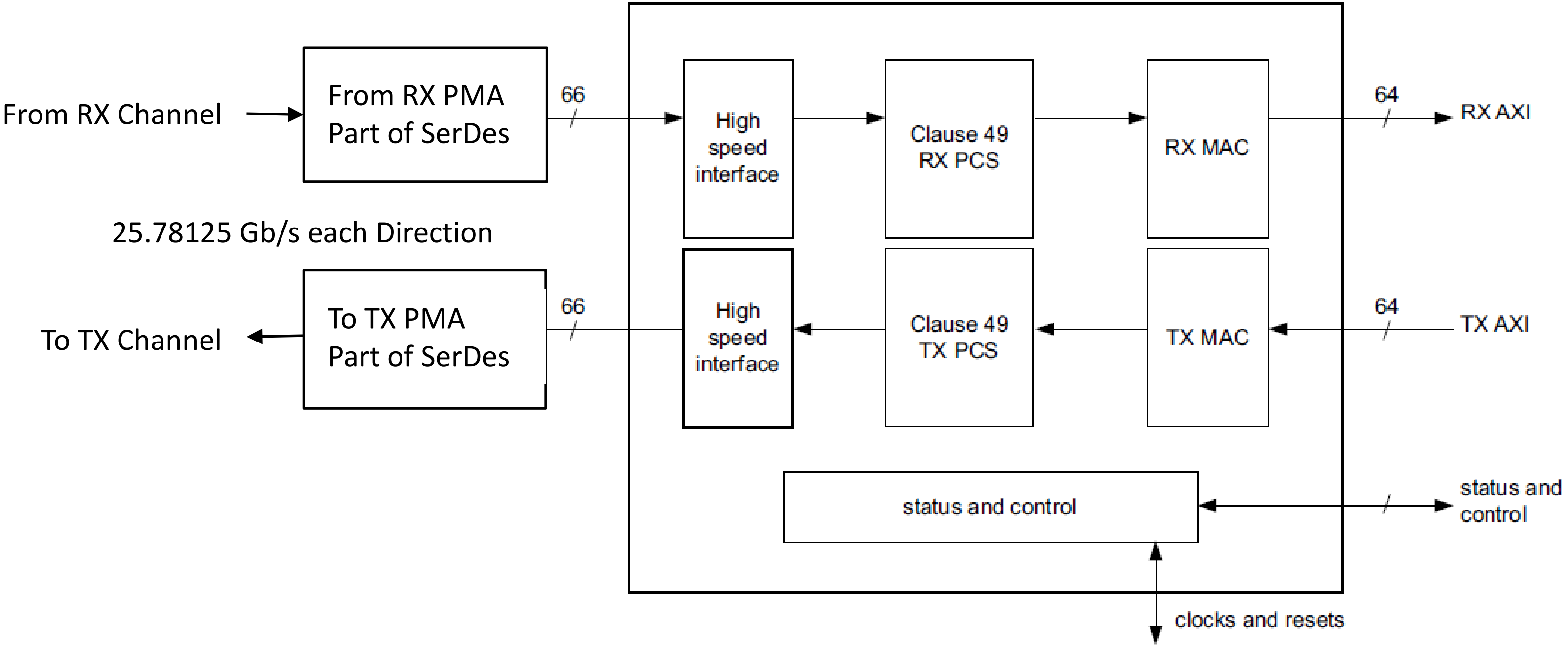


100GBASE-KR Backplane Interface

100GBASE-KR



100GBASE-KR: PCS/MAC Functional blocks



100GBASE-KR Backplane Channel

IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX – Annex 93B

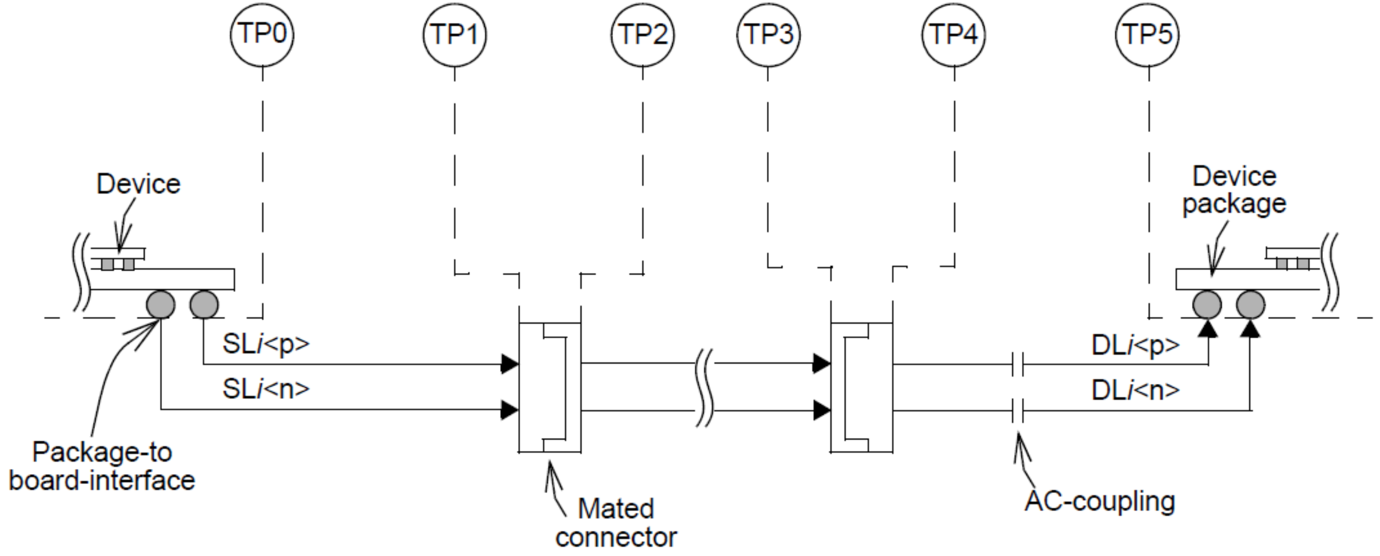


Figure 93B–1—Reference model (one direction from one lane is illustrated)

100GBASE-KR: Channel Testing

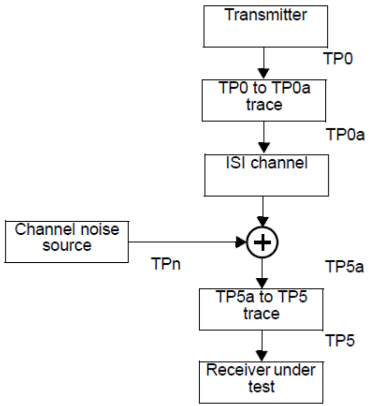
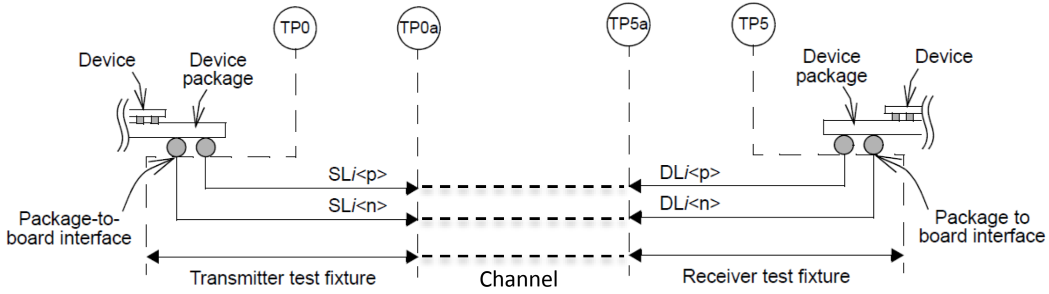


Figure 93C–2—Interference tolerance test setup



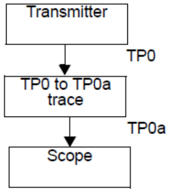
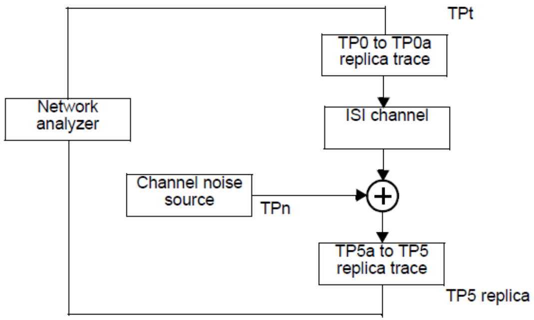


Figure 93C–3—Interference tolerance transmitter test setup



IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX

Figure 93C–4—Interference tolerance channel s-parameter test setup

100GBASE-KR: Channel Spec's

IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX

$$IL(f) \le \begin{cases} 1.5 + 4.6\sqrt{f} + 1.318f & 0.05 \le f \le f_b/2 \\ -12.71 + 3.7f & f_b/2 < f \le f_b \end{cases} \quad \text{(dB)}$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$IL(f)$ is the insertion loss at frequency f

$$RL_d(f) \ge \begin{cases} 12 & 0.05 \le f \le f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \le f_b \end{cases} \quad \text{dB}$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$RL(f)$ is the return loss at frequency f

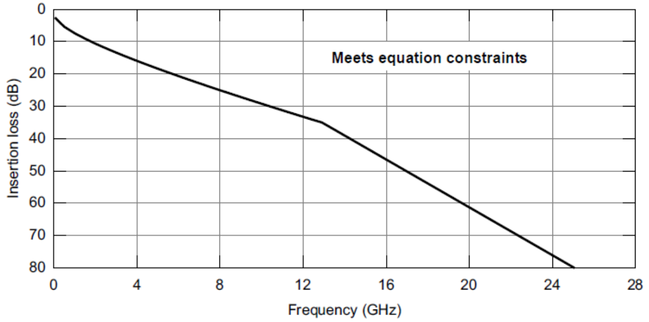


Figure 93–13—Insertion loss limit

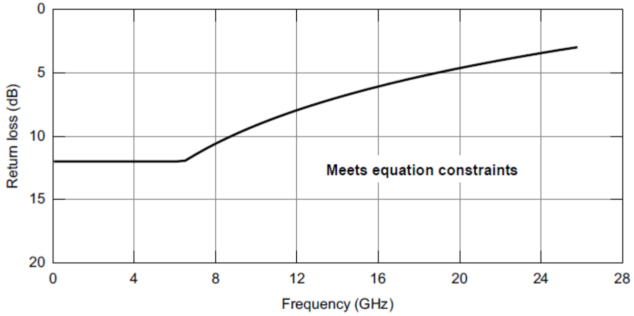
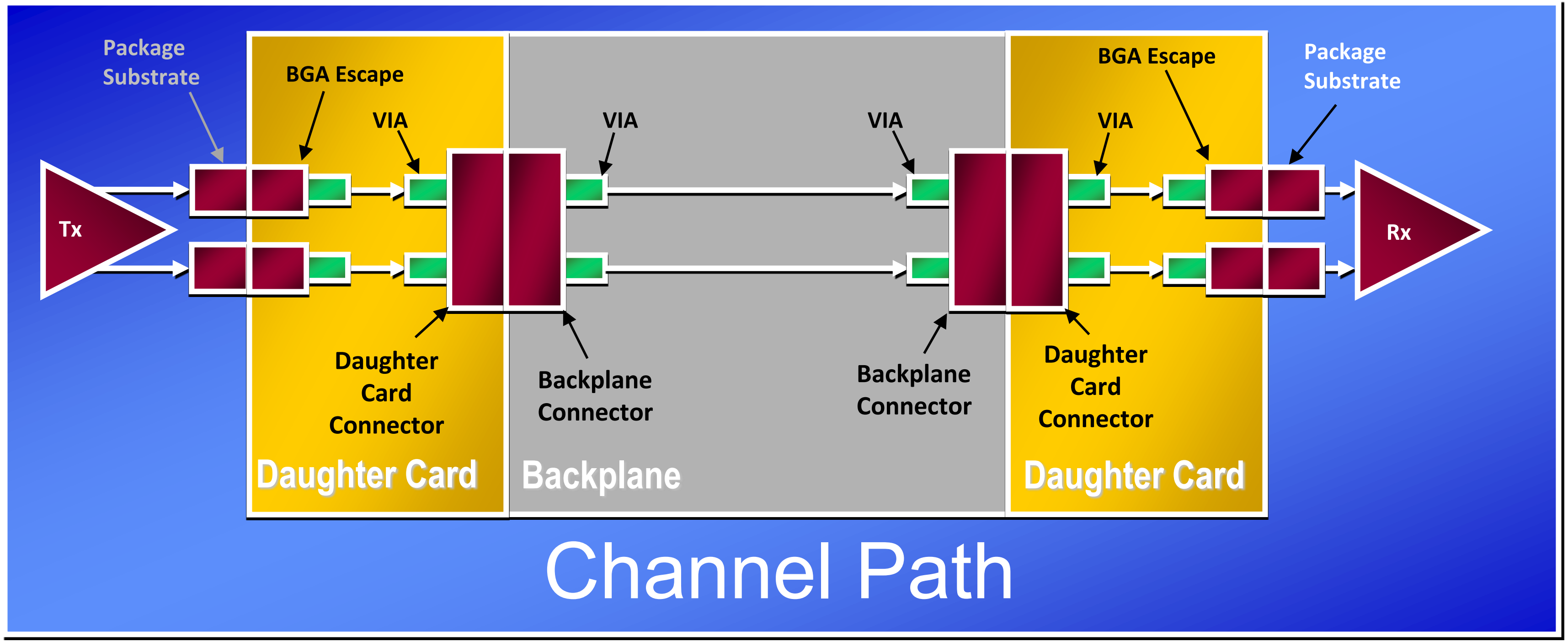
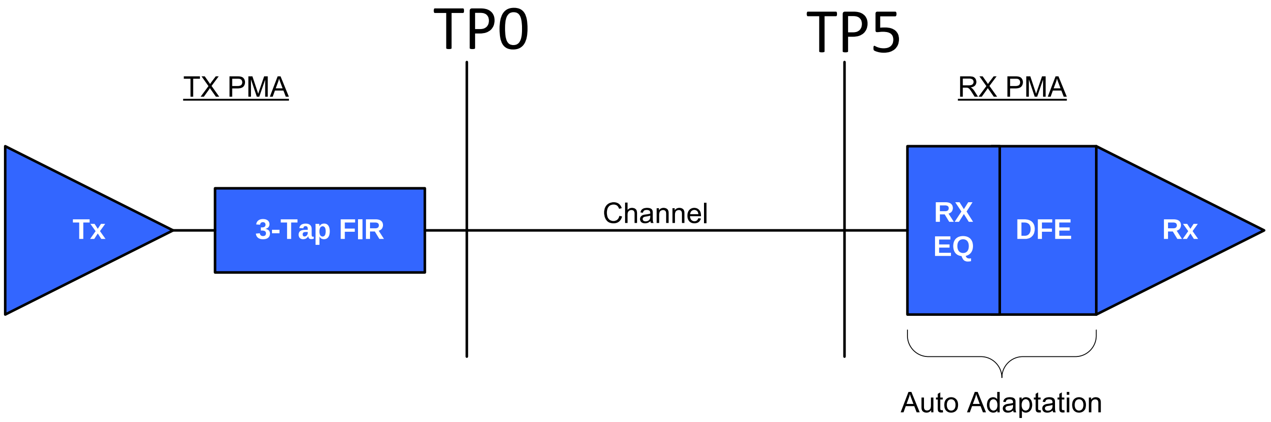


Figure 93–14—Differential return loss limit

100GBASE-KR: Channel Path Details – 1 Lane



100GBASE-KR: Rx/Tx Components – 1 Lane



100GBASE-KR: What's next?

- "No battle plan survives contact with the enemy"
  - Helmuth von Moltke

- "Everyone has a plan 'til they get punched in the mouth"
  - Mike Tyson

What if the link doesn't work?
"Stay Tuned"

Agenda

Al Neves

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Pathological Design Space – Advancing optimization and characterization

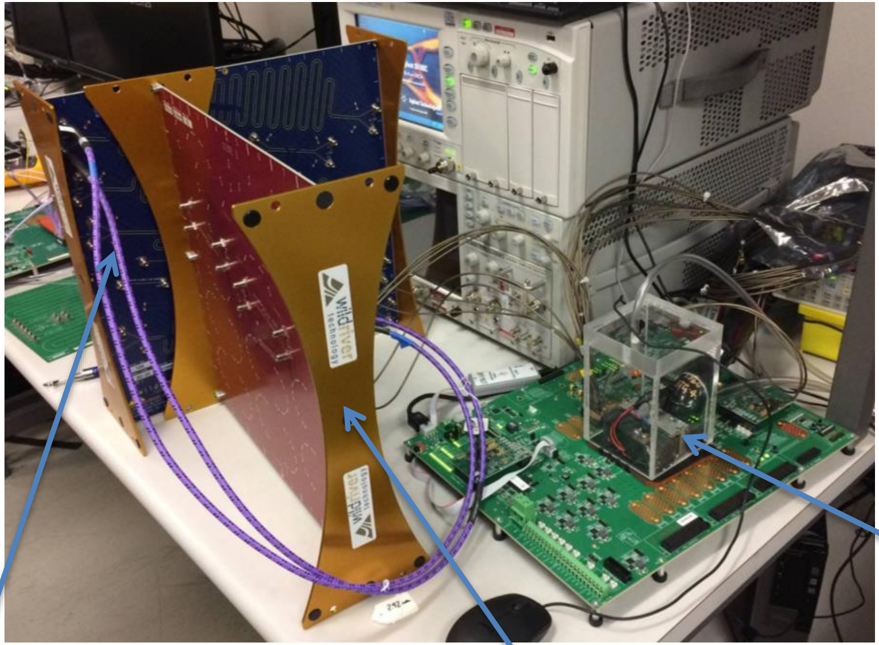
- Backplane characterization is a requirement
- Backplanes are, however, very complicated
- Difficult to form a coherent optimization strategy
- Difficult to establish clear margins versus issues

- *Good Engineering starts simple and systematic!*

“It’s all about the margins…”

Jack Carrel

Pathological Design Space – Guiding Principles



- Replace backplane with simple pathological structures.
- Structures can be systematically added
- Re-optimization for new and simple channel, then…
- Analysis of margin

UltraScale+ TX and RX, 32Gbpsec NRZ

XTALK-32 Crosstalk Platform

ISI-32 Loss Platform

Pathological Channel Concept

- **What is it?**
- **Example**
- **Benefits**
- **More Examples**

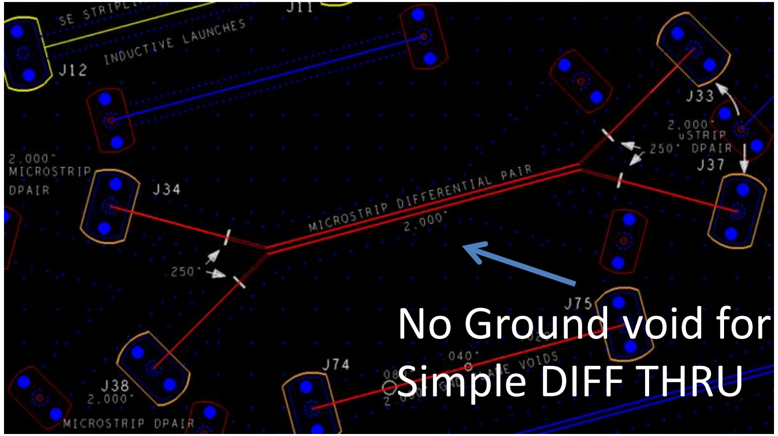
Pathological is an Analogous Concept

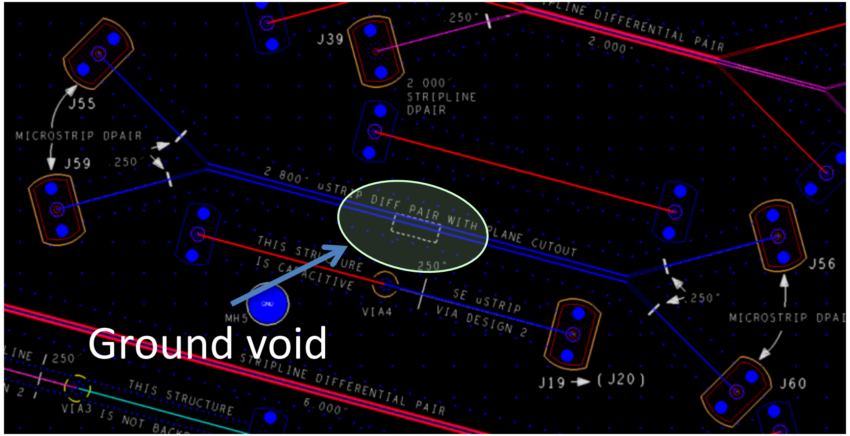
- Involving, caused by, or of the nature of a physical or mental disease, denoting a very specific disease
- For our application it denotes a stellar signal integrity structure with something with intentional poor S.I. added
- The overall structure itself, aside from the pathological element, is healthy with good signal integrity

Pathological Channel Concept – What is it?

- It is a family of interrelated structures
- There is always a root structure (like a THRU)
- Except for a single pathology, the structure is high S.I. (launches, transitions, fiber weave… etc.)
- You add the structures with stable phase, low skew matched cables with S-parameter models (for simulation) for combining pathologies
- EDA simulation of structures match measurements (testing IBIS AMI models, system simulations, testing optimization strategies in EDA)
- It follows quality recommendations of IEEE PG370 TG1, Test Fixture Group

Pathological Channel Concept – Example





- **2inch DIFF microstrip THRU,**
- Good signal integrity and low loss

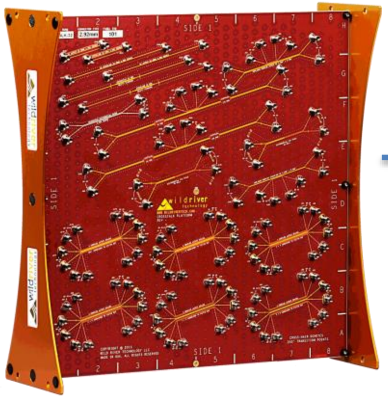
- *Also used for 2X THRU for AFR and Measure Based Modeled de-embedding structure on right*

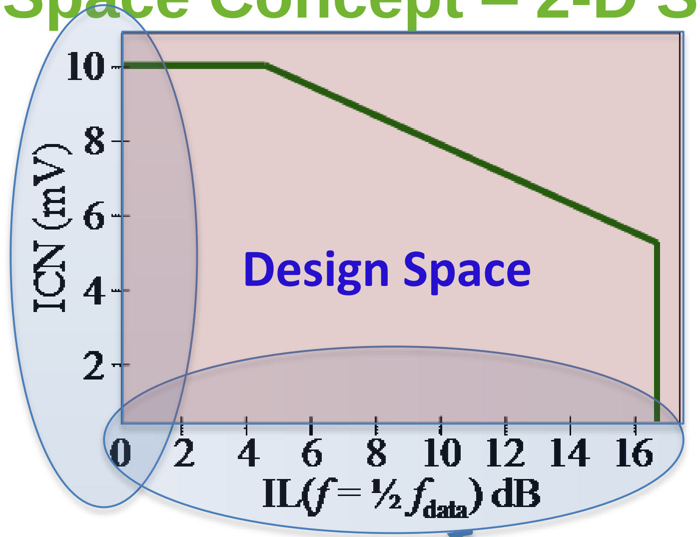
- **2inch DIFF microstrip THRU Exact Copy of left + Asymmetric Ground Void**
- Results in SDD11 degradation and mode issue of SCD21

Pathological Design Space - Benefits

- Improve SERDES characterization
- Ability to Improve manufacturing (Test, Product, and Characterization Engineering) and design process
- Drive technology tweaks and next generation products
- Provides systematic approach over complete design space of all pathologies
- Improve Measurement-Simulation correspondence
- Test IBIS AMI models over full Pathological space

Pathological Design Space Concept – 2-D Space





Loss and Crosstalk combinations can be mapped over the entire design space

Crosstalk Noise Test vehicle, calculated RX noise as Integrated Crosstalk Noise (ICN)

Insertion Loss Test Vehicle (IL) at Nyquist Sampling Freq

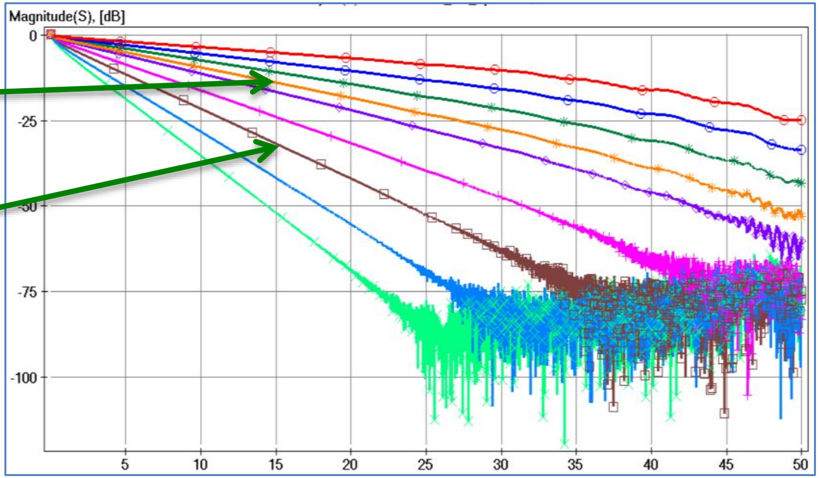
Pathological Space – Loss Example

START: Clean Pristine Low-Loss Channel

-13dB @15GHz

+Moderate Loss

-30dB @15GHz



+ RJ

next patho

+ SDD11 Degradation

next patho

+ PSEXT

next patho

+ Resonance

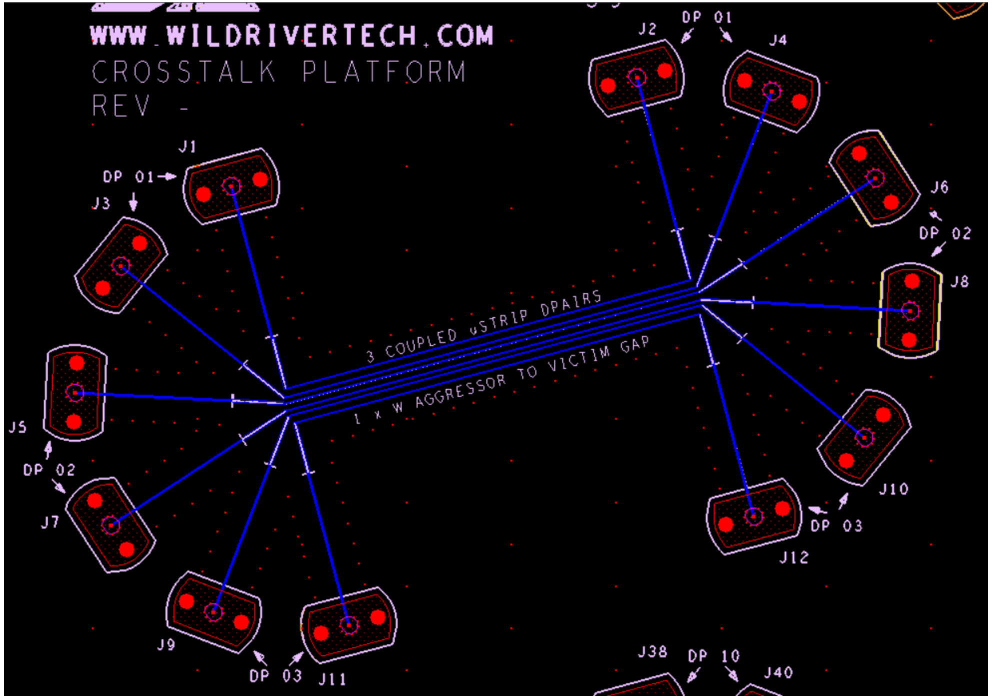
next patho

+More Loss

next patho

First start with pristine loss due to dielectric+skin of real channels, then add other pathologies

Pathological Design Space – Advancing optimization

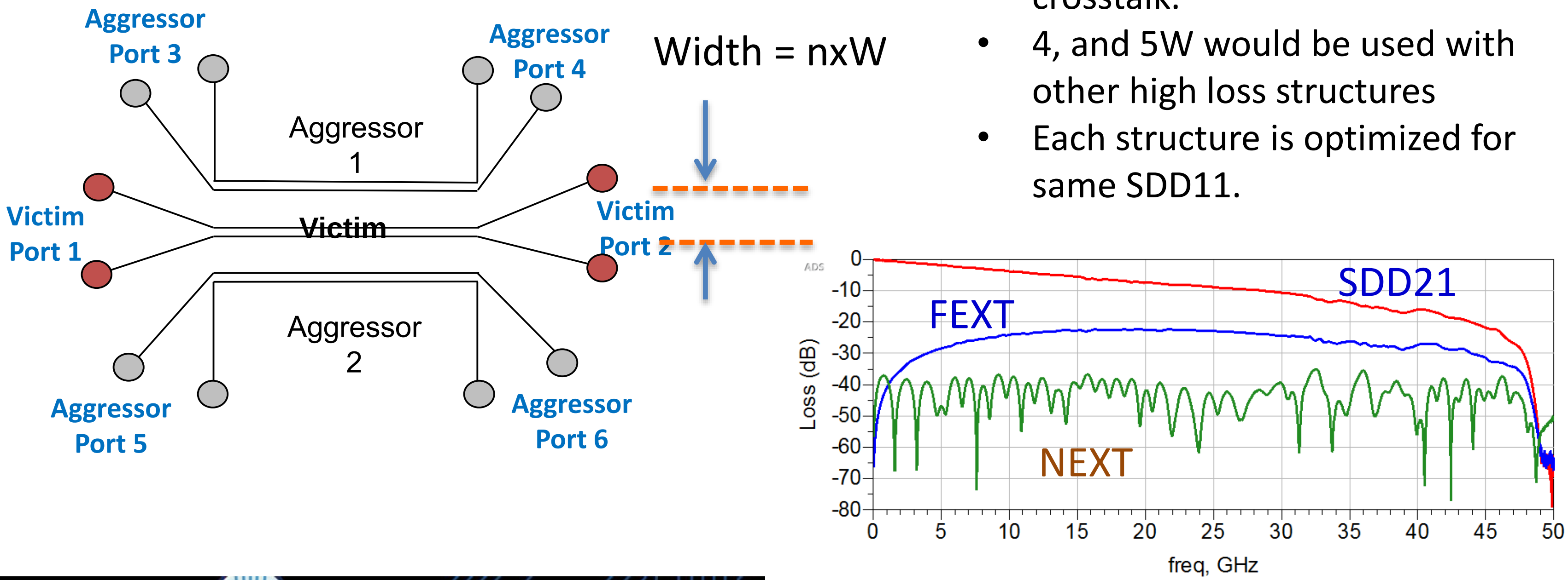


Crosstalk energy at RX also has SDD11 degradation, possible SCD21 (differential to common mode) and possible resonance.

So did the channel have issues due to RX noise due to crosstalk or the other issues?

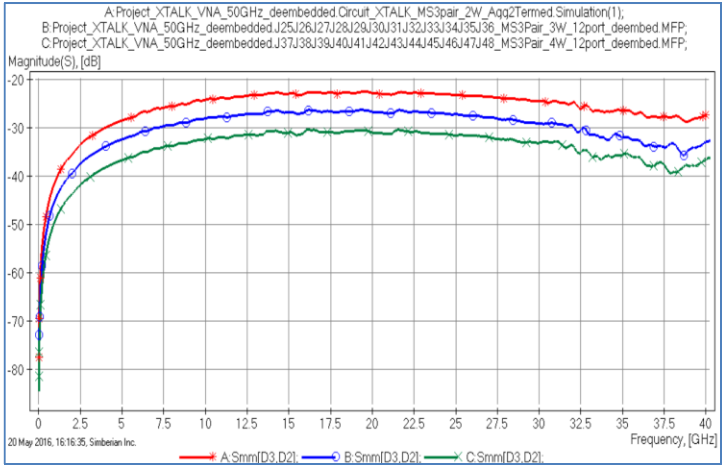
This structure provides real crosstalk with good S.I.

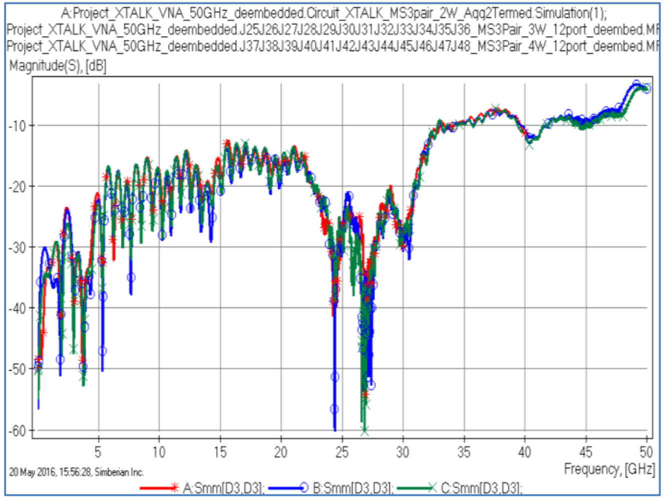
Pathological Space Design – Crosstalk Example



- Decrease width, .5W, 1W, 2W, 4W, and 5W, translates to less crosstalk.
- 4, and 5W would be used with other high loss structures
- Each structure is optimized for same SDD11.

Pathological Crosstalk Example – Changing FEXT with same SDD11





Sdd[4,1] (FEXT)

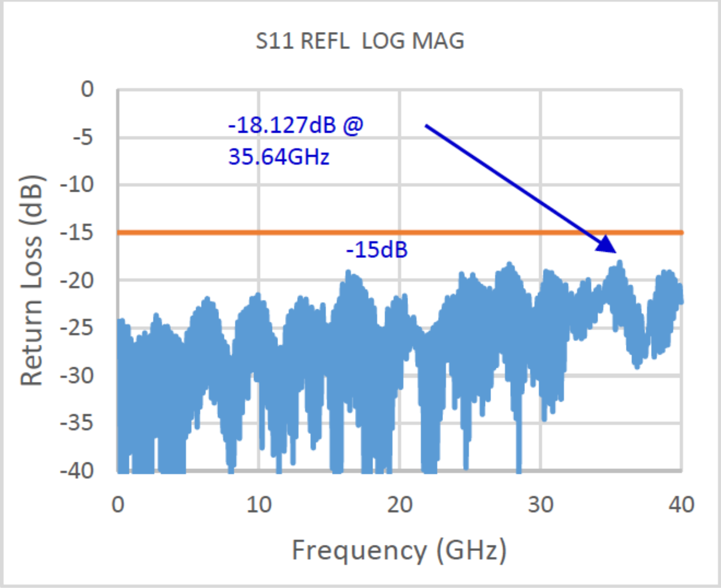
Red = 2W Separation

Blue = 3W Separation

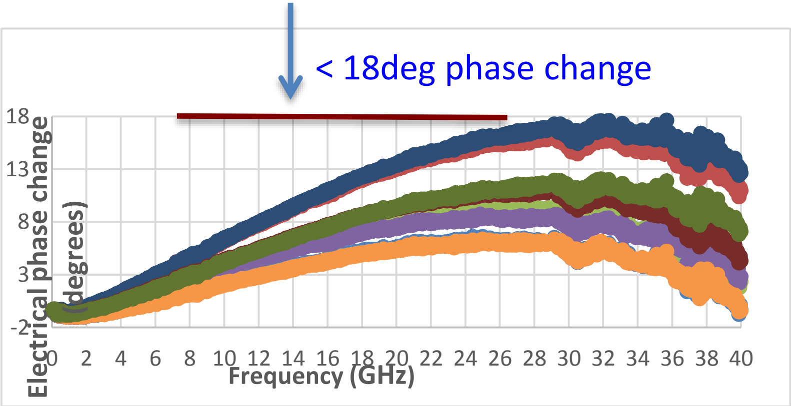
Green = 4W Separation

Each crosstalk structure is mapped to the same return loss, SDD11, only RX RMS noise changes

Cables are the hidden problem in many Jitter analysis systems



Good return Loss (or VSWR) and phase stability maintains jitter metrics consistently for skew matched cables (IEC-60966-1 spec) over full BW



In Summary….

Establishing a Pathological approach uses high-signal integrity structures with isolated issues, and adds those structures in a systematic fashion to establish a channel which serves to improve the methodology of determining margin, and optimization strategies and for the modern SERDES

References

- DesignCon2015 Tutorial: Lee Ritchey, Heidi Banes, Chun-Ting “Tim” Wang Lee, Al Neves: **Breaking the 32 Gb/s Barrier: PCB Materials, Simulations, and Measurements**
- DesignCon2014 Presentation: Bob Buxton, Al Neves: **The Role of Improved Measurements and Tools in Assessing Simulation-Measurement Correspondence for 32 Gbps**
- DesignCon2011 Paper: James Bell, Scott McMorrow, Martin Miller, Alfred Neves; **Developing Unified Methods of 3D Electromagnetic Extraction, System Level Channel Modeling, and Robust Jitter Decomposition in Crosstalk Stressed 10 Gbpsec Serial Data Systems**
- **WRT Skew Matched Data Sheets, www.wildrivertech.com**
- **XTALK-28/32 Data Sheet**
- **ISI-28/32 Data Sheet**
- IEEE PG370 TG1, Test Fixture Group Draft 1.0

Thank You! – Visit us Booth #850

Deschutes River   Maupin, Oregon

- Technology Development Platform 50GHz – Industry First
- Check out our latest Hermetic Cables to 50GHz
- 70GHz Test Fixture Design

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Agenda

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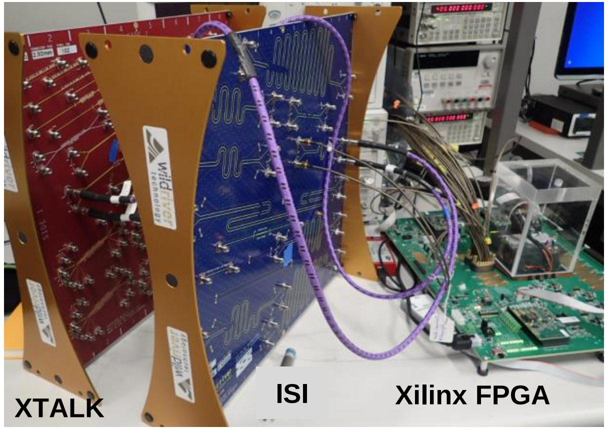
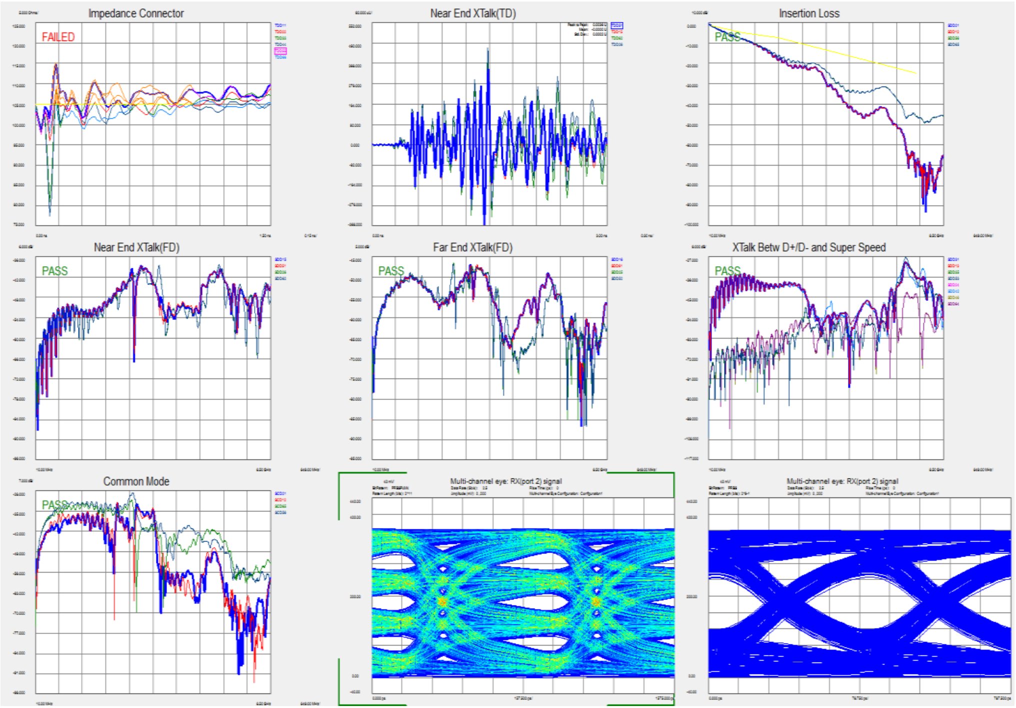
Where are We?

- In the Lab
- Early in design cycle
- Making measurements of prototype channel
- Backplane example
- Learn as early as possible:
  - Impedance profile
  - Insertion Loss
  - Return Loss
  - Eye diagram
  - Mode conversion

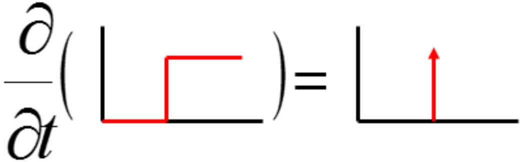


Specifics of Data Visualization

- **Traditional Options:**
  - Step Response
  - Impulse Response
  - S-parameters
  - Eye Diagrams
- **Trending Options:**
  - Single Pulse response
  - Channel Operating Margin (COM)
  - PAM-4 Eye Diagram
  - Multiport Analysis



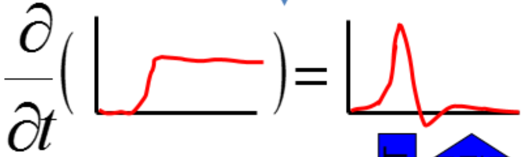
Step Response (TDR/TDT) vs Impulse Response

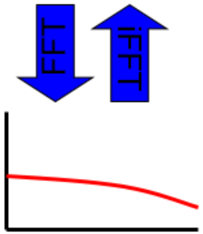


A perfect *impulse* is equivalent to a *differentiated* perfect *step*

Therefore if we differentiate the Step *Response* we get the Impulse *Response*

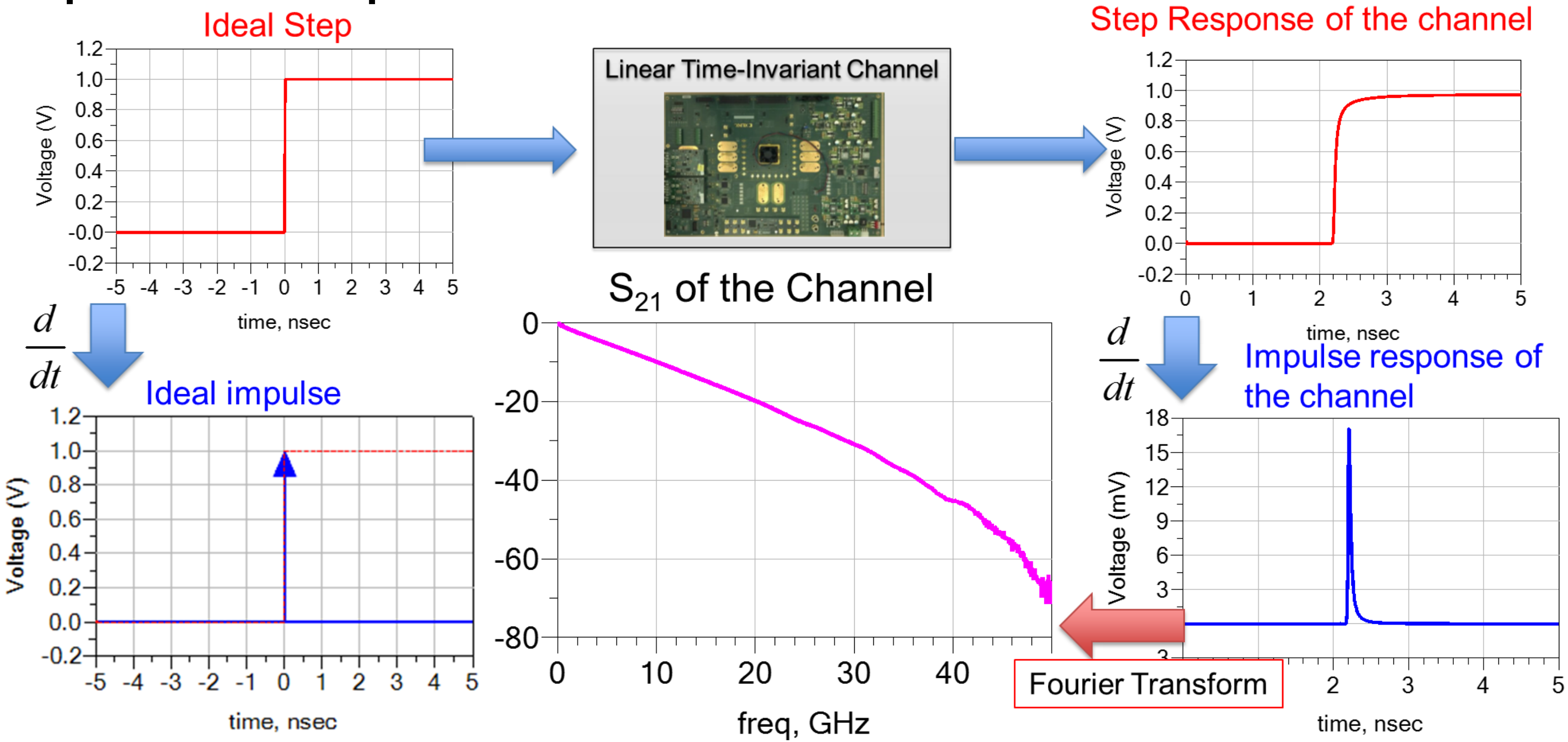
$$T(t) \otimes H(t) = R(t)$$





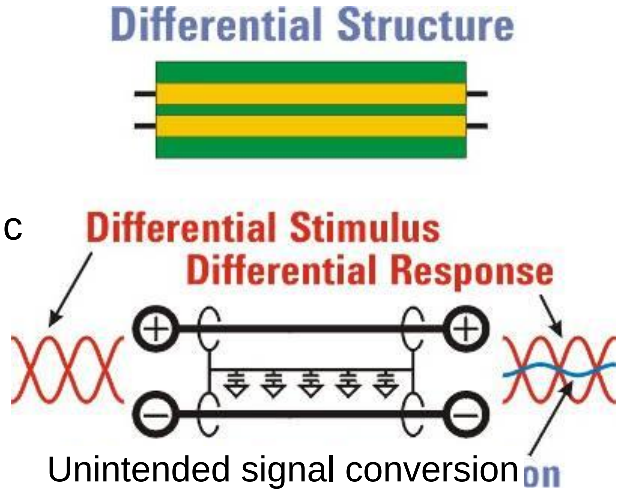
S-Parameter! (S_{21})

Impulse Response Derivation

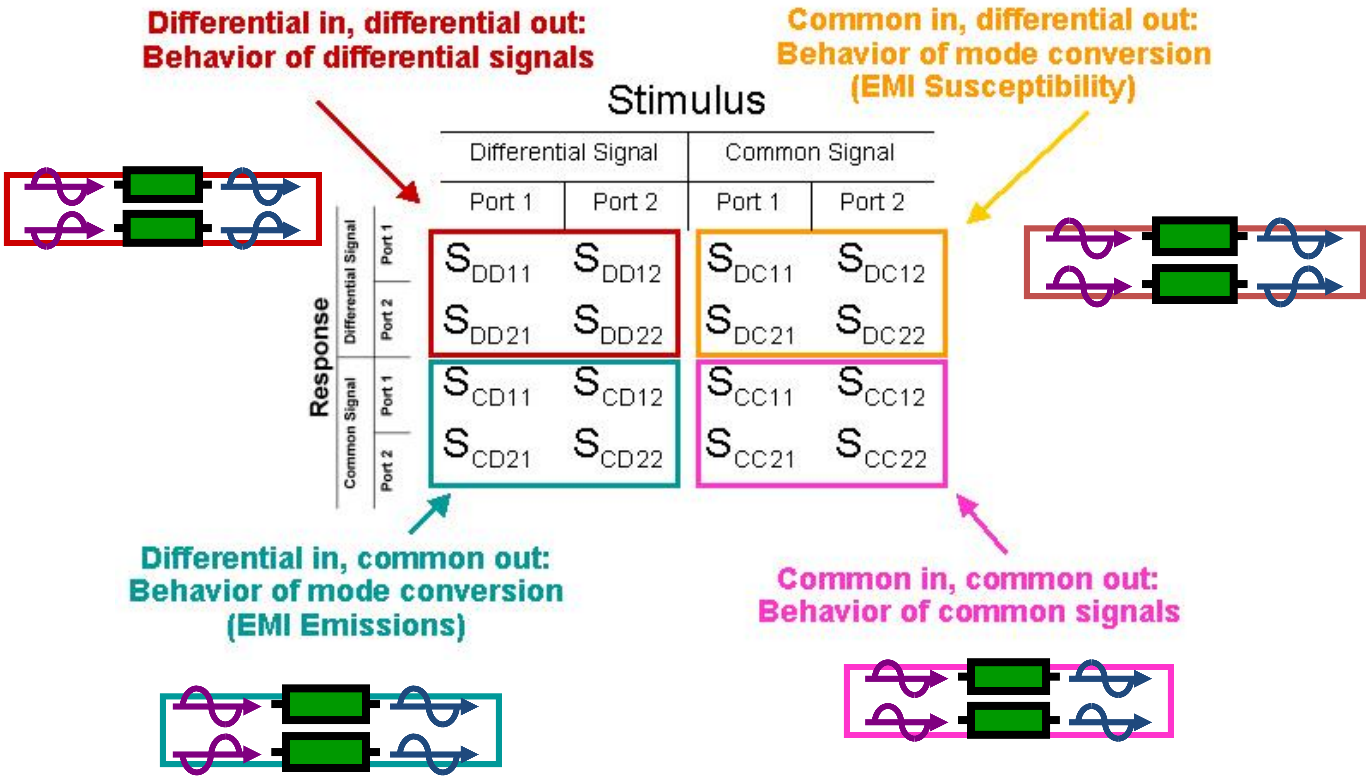


Why Differential Topologies?

- Ideal differential devices
  - Low voltage requirements
  - Noise and EMI immunity
  - Virtual grounding
- Non-ideal devices are not symmetric
  - Can be identified by signal-conversions
    - Differential → Common
    - Common → Differential
- Differential signal integrity design tools are needed



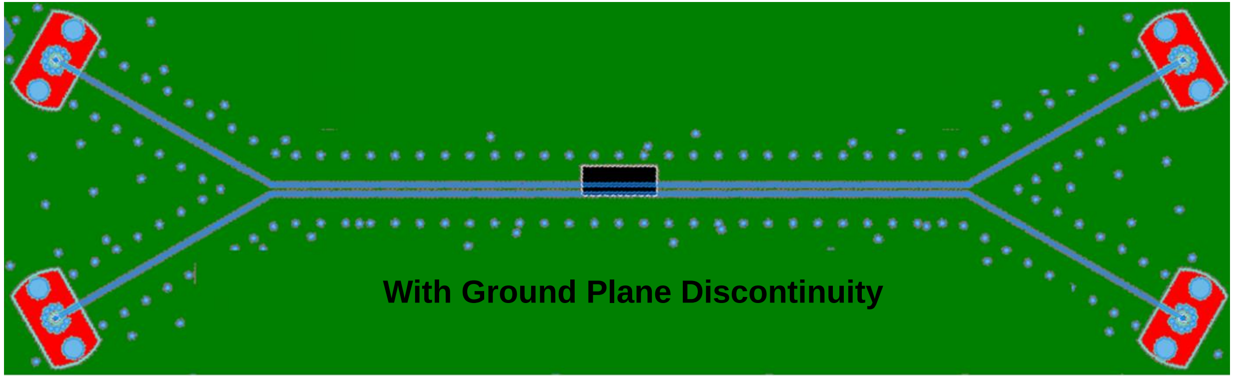
Differential S-parameters

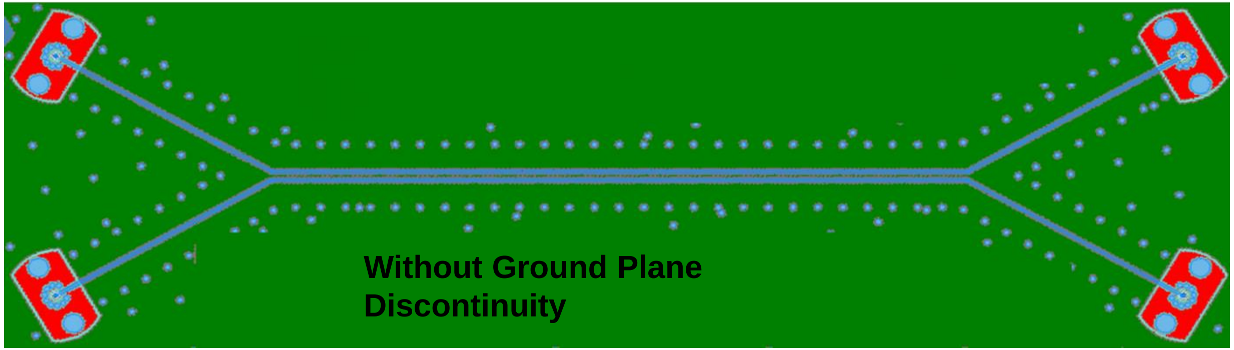


Our Analysis: Data Mining The Matrices

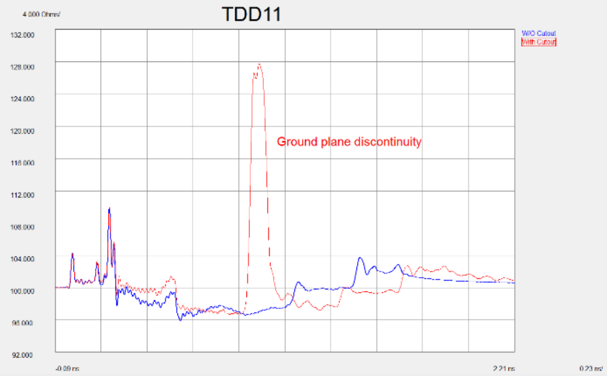
- TDD11-Differential impedance profile
- TDD21-Differential time domain transmission
- SDD11-Differential return loss at port 1
- SDD21- Differential insertion loss from port 1 to port 2
- SCD21-Differential-to-common mode conversion from port 1 to port 2
- SCD31- Differential-to-common mode conversion from port 1 to port 3
- SCD41-Differential-to-common mode conversion from port 1 to port 4

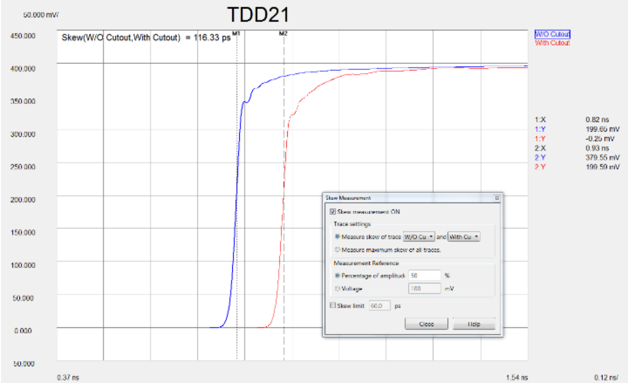
Ground Plane Discontinuity

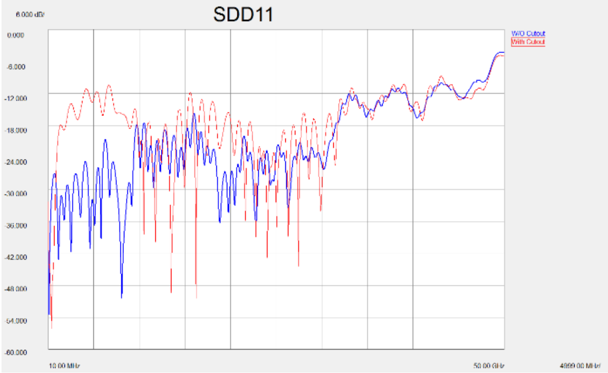


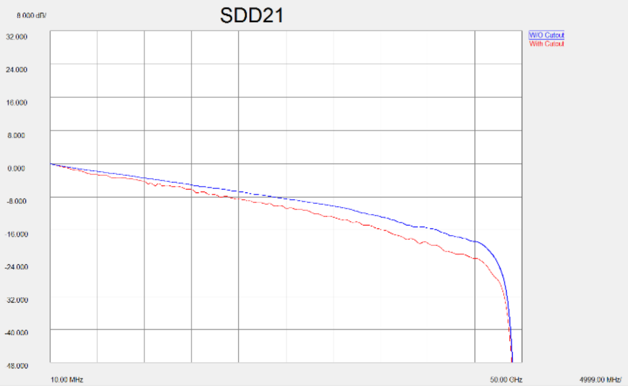


Analysis of Ground Plane Discontinuity

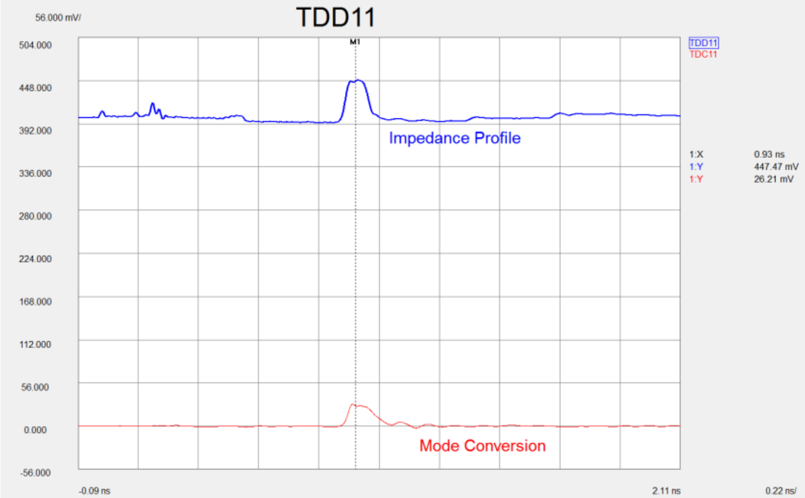








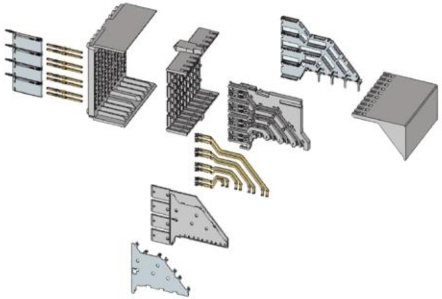
Mode Conversion Analysis of Ground Plane Discontinuity

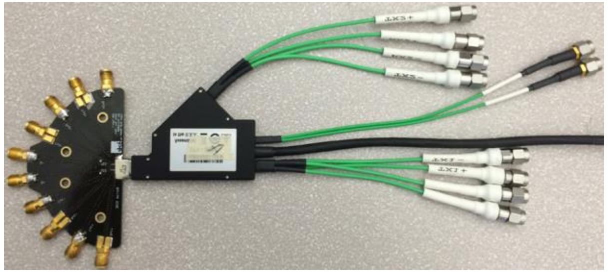


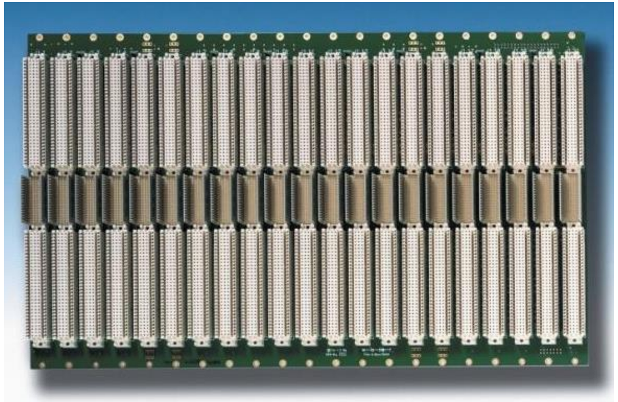
<u>Locate Source of Mode Conversion</u>

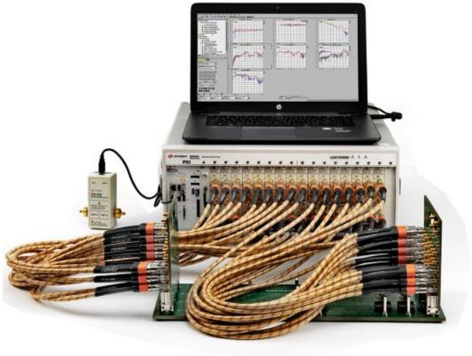
- Display mode conversion waveform (TCD11)
- Place marker on largest peak or valley
- Co-display impedance profile (TDD11) on same plot
- Autoscale and follow time marker to known structure

Simple 4-port Measurements are No Longer Enough

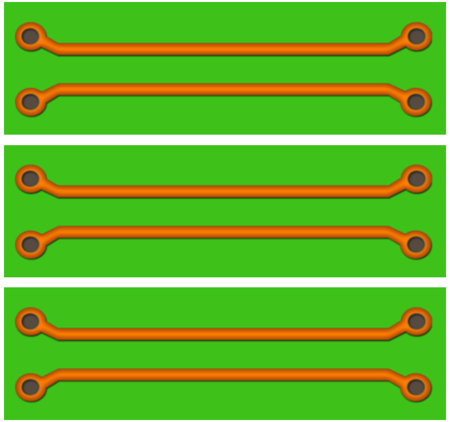






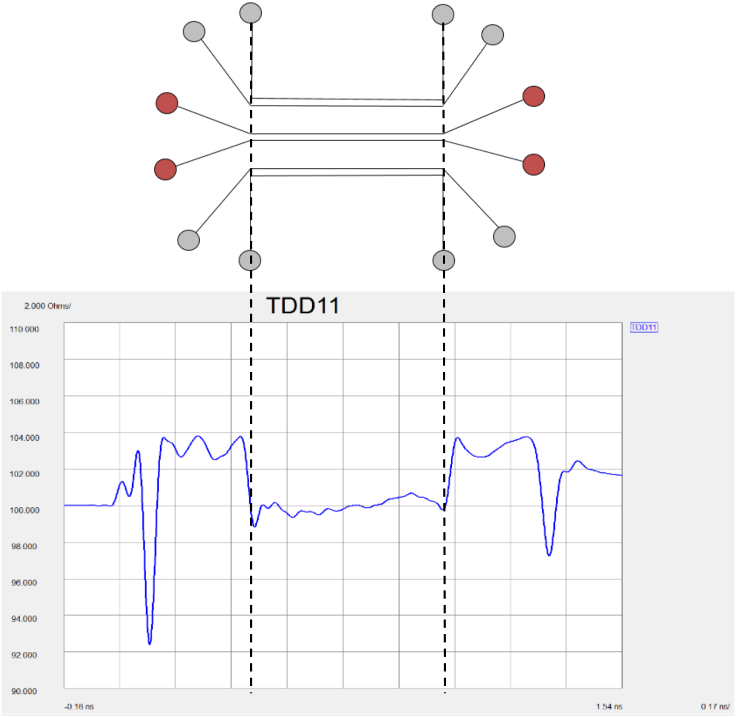


12-Port S-Parameters: Defining the Ports

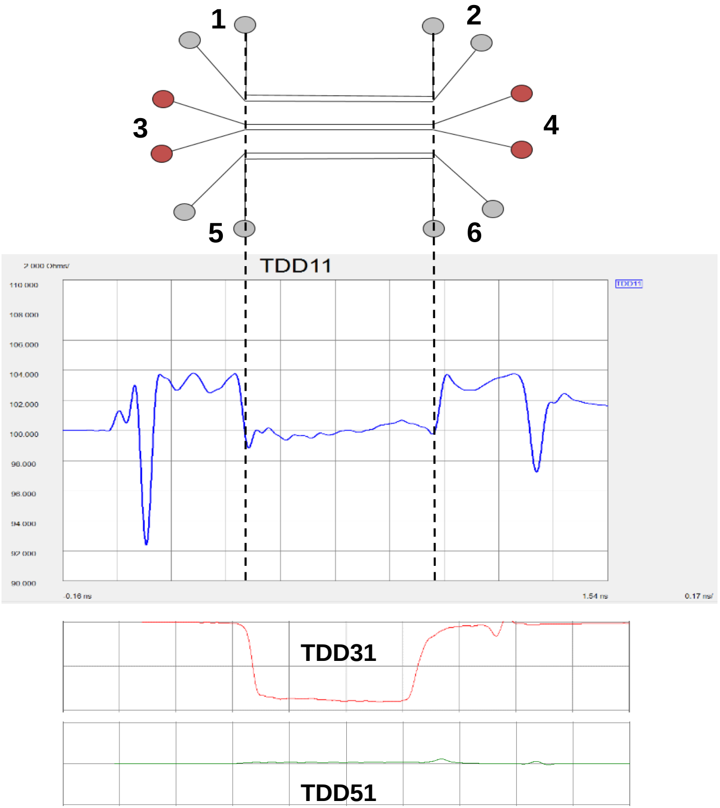


Differential ports	Single ended ports	Single ended ports	Differential ports
1	1 3	2 4	2
3	5 7	6 8	4
5	9 11	10 12	6

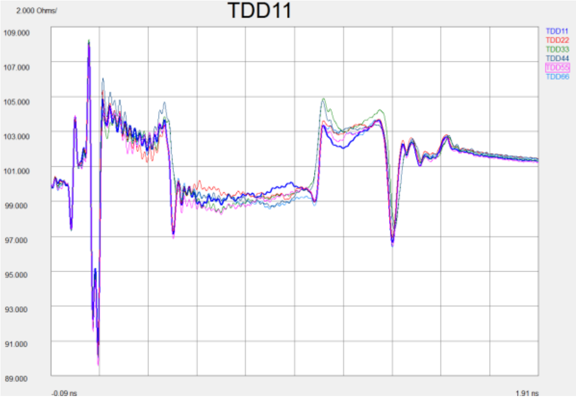
12-port Crosstalk Test Structure

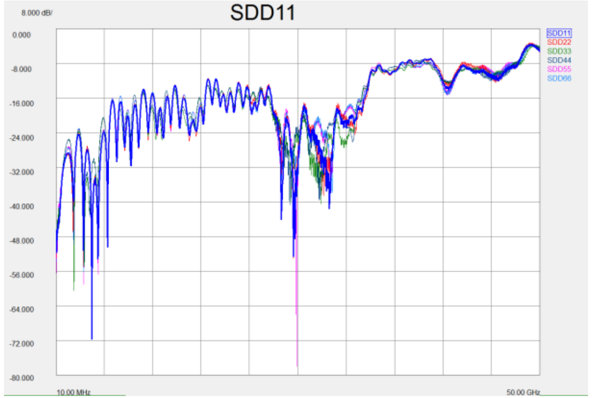


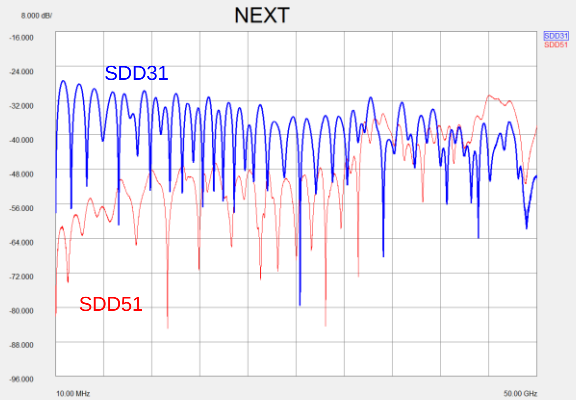
12-port Crosstalk Test Structure1

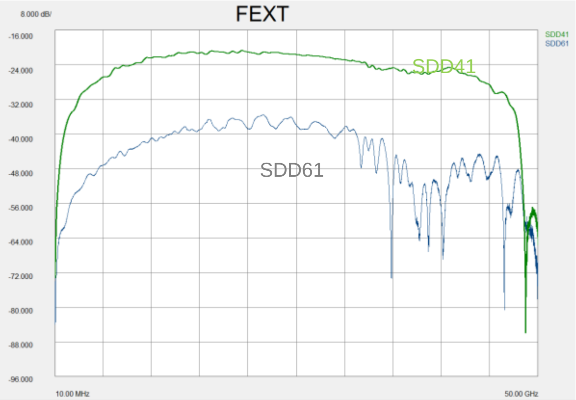


12-port Data Mining

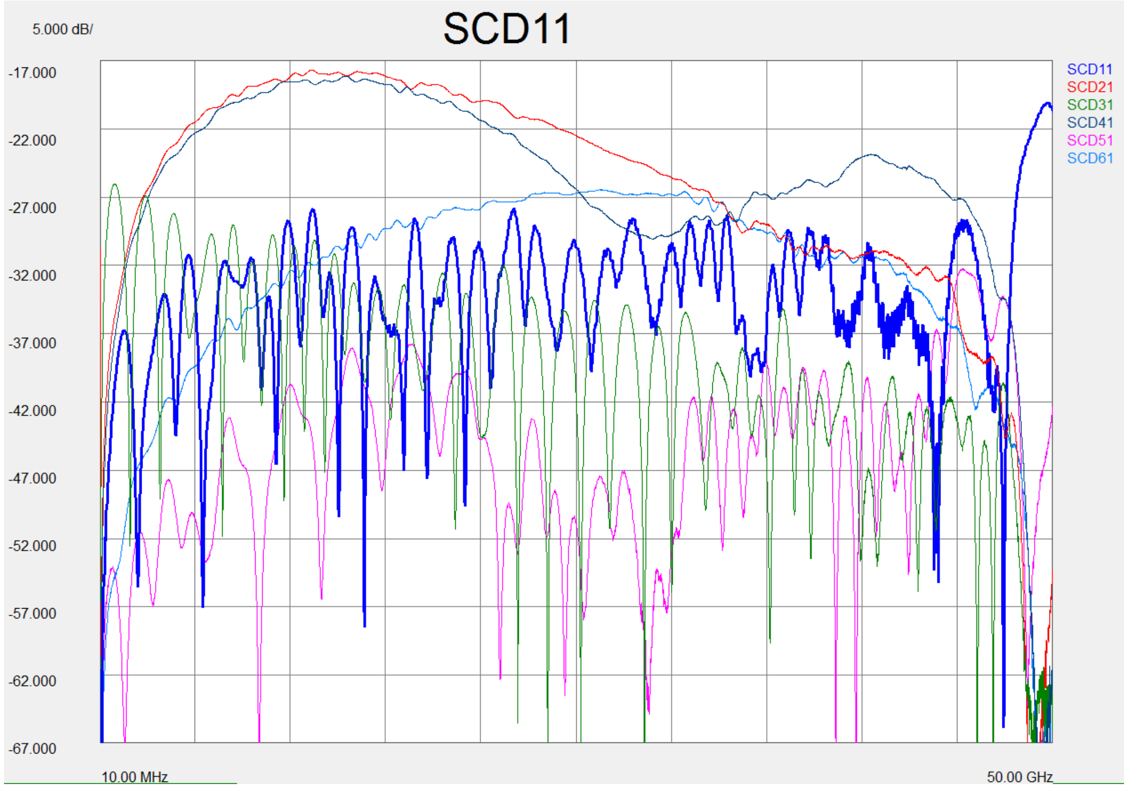






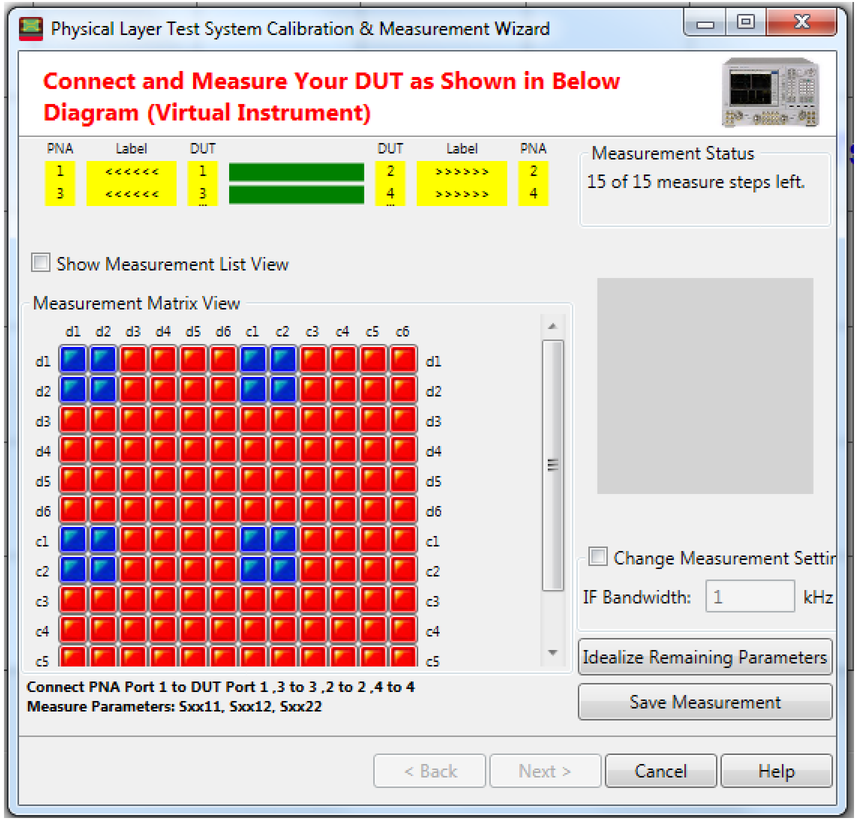


12-port Mode Conversion Analysis

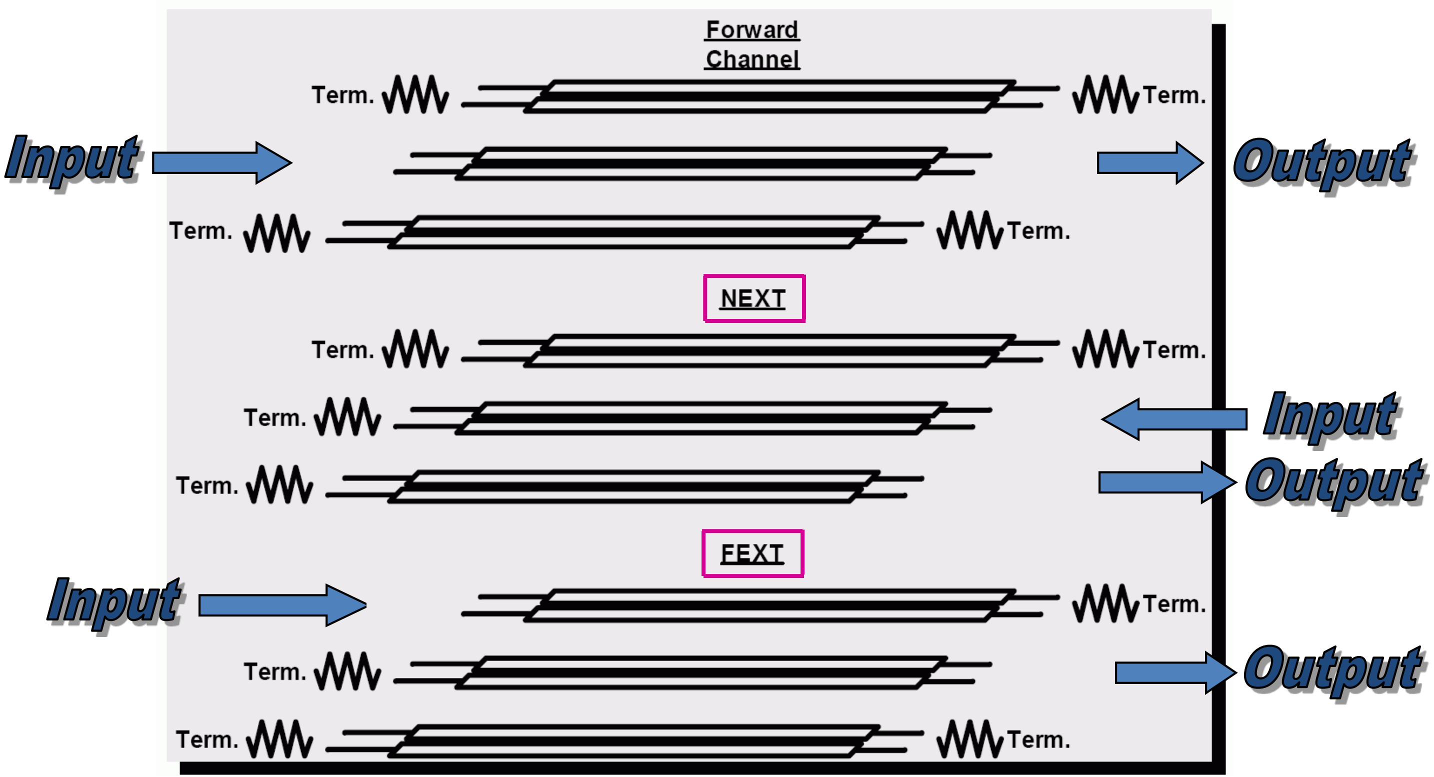


How to Obtain 12-port s-parameter Data?

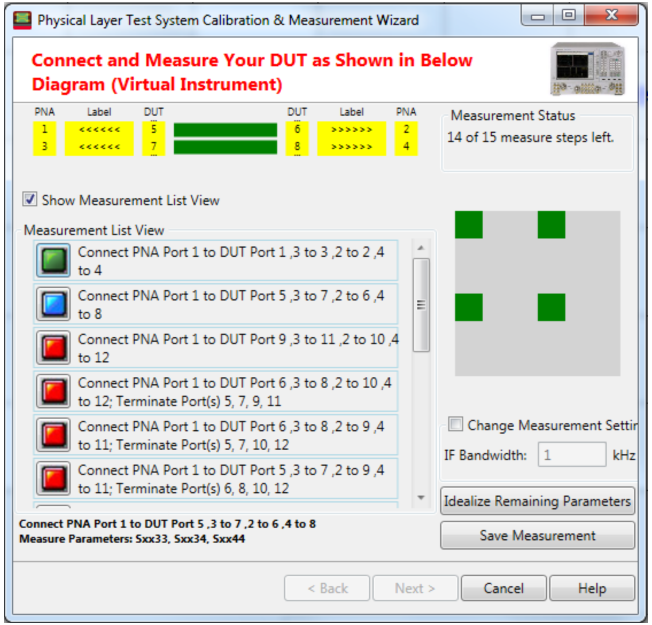
- Method #1: Use 12-port VNA
- Method #2: Use 4-port VNA with “Round Robin”
  - Requires 16 separate 4-port measurements to build 12-port s-parameter
  - 12-port can be build “live” or off line

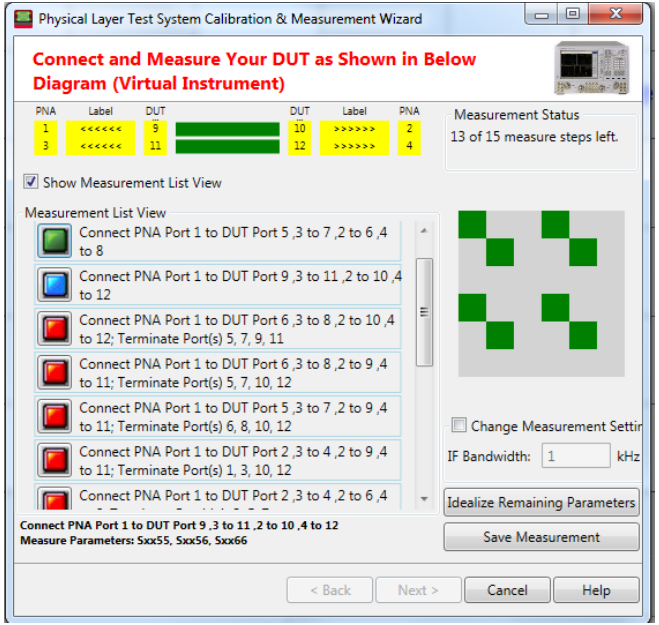


Differential NEXT & FEXT Measurements w/4-port VNA



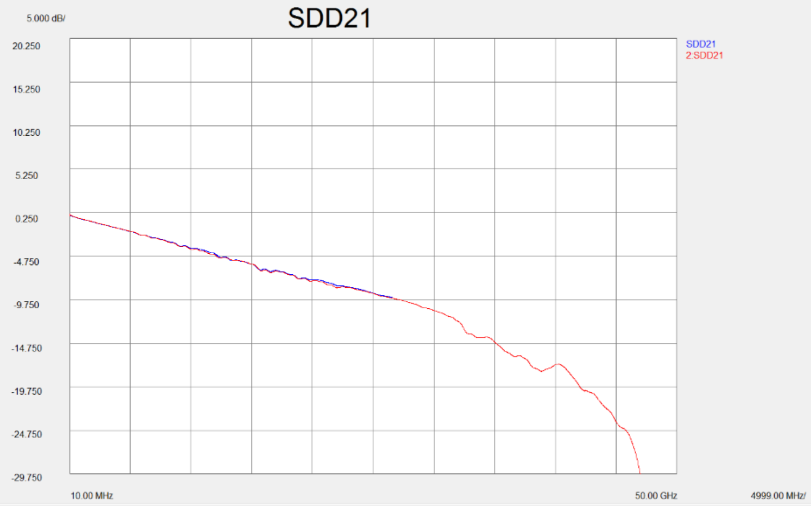
Round Robin Method of Building 12-port s-parameter

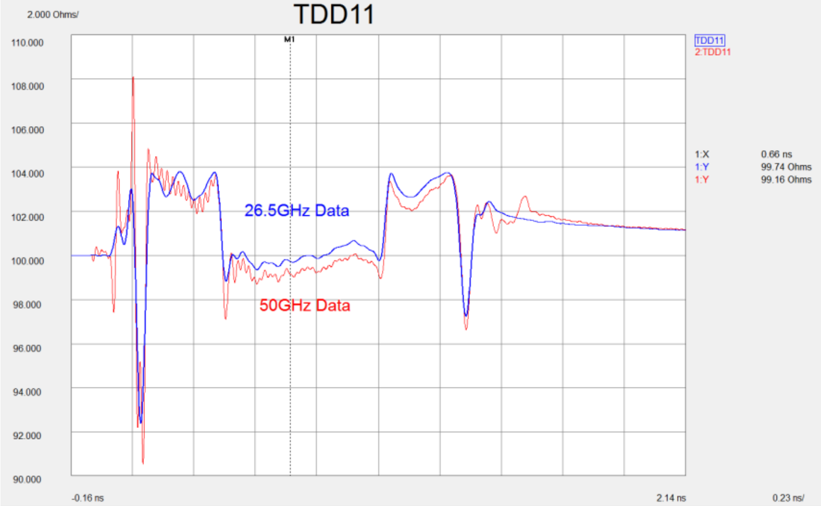




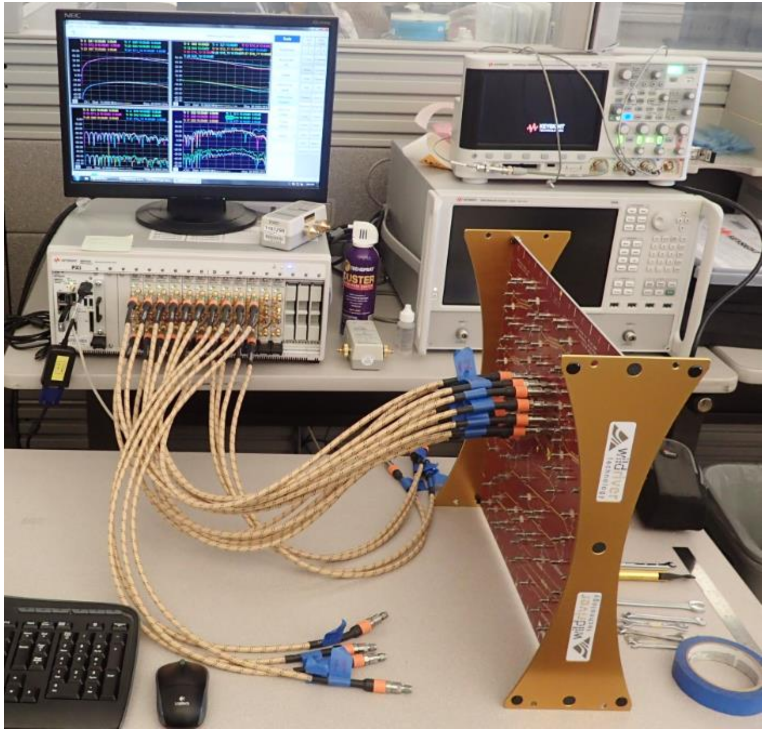
Round Robin Method of Building 12-port s-parameter

Comparison of 12-port 26.5GHz Measurement with 16 4-port 50GHz Measurements “Built Up”

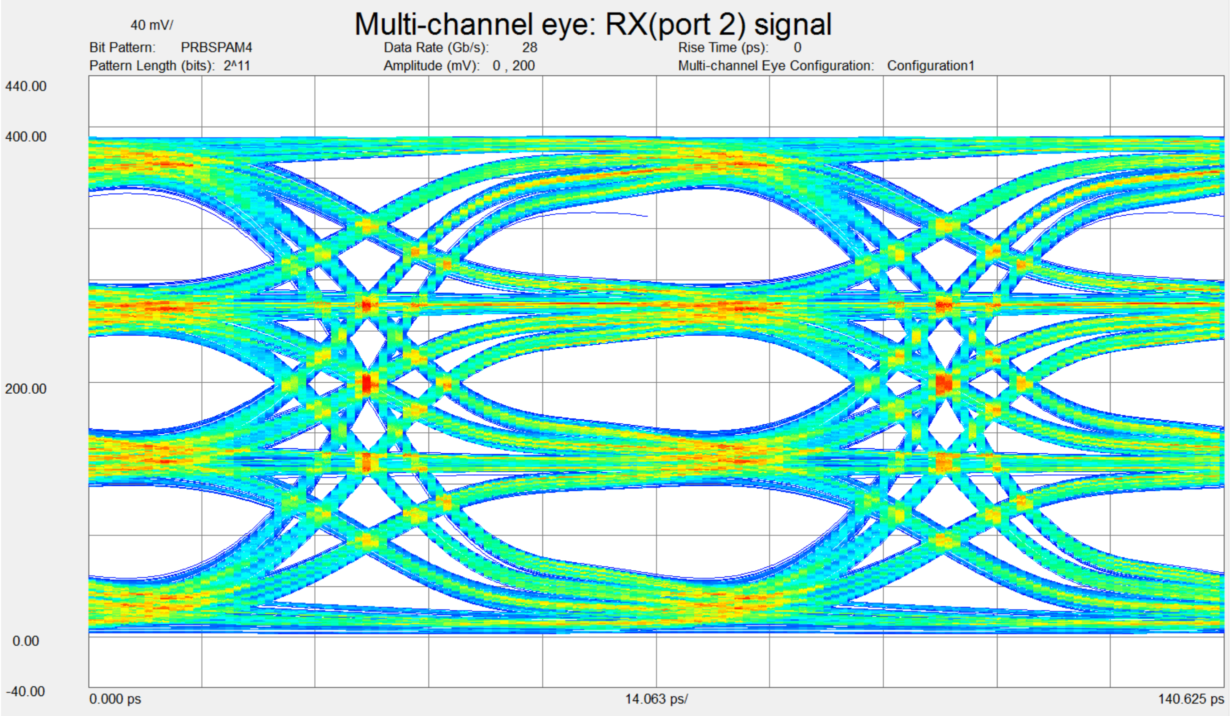




Test System with 26-port PXI-VNA @ 26.5GHz



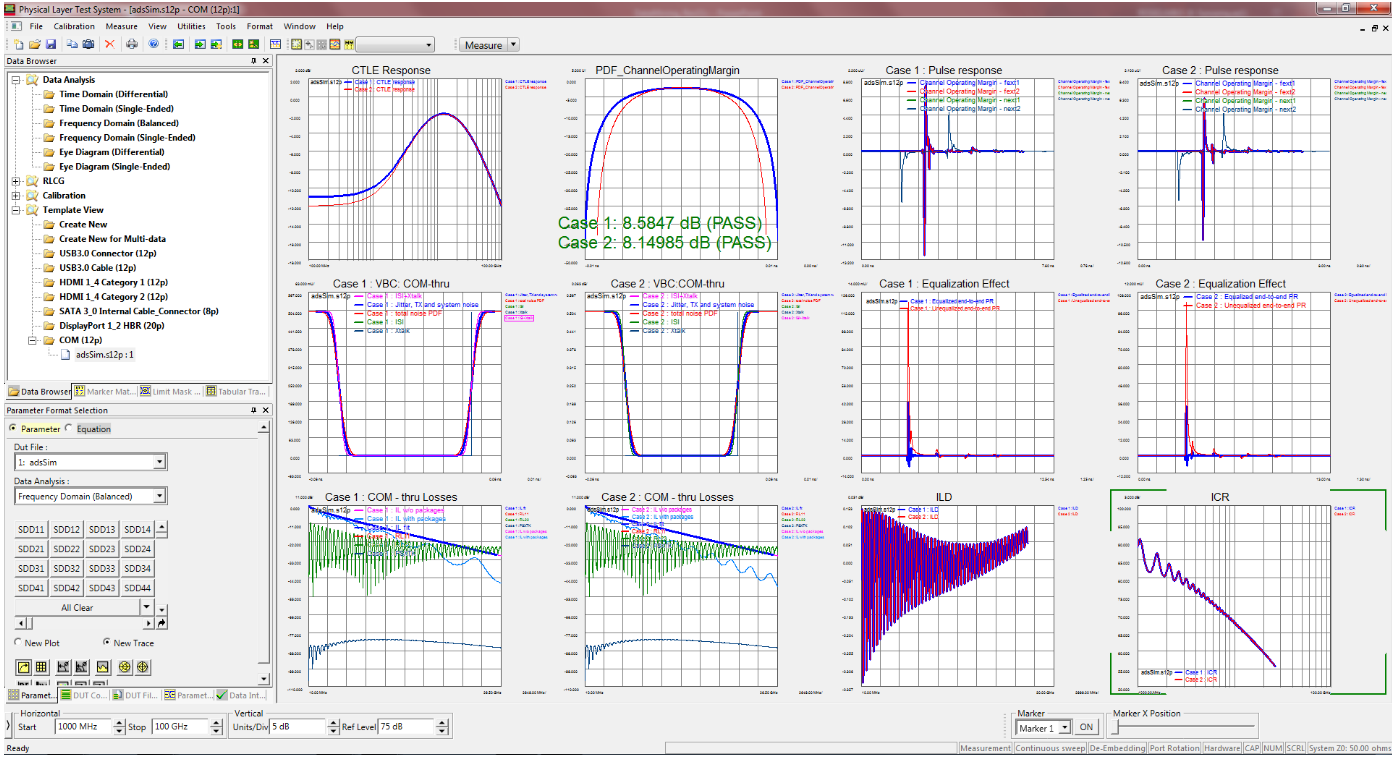
PAM-4 Eye Diagram



Channel Operating Margin (COM)

New Single Figure of Merit for Channel Analysis

- 100 GbE
- IEEE 802.3bj-2014
- Over 500 lines of MATLAB code
- User input required:
    - 12-port s-parameter
- COM test result:
    - Single number in decibels



What Did We Learn?

- New data visualization options are available today
- Standard 4-port s-parameters are no longer enough
- “Round Robin” methodology can save $$
- Mode conversion analysis can identify problems early
- PAM-4 and COM are now implemented in convenient tools

Resources

- PLTS 2017 Release: www.Keysight.com/find/plts
- Keysight booth # 1234
- Mike Resso: mike_resso@Keysight.com
- *“Signal Integrity Characterization Techniques”*, M. Resso and E. Bogatin, second printing 2015, International Engineering Consortium

Agenda

Heidi Barnes

SI/PI Apps. Engineer
Keysight Technologies

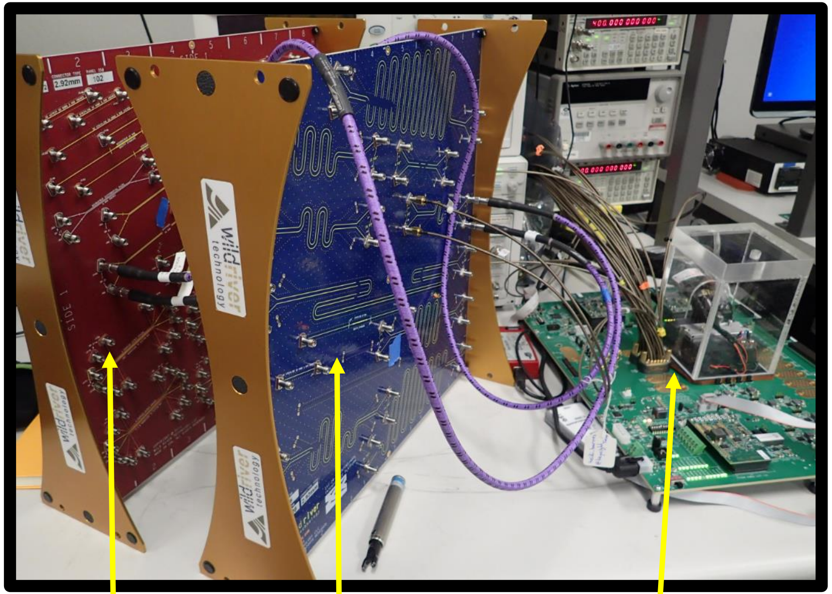
- Full-Link KR Example
- What is a “Pathological Channel”
- Measuring Pathological Channels
- Band Limited S-Parameters
- Using the Pulse Response to Gain Insight

- BREAK

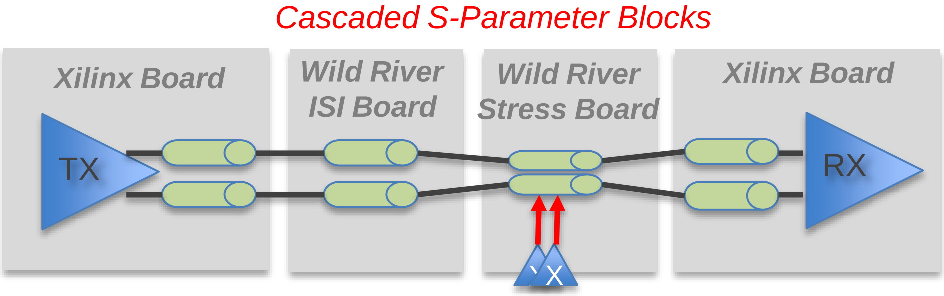
- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- Summary

Measuring Band Limited S-Parameters

Simulation requires a cascade of S-Parameters to analyze pathologies.

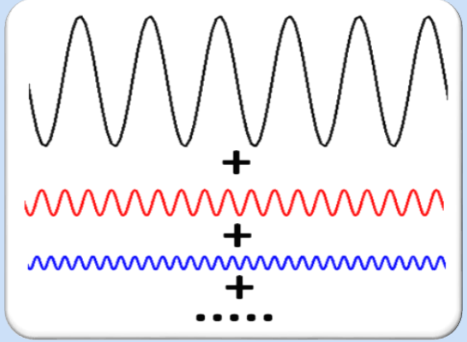


XTALK ISI Xilinx Board



S-Parameters are Transformed to the Time Domain

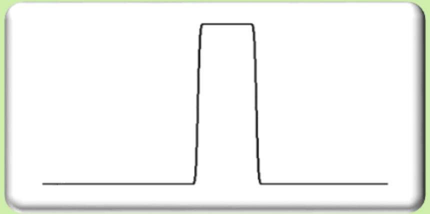
Frequency to Time Domain
Inverse Fourier Transform



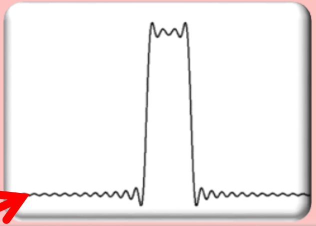
Summation of Sine Waves

=

Case 1
Infinite Sum of Sine Waves



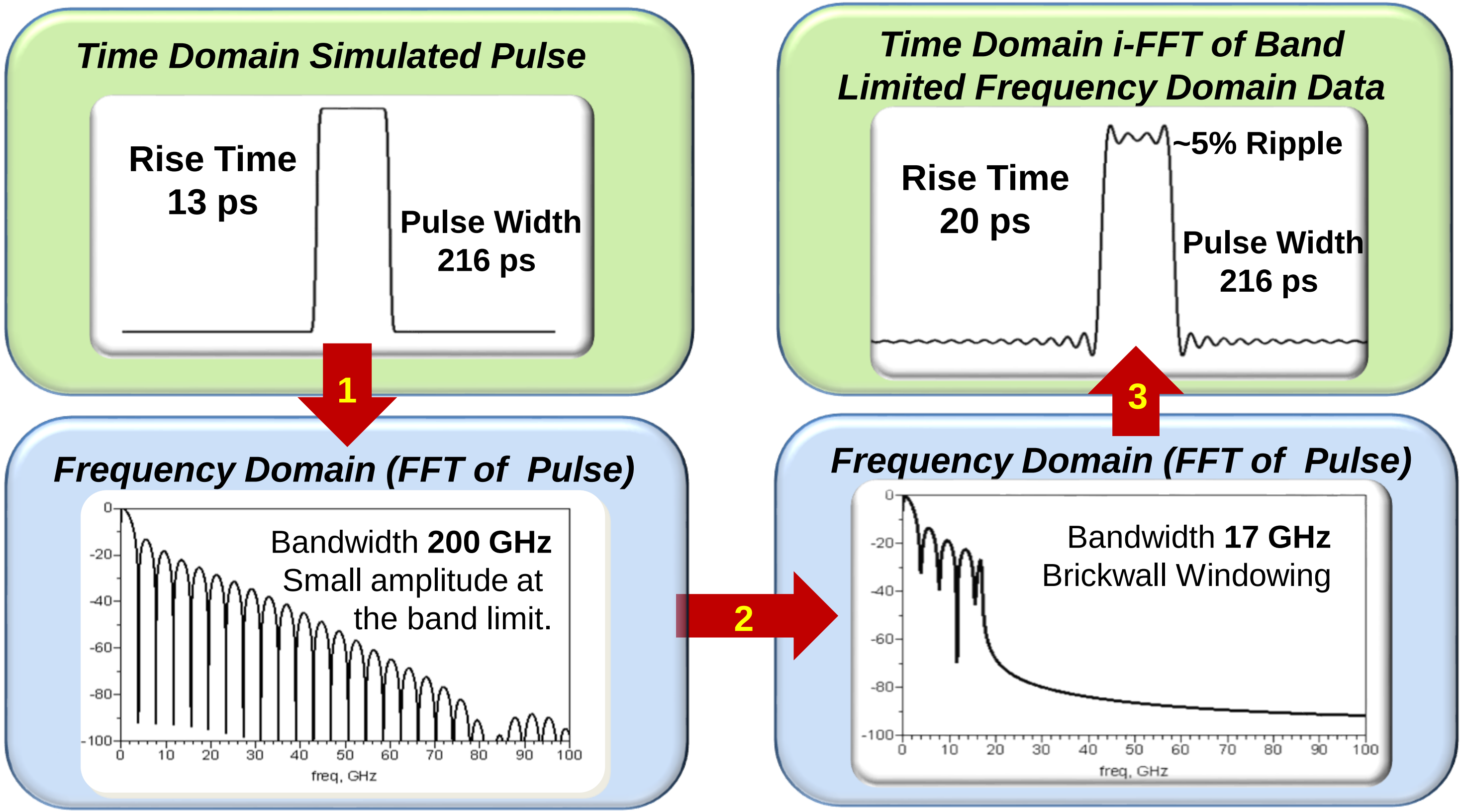
Case 2
Finite Sum of Sine Waves



Non-Causal Ripple - Gibbs Phenomena

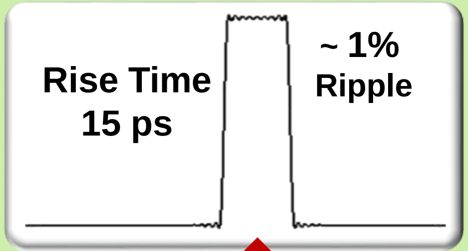
32 Gb/s Tx	Bandwidth Rule-of-Thumb
Rise Time 13 ps 10-80 step	17 GHz
Rise Time 5 ps 10-80 step	44 GHz
3rd Harmonic	48 GHz
5th Harmonic	74 GHz

Error Due to Gibbs Phenomena



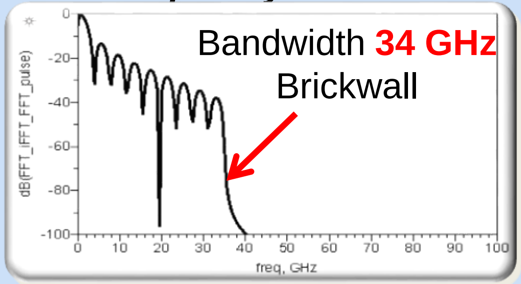
Required Channel Bandwidth

Time Domain
i-FFT of 34 GHz Band Limited Data

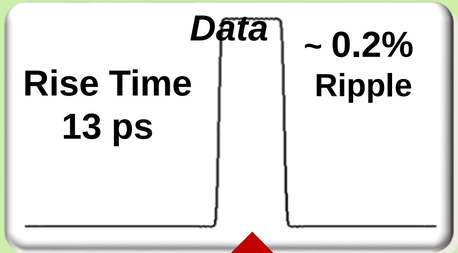


Inverse-FFT

Frequency Domain

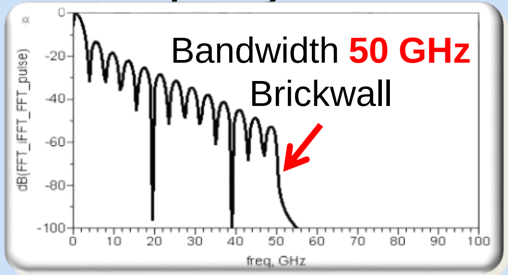


Time Domain
i-FFT of 50 GHz Band Limited Data



Inverse-FFT

Frequency Domain



Do the Rules of Thumb Really Help ?

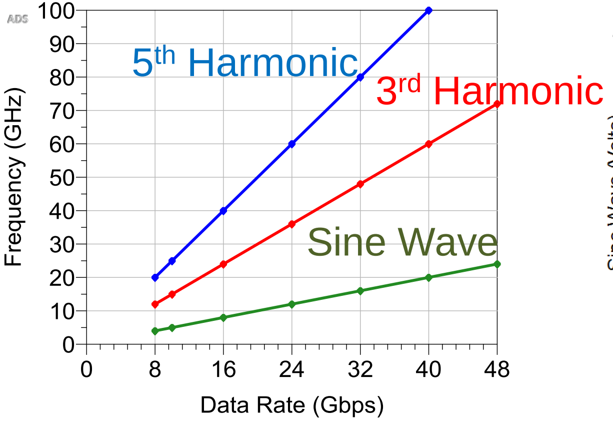
Bandwidth Square Wave
Harmonics

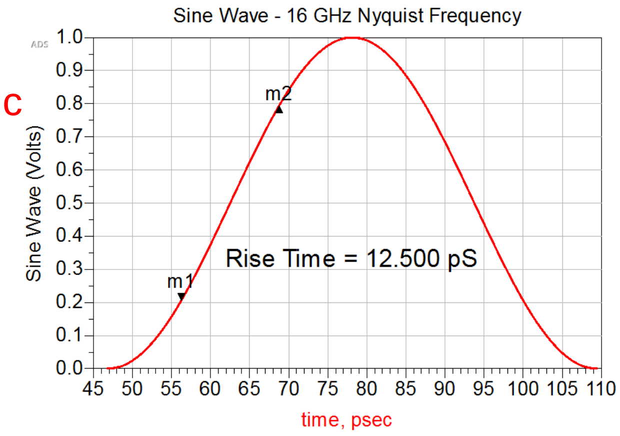
Rise Time Sine Wave

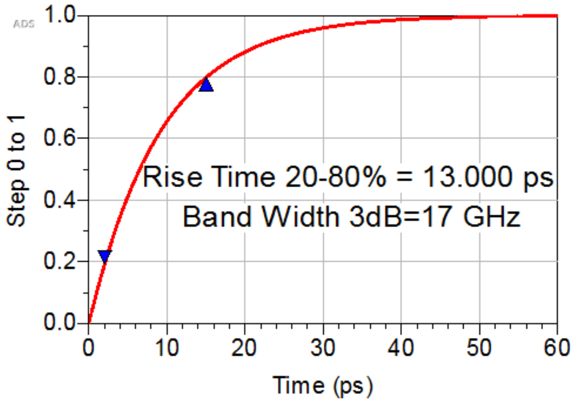
$$Frequency_{Nyquist} = \frac{0.2}{Rise\ Time_{(20\%\ to\ 80\%)}}$$

Bandwidth Step Response
RC Tank Circuit

$$Frequency_{3dB} = \frac{0.22}{Rise\ Time_{(20\%\ to\ 80\%)}}$$



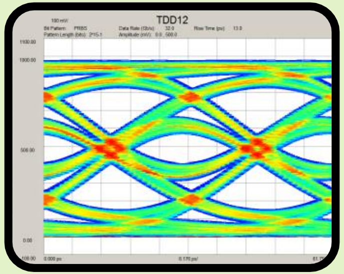


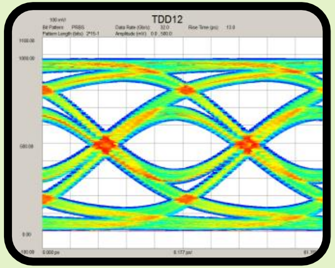


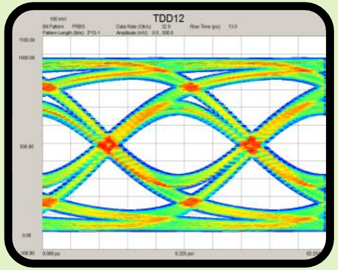
Simulated Eye Diagrams with Band-Limited S-Parameters

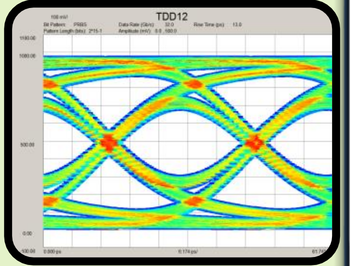
32 Gb/s , PRBS15, RT_10-80 13ps, Eye Diagrams

Inverse Fourier Transform with 4^{th} Order Bessel Windowing



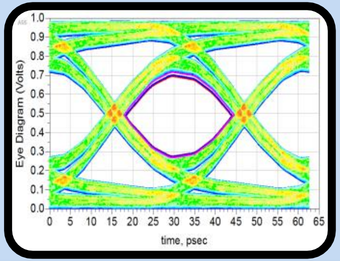


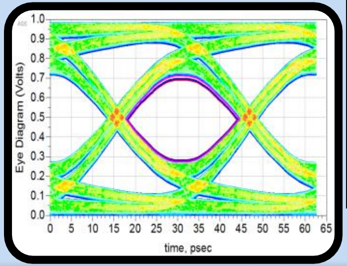


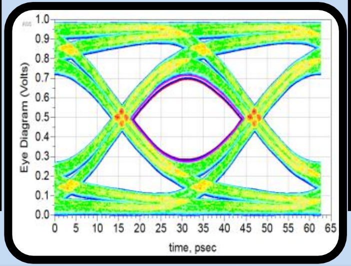


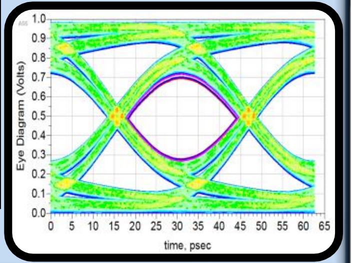
Bandlimited 24 GHz S-Parameters	Bandlimited 32 GHz S-Parameters	Bandlimited 40 GHz S-Parameters	Bandlimited 48 GHz S-Parameters

Hilbert Transform with Causality Enforcement









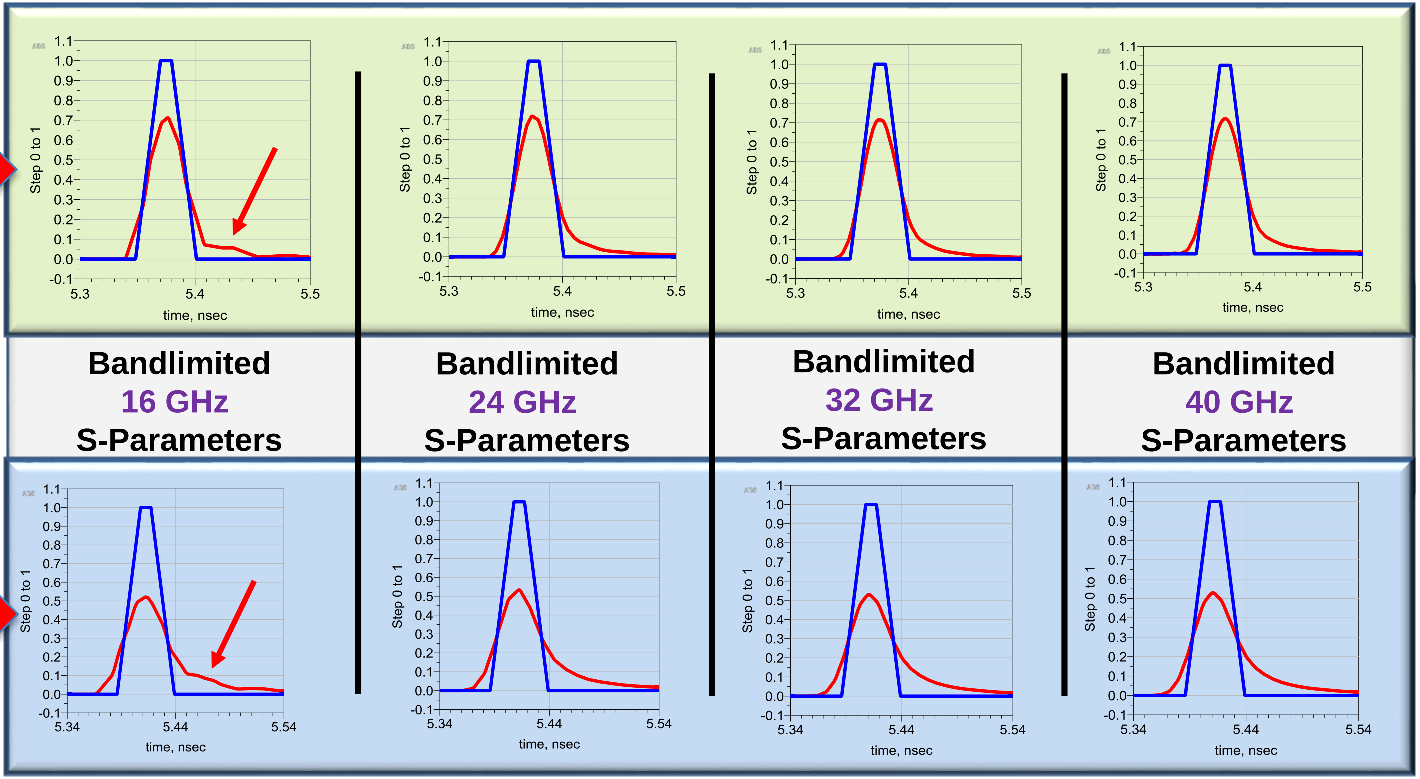
Comparing Single Symbol Response

Single Pulse Response Highlights the Impact of Band Limited S-Parameters

13pS Rise Time Transmitter with single 4.5 inch ISI Channel

Hilbert Transform with Causality Enforcement

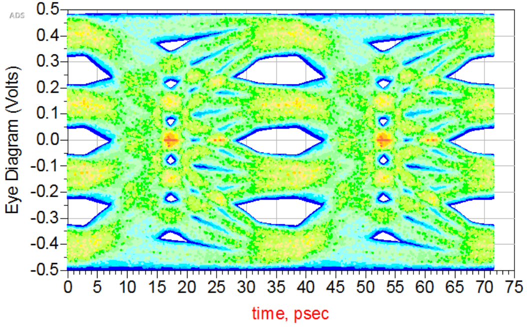
13pS Rise Time Transmitter with 9 inch ISI Channel

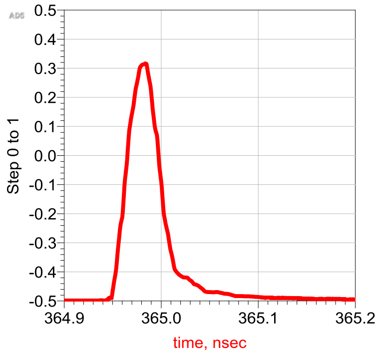


And for 56 GBaud PAM-4

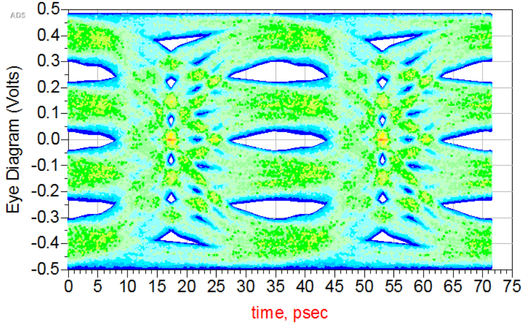
13pS Rise Time Transmitter with single 4.5 inch ISI Channel, PRBS15, No Equalization

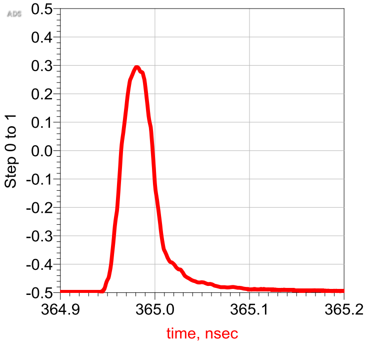
Bandlimited
24 GHz S-Parameters



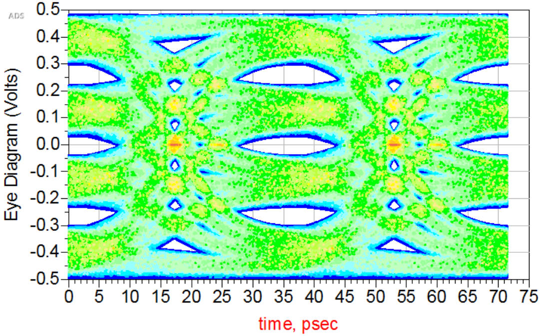


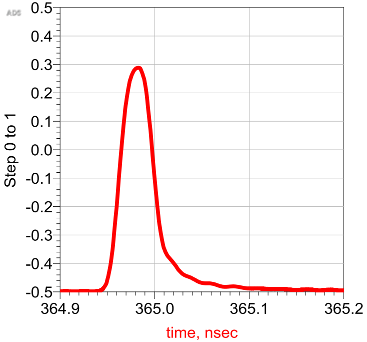
Bandlimited
32 GHz S-Parameters





Bandlimited
48 GHz S-Parameters





Hilbert Transform with Causality Enforcement

Conclusion for Lossy Channels

- S-Parameters are always “band limited”
- 3rd Harmonic is conservative
- Rise time estimate is not enough when rise time>¼ UI

$$Frequency_{3dB} = \frac{0.22}{Rise\ Time_{(20\%\ to\ 80\%)}}$$

- Simulation algorithms are not all the same!
- Verify with simulation is the best method

References

- Jack Carrel, et al. “De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement” DesignCon 2014.
- Colin Warwick, “Understanding the Kramers-Kronig Relation Using A Pictorial Proof” Agilent Technologies, Inc. 2010, White Paper 5990-5266EN.
- Eric Bogatin, *Signal Integrity - Simplified*, Chapter 7; Prentice Hall, 2003 (ISBN 0-13-066946-6).

- www.keysight.com/find/eesof-sipi-resources

Agenda

Tim Wang Lee

Signal Integrity Consultant,
Wild River Technologies,
University of Colorado
timwanglee@gmail.com

- Full-Link KR Example
- What is a "Pathological Channel"
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- BREAK

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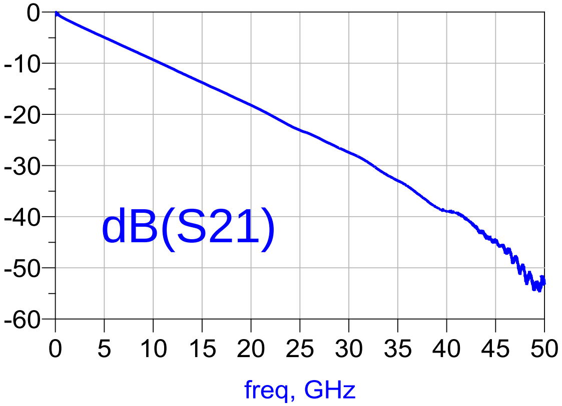
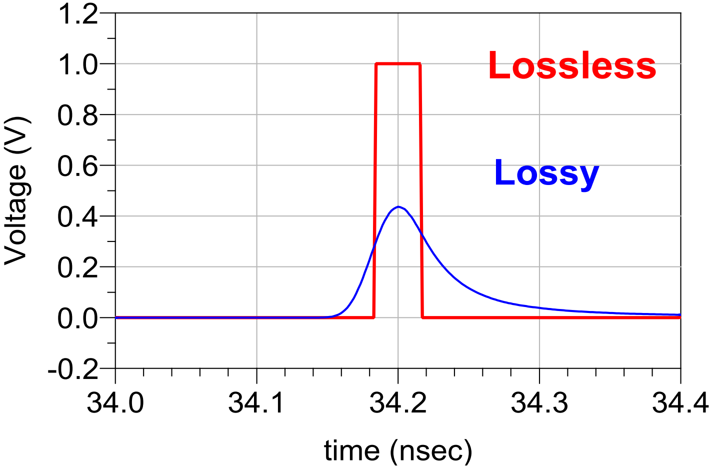
Using Single Pulse Response to Gain Insight of the Channel

- Tim Wang Lee, Wild River Technologies

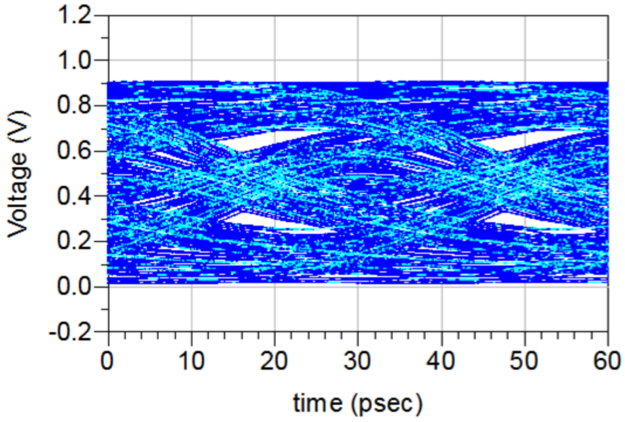
Frequency Domain



Single Pulse Response of a Channel



Time Domain



The Impulse Response Characterizes a Channel

Stimulus

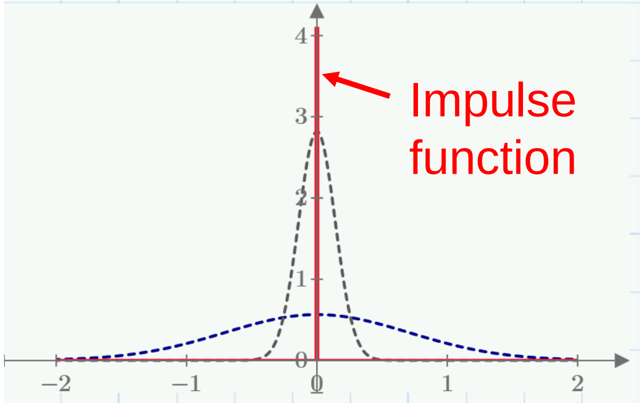
Input: x(t)

Linear Time-Invariant

Response

Output: y(t)

Dirac delta distribution*



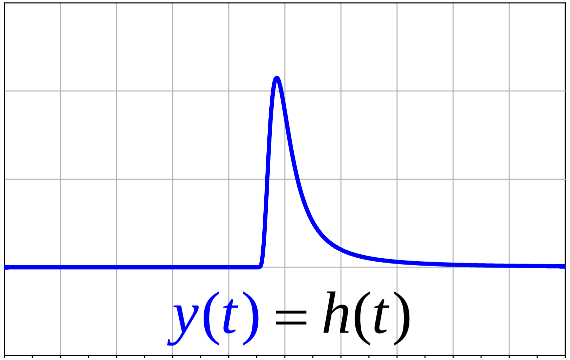
Channel: h(t)

$$y(t) = x(t) * h(t)$$

$*$: Convolution operator

In an LTI system, the **impulse response** characterizes the system **completely.**

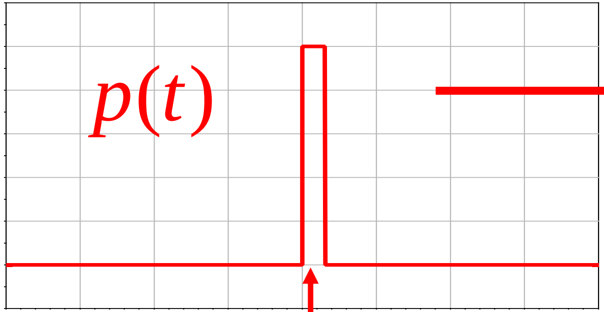
Impulse Response of the channel



*Dirac, Paul (1958), The Principles of Quantum Mechanics (4th ed.), Oxford at the Clarendon Press, ISBN 978-0-19-852011-5.

The Single Pulse Response of a Channel

Single **pulse** function



$$width_{pulse} = \frac{1}{\text{data rate}}$$

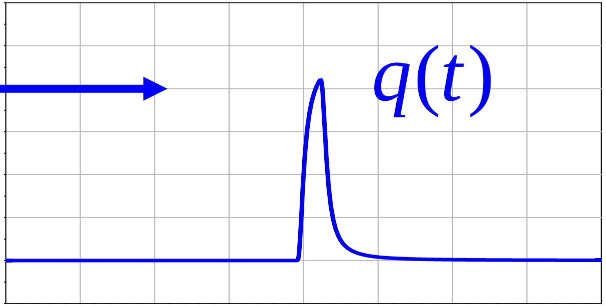
Pulse height: depends (NRZ/PAM4)

When using NRZ, the response is the single **Bit** response.

Linear Time-Invariant

Channel: h(t)

Single **Pulse** Response



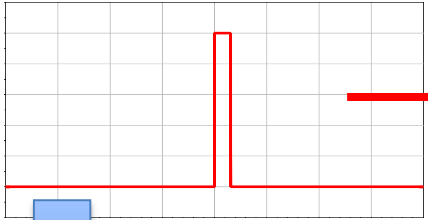
$$q(t) = p(t) * h(t)$$

Single pulse response properties:

- Is a deconstructed eye.
- Shows effect of equalization.
- Gives insights to reflection and crosstalk.
- Helps characterize frequency-dependent loss .

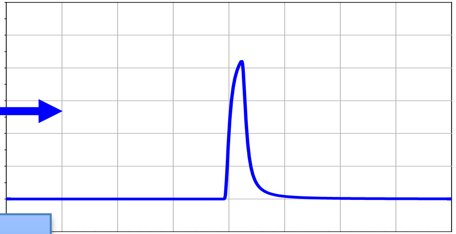
Frequency Spectrum of the Single Pulse

Single **pulse** function

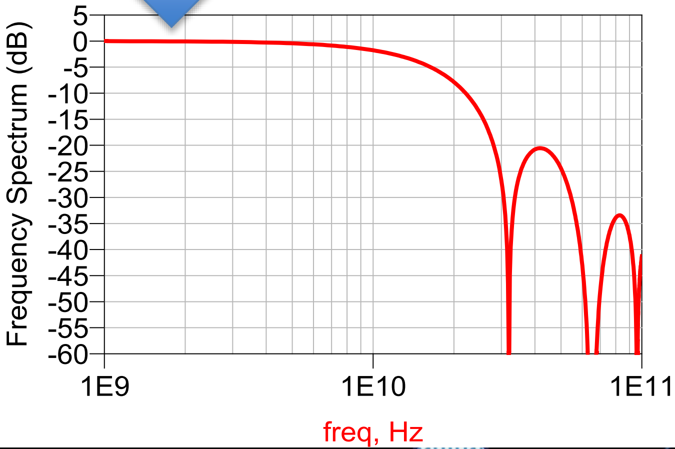


Linear Time-Invariant

Single **pulse** Response



Fourier Transform

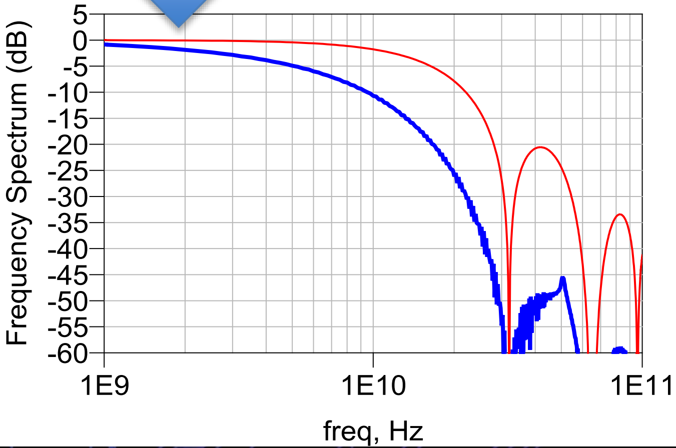


Channel: h(t)

Investigate on different loss mechanisms:

- Conductor loss
- Dielectric

Fourier Transform

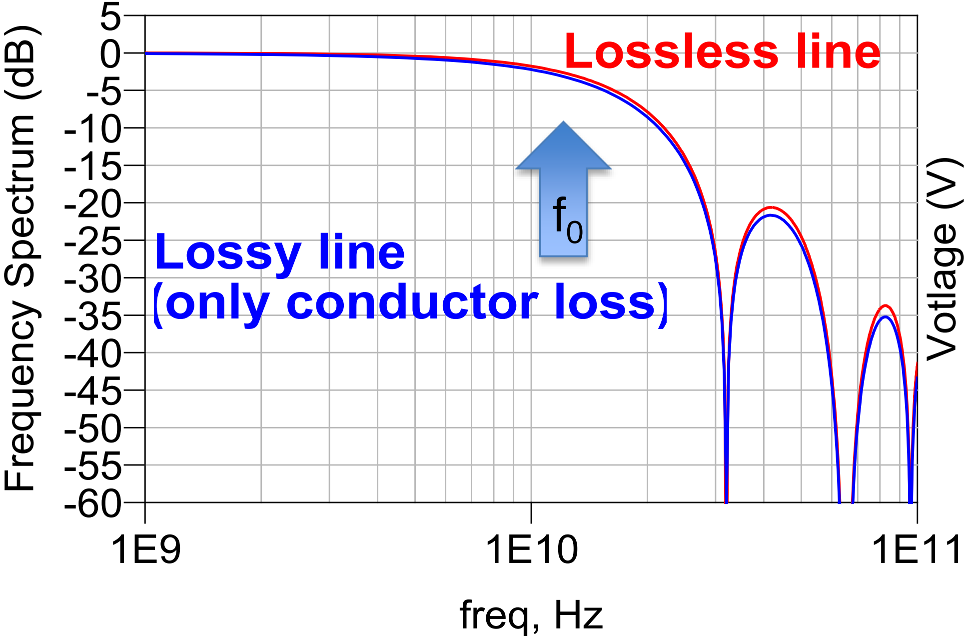


Single Pulse Response Conductor Loss Signature

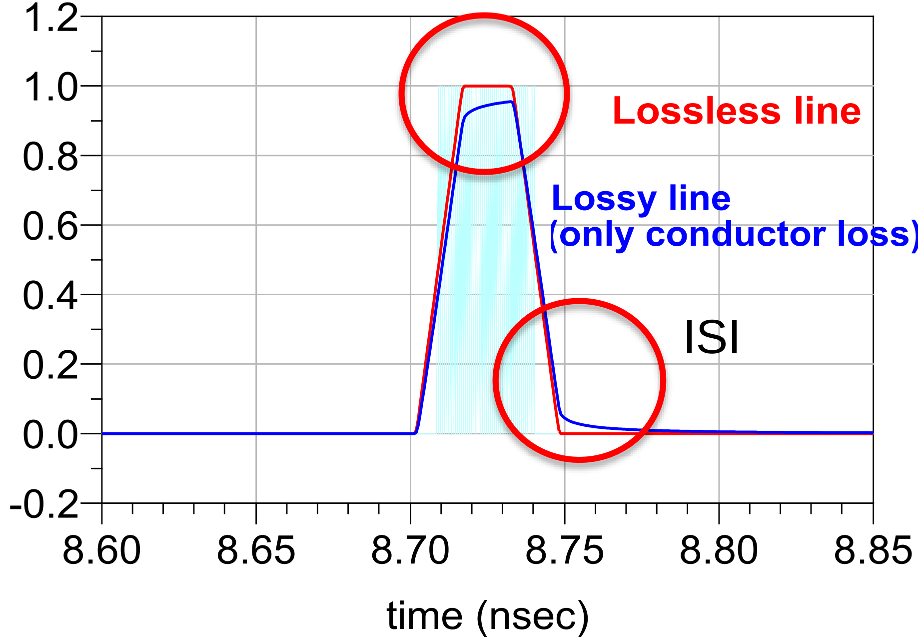
TX: 32 Gbps (f_0=16 GHz), Rise Time: 15 psec

T-Line: 5 inch, microstrip FR4 50 Ohm (w = 20 mil)

$$Loss_{cond} \approx \frac{len\,(\text{inch})}{w\,(\text{mil})}\sqrt{f} = 1\,\text{dB}\Big|_{16\text{ GHz}}$$



Pulse Response vs. Cond. Loss



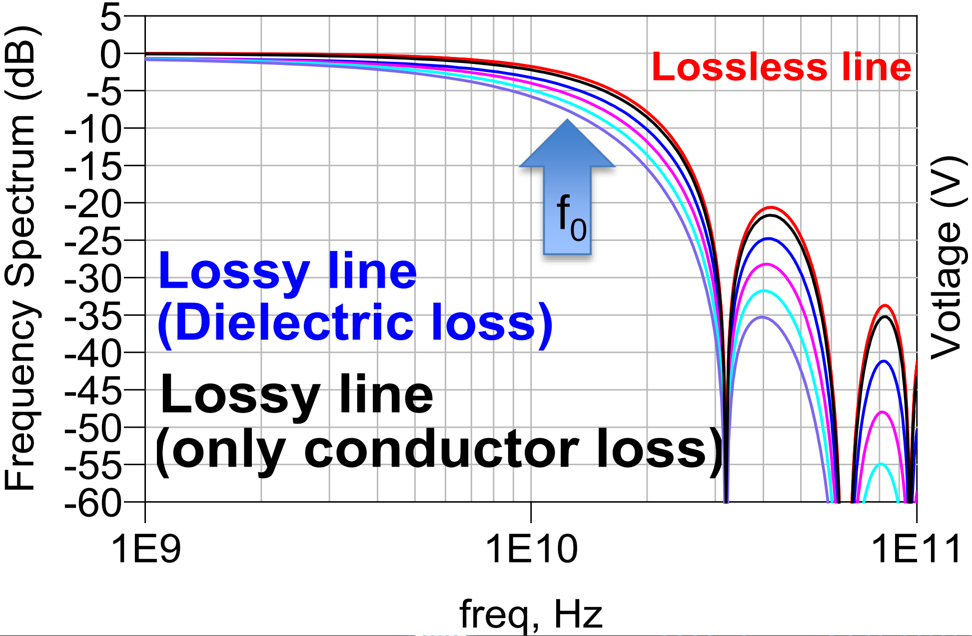
http://www.edn.com/electronics-blogs/all-aboard-/4429778/Loss-in-a-channel--Rule-of-Thumb--9

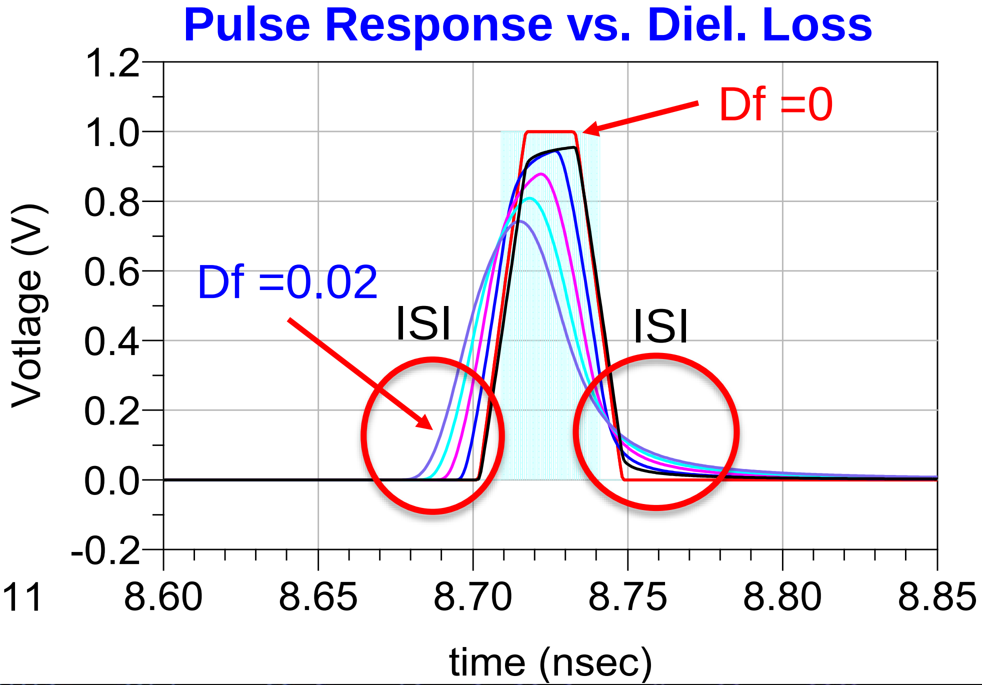
Single Pulse Response Dielectric Loss Signature

TX: 32 Gbps (f_0=16 GHz), Rise Time: 15 psec
T-Line: 5 inch, microstrip FR4 50 Ohm (Dk = 4)
Df = 0~0.02, 0.05 step.

$$Loss_{diel} \approx len \cdot f(GHz) \cdot 2.3 \cdot Df \cdot \sqrt{Dk}$$

$$Loss_{diel} \approx 7.36\ \mathrm{dB}\Big|_{16\,GHz,\,Df=0.02}$$

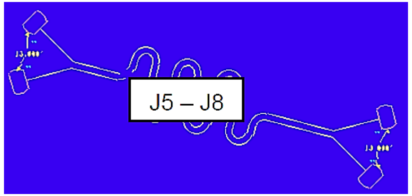




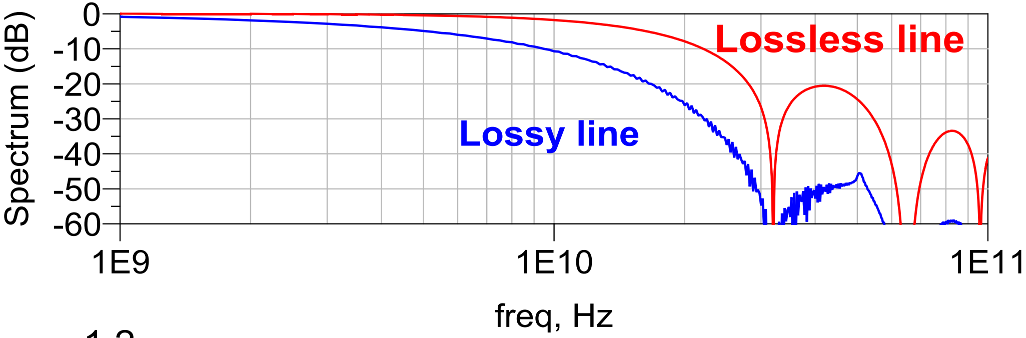
http://www.edn.com/electronics-blogs/all-aboard-/4429778/Loss-in-a-channel--Rule-of-Thumb--9

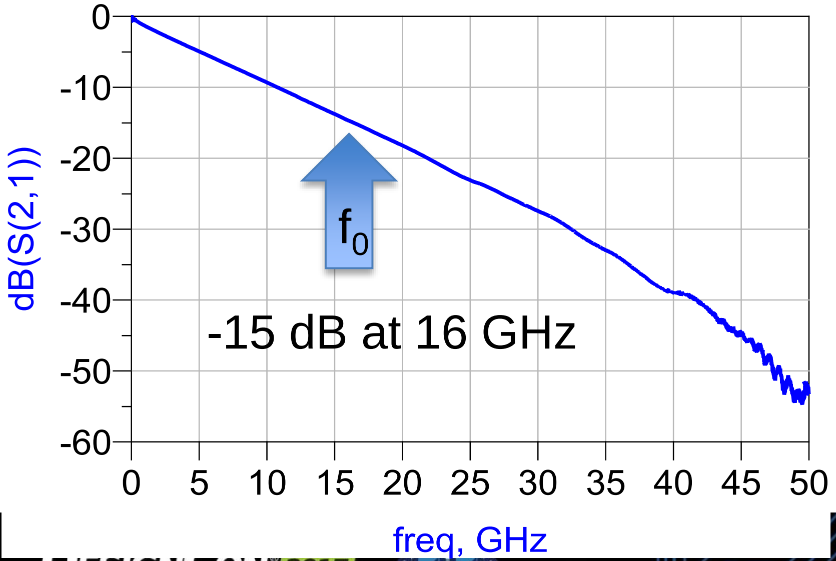
Single Pulse Response Example with WRT ISI-32

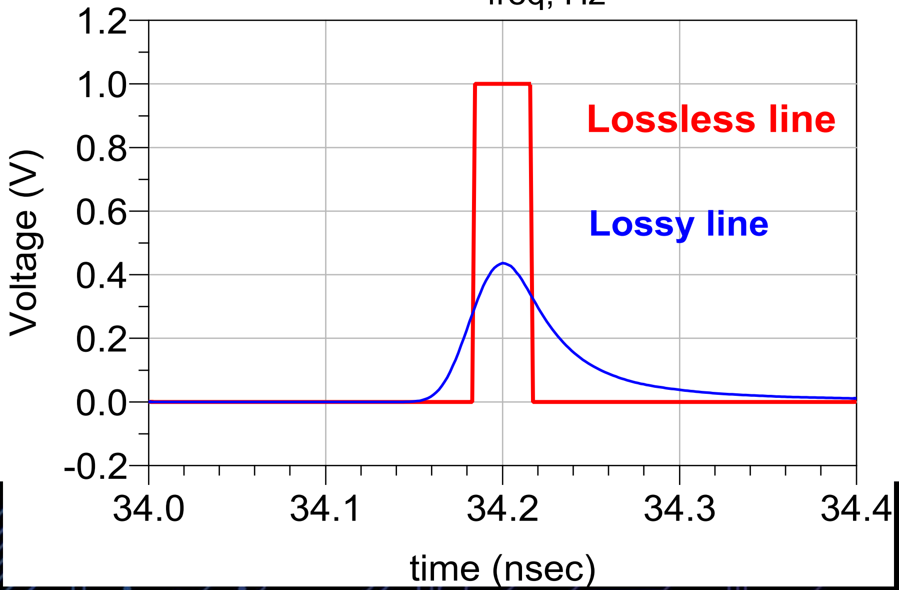
ISI 13-inch channel



Rule of thumb:
loss~ 0.1 dB/inch/GHz
Expect: ~16dB at 16GHz





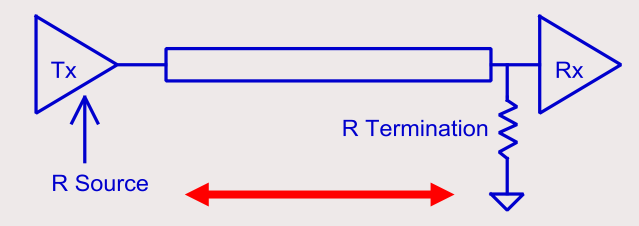


Single Pulse Response Mismatch Signatures

TX: 32 Gbps, Rise Time: 15 psec
T-Line: 1 inch, microstrip FR4
50 Ohm, lossless
UI: 31.25 psec

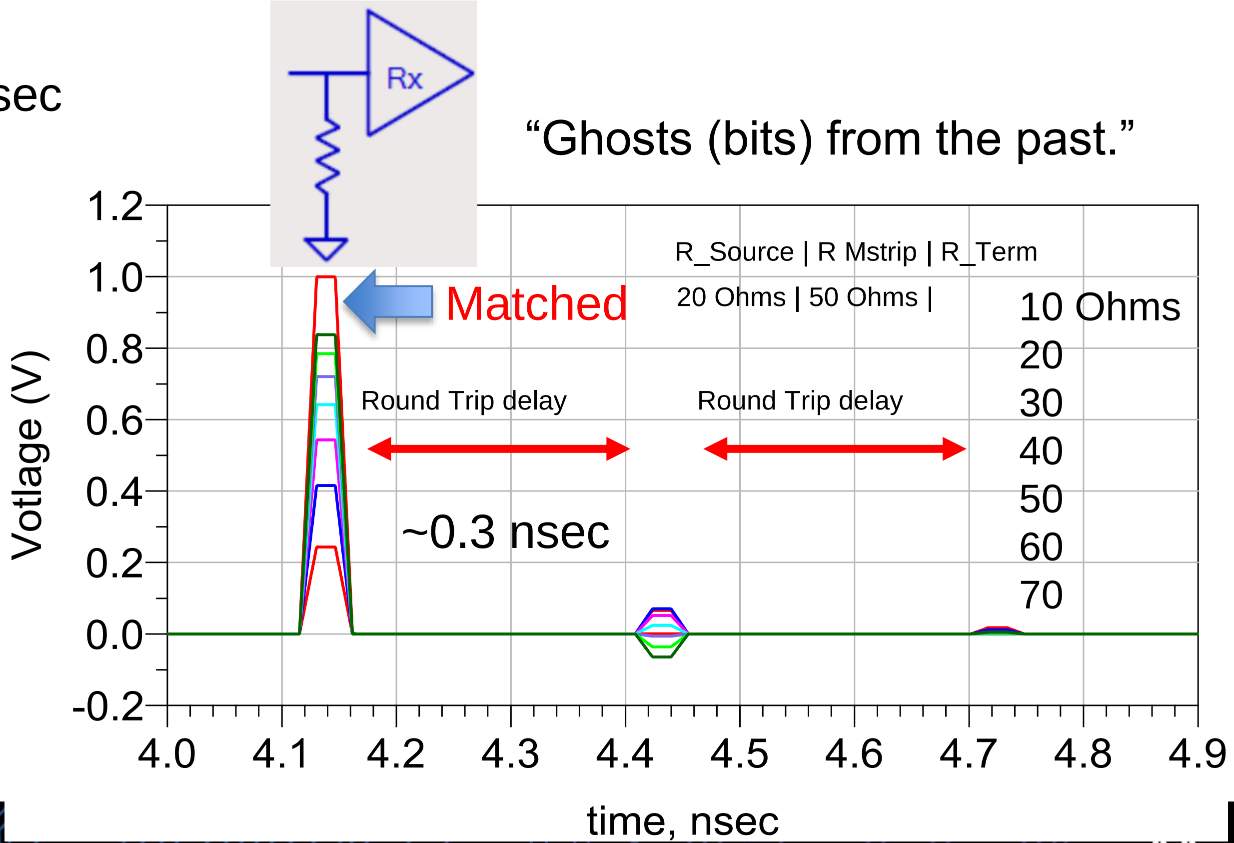
R_Source | R Mstrip | R_Term

20 Ohms | 50 Ohms | 10~70 Ohm

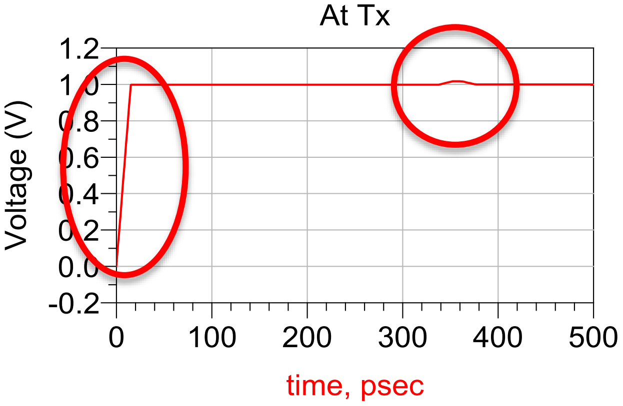


One way delay = ~ 0.167 nsec
Round Trip delay = ~ 0.33 nsec

“Ghosts (bits) from the past.”

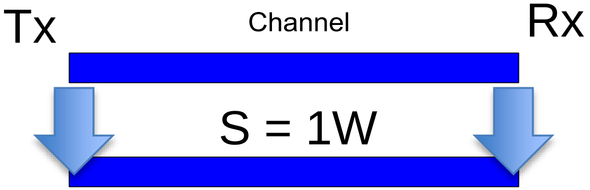


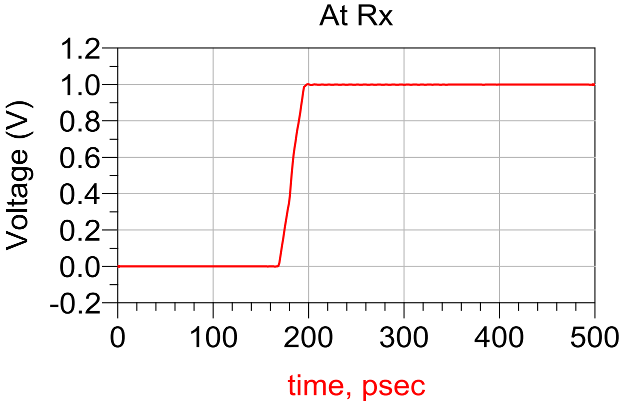
Examine Single-ended Crosstalk With Step Response

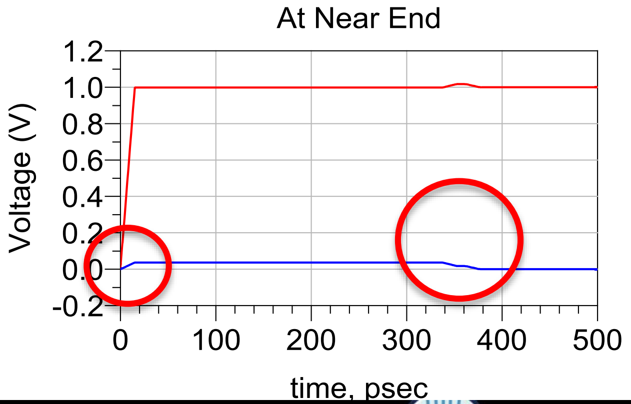


T-Line: 1 inch, microstrip
FR4, 50 Ohm, lossless

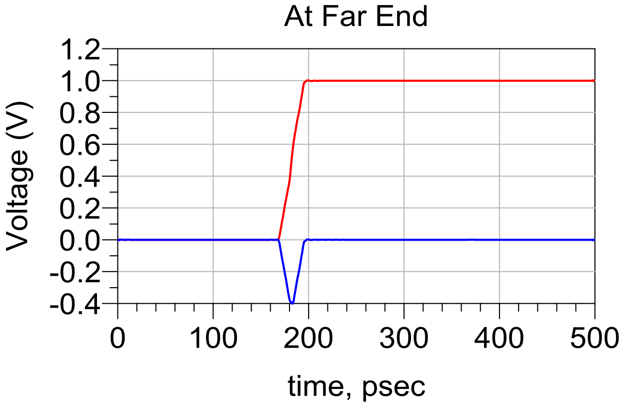
One way delay ~0.167 nsec



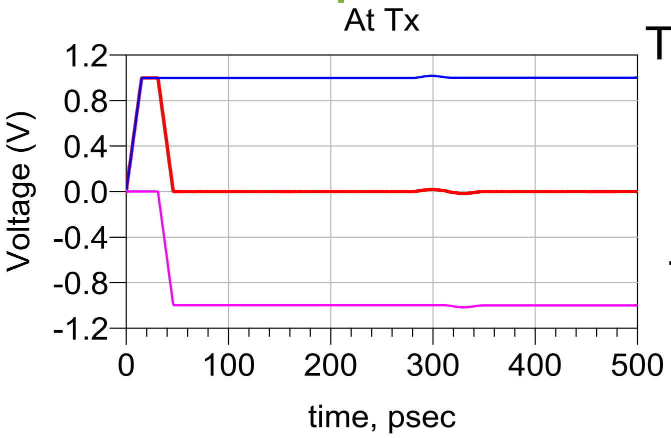




Lenz's Law: induced current opposes the change of current

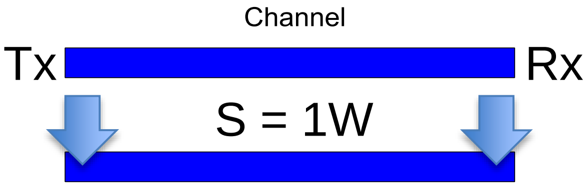


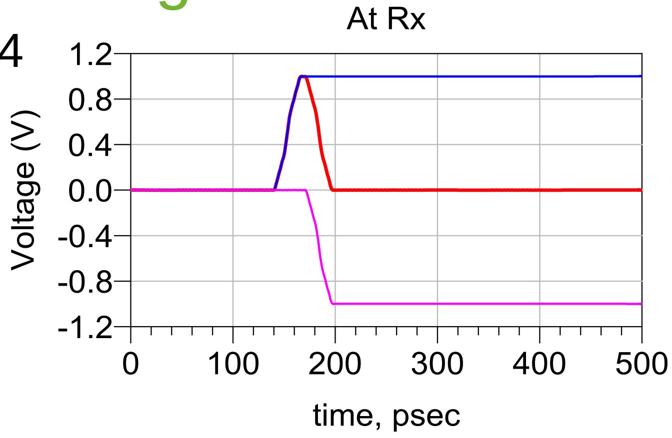
Two Steps Make a Single Pulse Crosstalk Signature



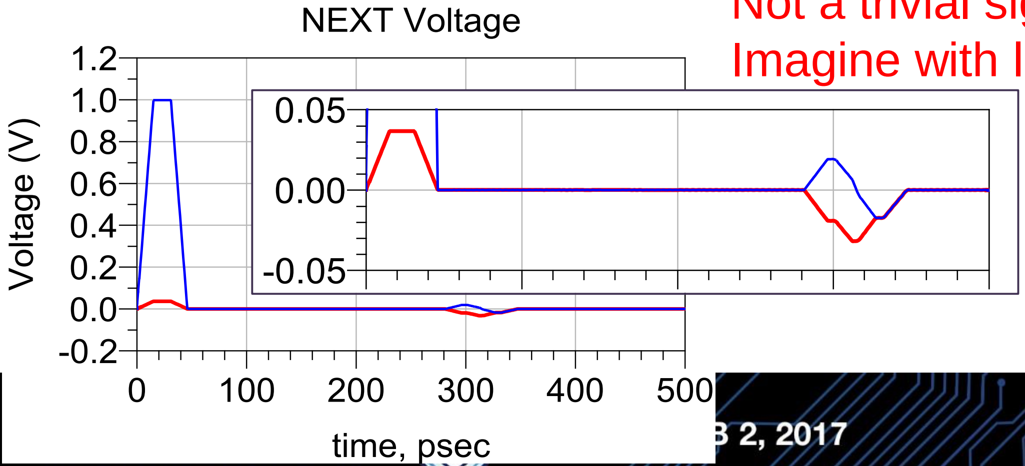
T-Line: 1 inch, microstrip FR4
50 Ohm, lossless

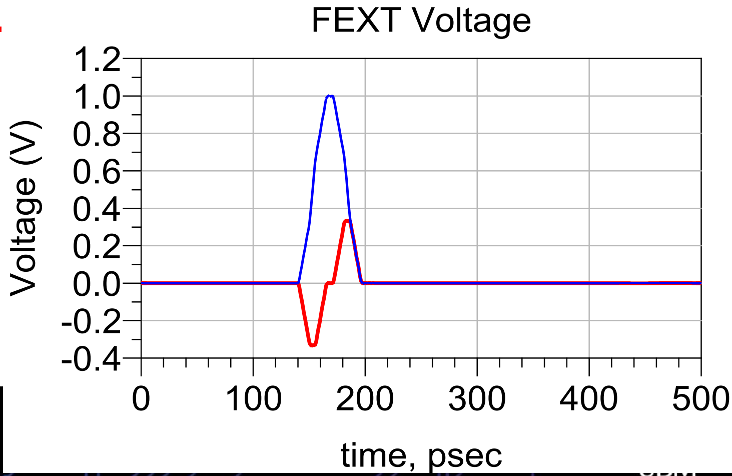
Single-ended channel



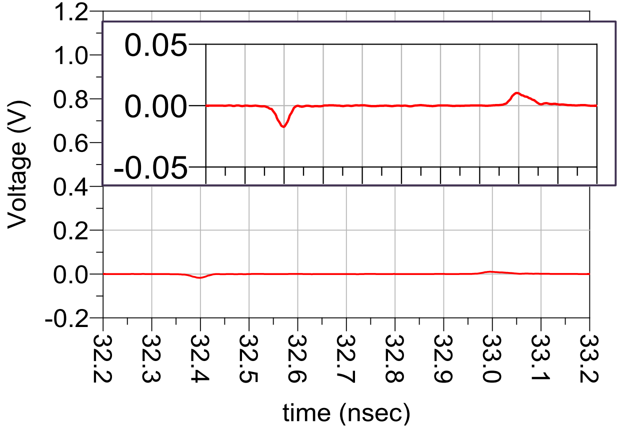


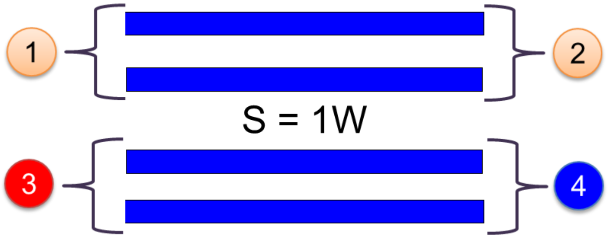
Not a trivial signature.
Imagine with loss.

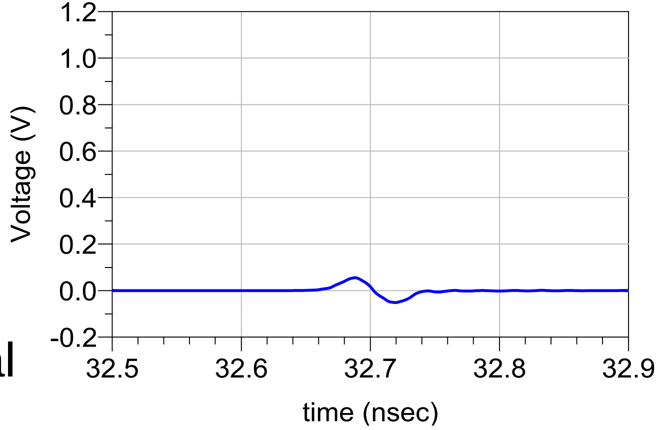




Single Pulse Response Example: WRT XTALK-32

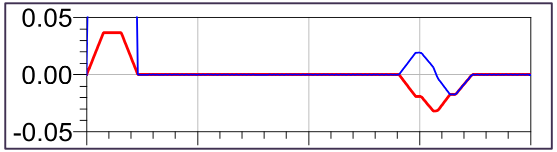






The general shape is identical to what we expected, but not the sign. Why?

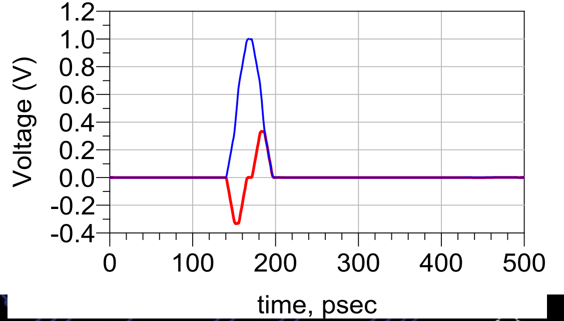
Expectation



Differential signaling!

We learn a lot more by exercising engineering knowledge and safe simulation.

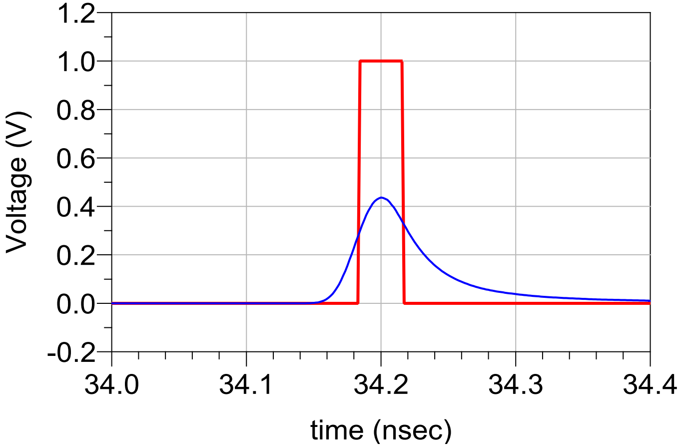
Expectation

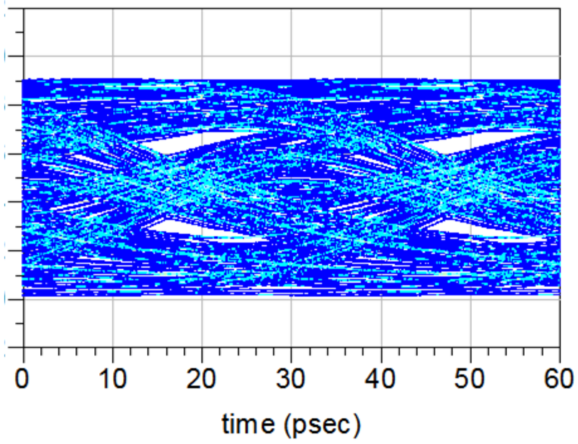


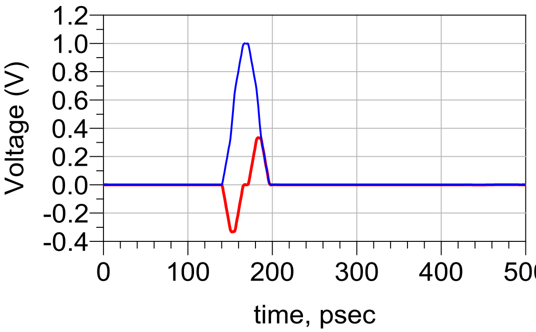
Summary on Single Pulse Response

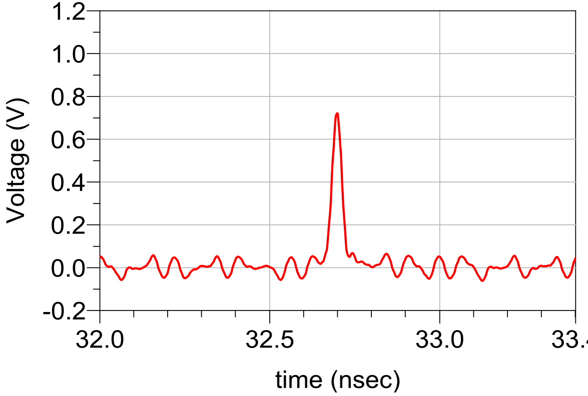
Single **Pulse** Response

(NRZ: Single **Bit)**









- Gives quick insight to the resulting eye.
- Identifies loss, mismatch and mismatch.
- Understand the effect of different equalization.

Resources

- Wild River Technologies
  - Booth #850
- Impulse response and signal integrity
  - S.H. Hall and H.L. Heck, Advanced Signal Integrity for High-Speed Digital Designs (2009).
- Impulse response and linear system
  - Dennis Freeman. *6.003 Signals and Systems.* Fall 2011. Massachusetts Institute of Technology: MIT OpenCourseWare, https://ocw.mit.edu. License: Creative Commons BY-NC-SA.

Agenda

- Full-Link KR Example
- What is a “Pathological Channel”
- Measuring Pathological Channels
- Band Limited S-Parameters
- Using the Pulse Response to Gain Insight

- **BREAK**

- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- Summary

Agenda

Tim Wang Lee

Signal Integrity Consultant,
Wild River Technologies,
University of Colorado
timwanglee@gmail.com

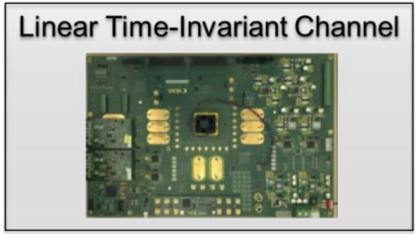
- Full-Link KR Example
- What is a "Pathological Channel"
- S-Parameter Data Mining
- Measuring Band Limited S-Parameters
- Using the Single Pulse Response to Gain Insight

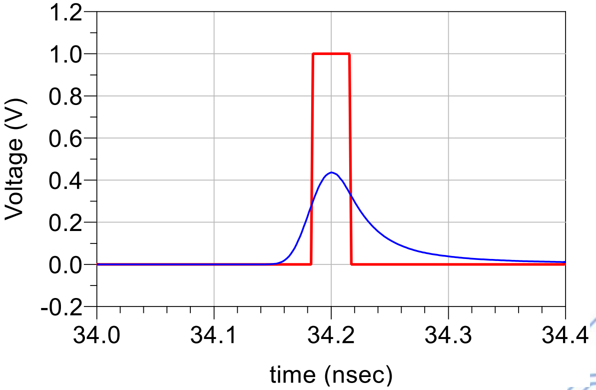
- BREAK

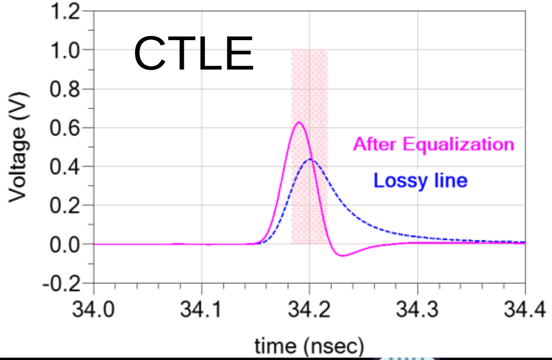
- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Strategies for managing Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- Conclusion

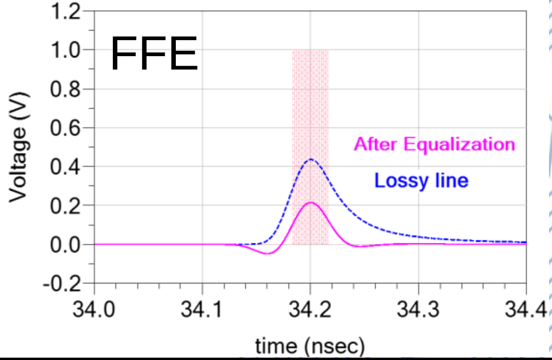
Single Pulse Response and Equalization

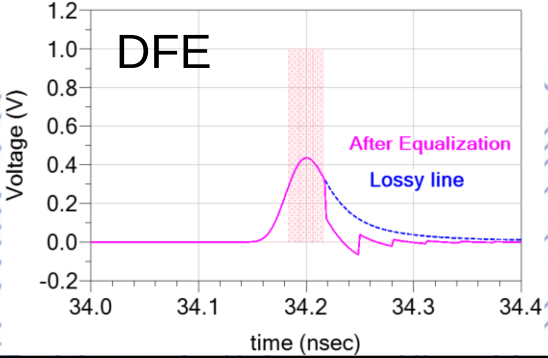
Tim Wang Lee, Wild River Technologies



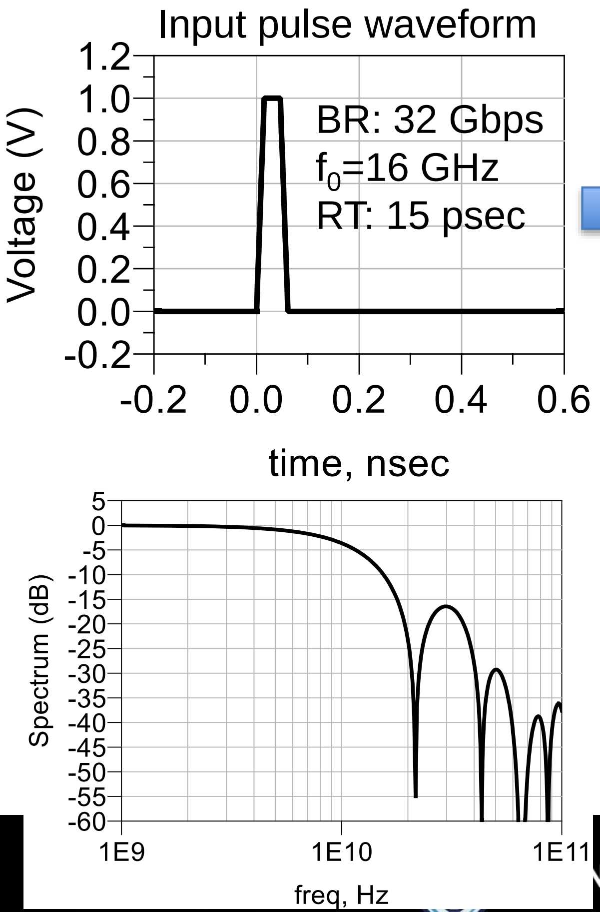




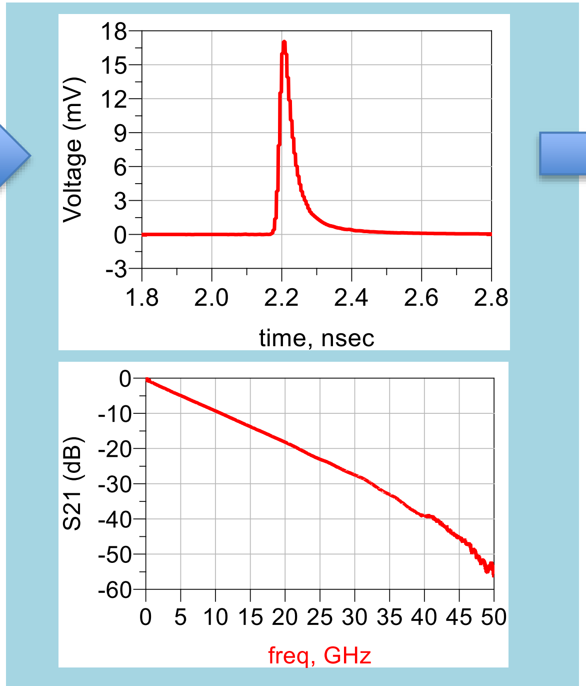


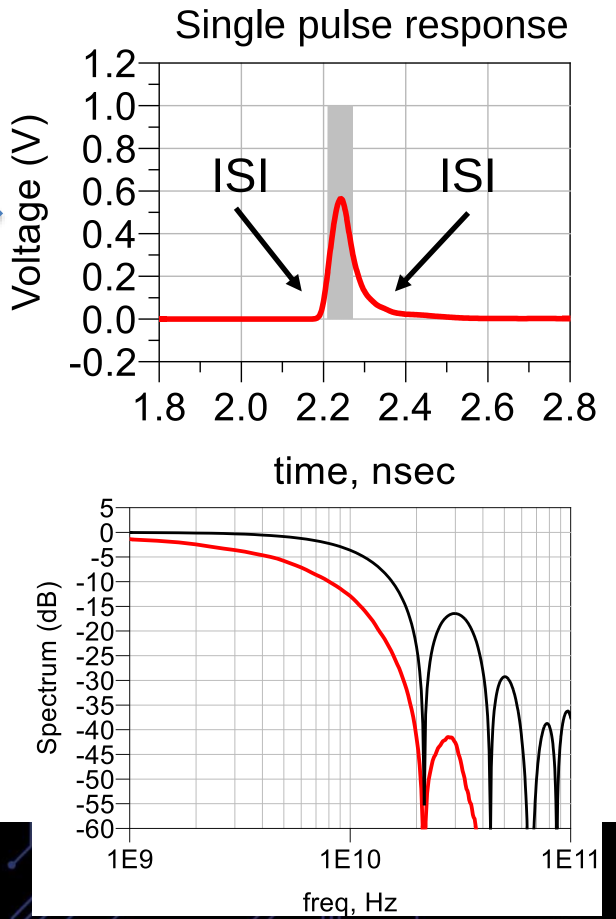


Looking at a Real Channel, ISI and the Root Cause



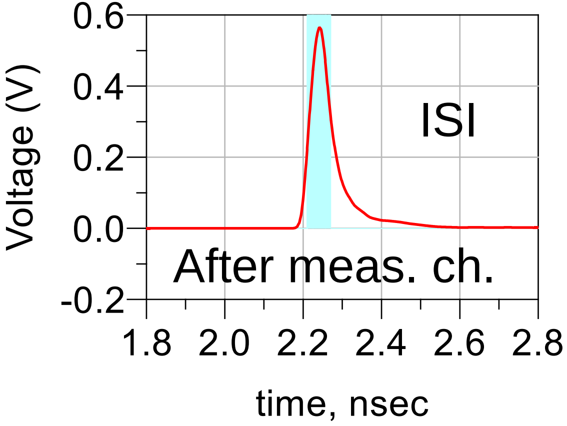
A 13 inch stripline channel

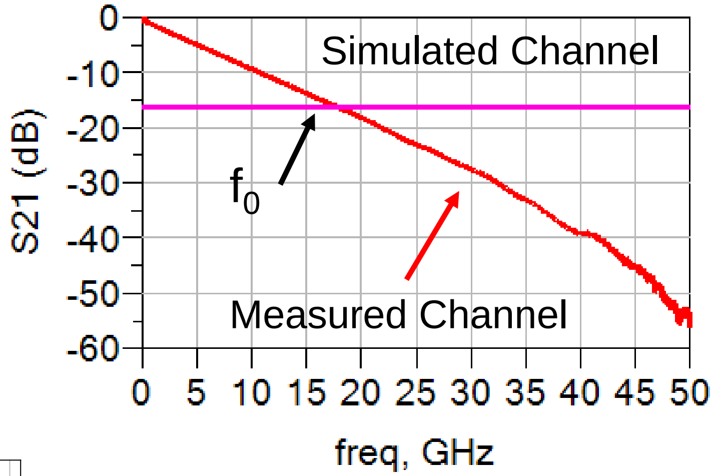


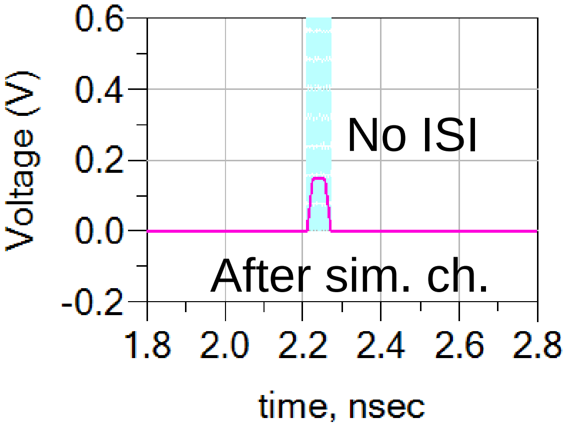


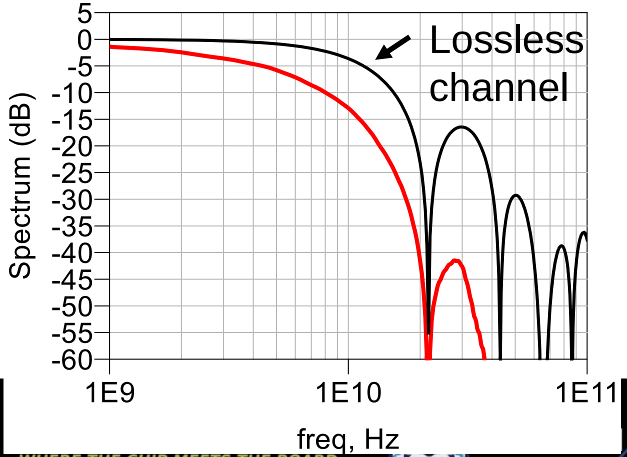
What's the root cause of ISI?

Frequency-dependent Loss Causes ISI

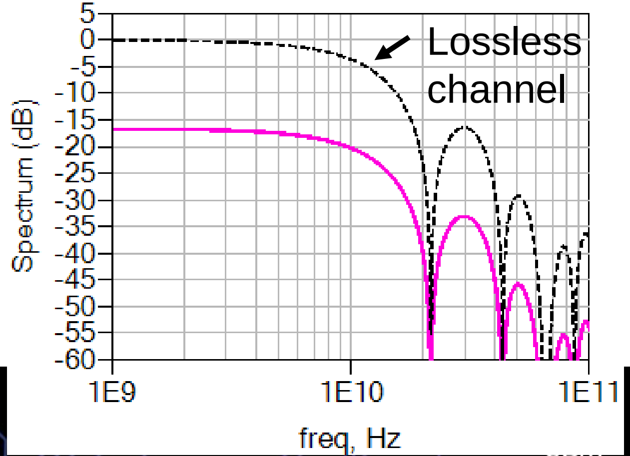






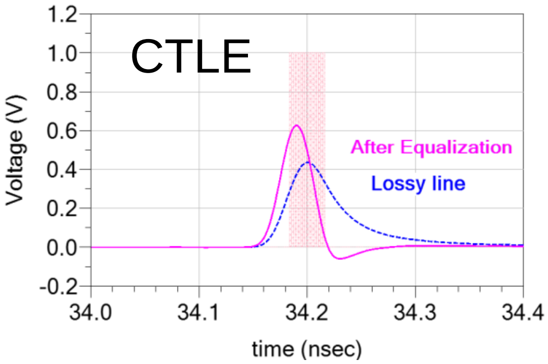


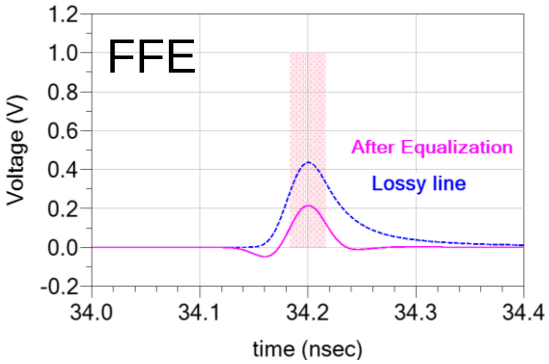
Equalization

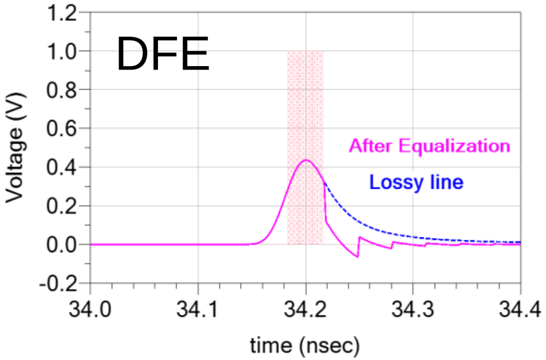


Need to **equalize** the frequency dependent loss

Different Equalization Approaches





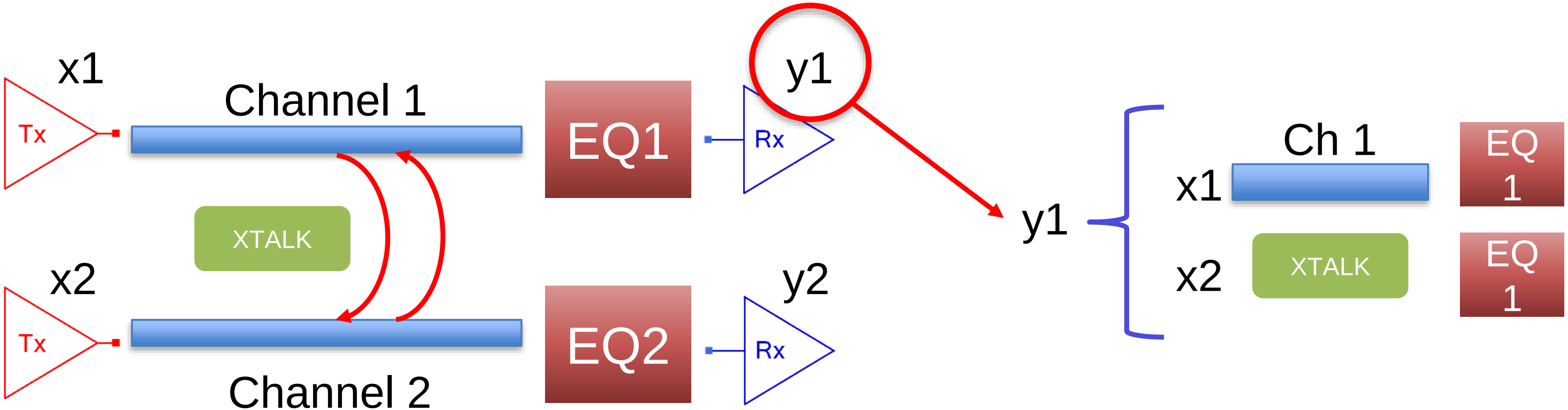


Continuous Time Linear Eq.	Feed Forward Eq.	Decision Feedback Eq.
Linear	Linear	**Non-Linear**
Analog	Digital	Digital
Only post cursor	**Pre and post cursor**	Only post cursor
Tx* or Rx	Tx* or Rx	**Rx**

*Need a back channel

Linear Equalization at Rx and its Influence on Crosstalk

Assume channels are symmetric, and equalization is linear.

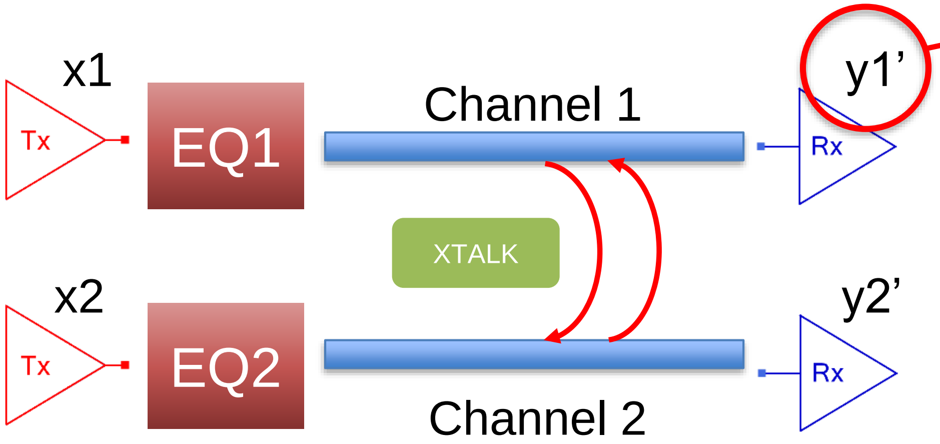


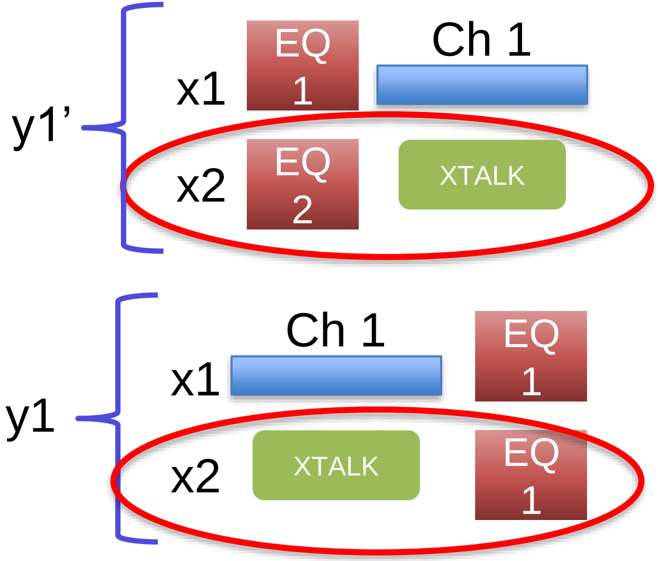
How about EQ at Tx?

x1, x2, y1, y2 are signals, and the blocks represent the transfer functions of each structure respectively.

Linear Equalization at Tx and its Influence on Crosstalk

Assume channels are symmetric, and equalization is linear.





Equalization at Tx can affect system crosstalk level.

Given the same channel, crosstalk is sensitive to EQ location **If two adjacent channels require different EQ.**

Summary of Equalizers and Priorities

Which tool do you grab first, and when?

Start here!

Tx

Tx Equalization

- Power limitation
- Adaptation to channel
- System crosstalk level

Channel

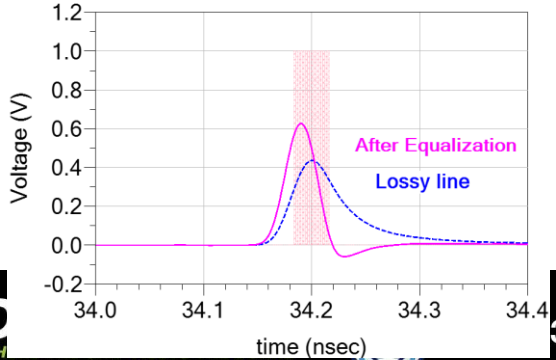
\+ Noise
\+ Crosstalk voltage

Rx Equalization

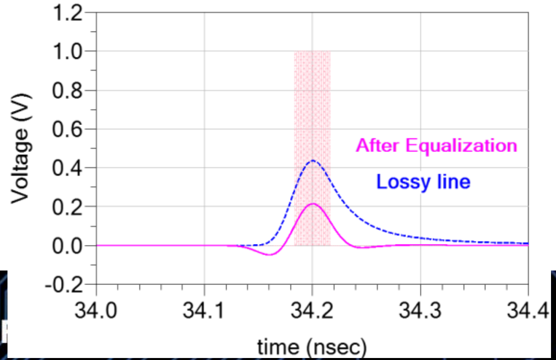
- Noise amplification
- Implementation complexity
- Signal to noise ratio

Rx

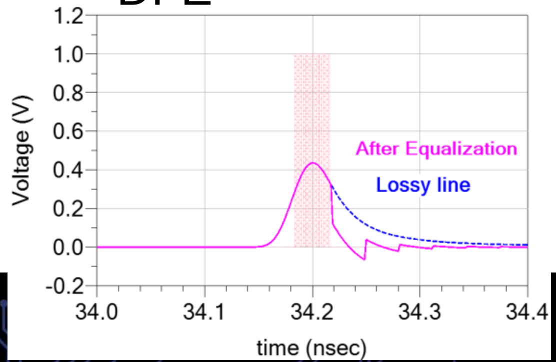
CTLE



FFE

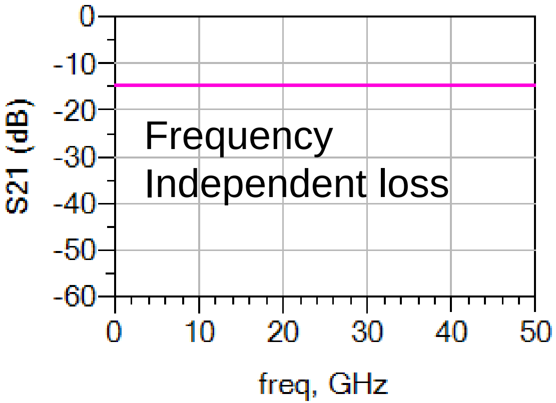


DFE

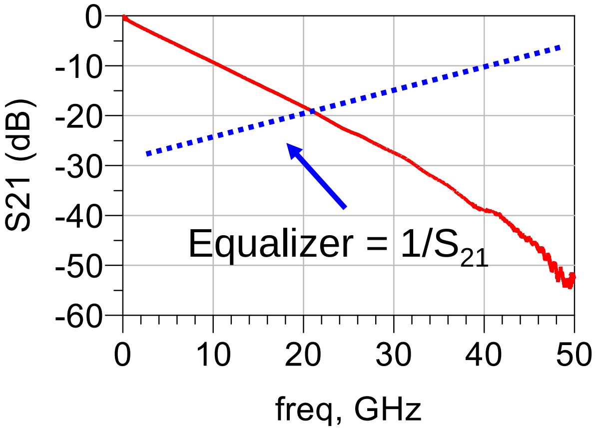


Continuous Time Linear Equalization Filter

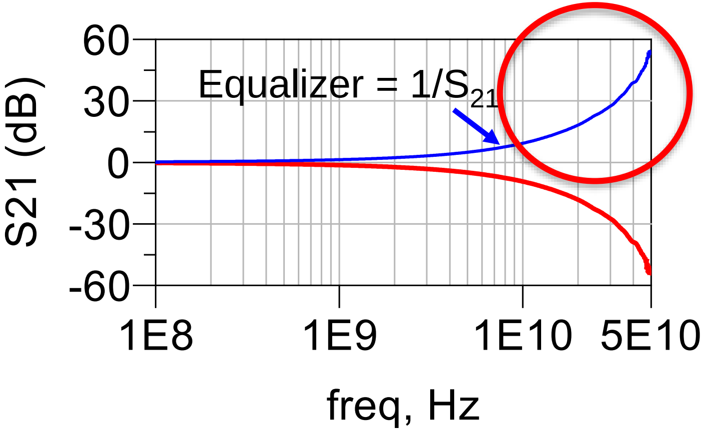
Desired Frequency Response



Channel Frequency Response

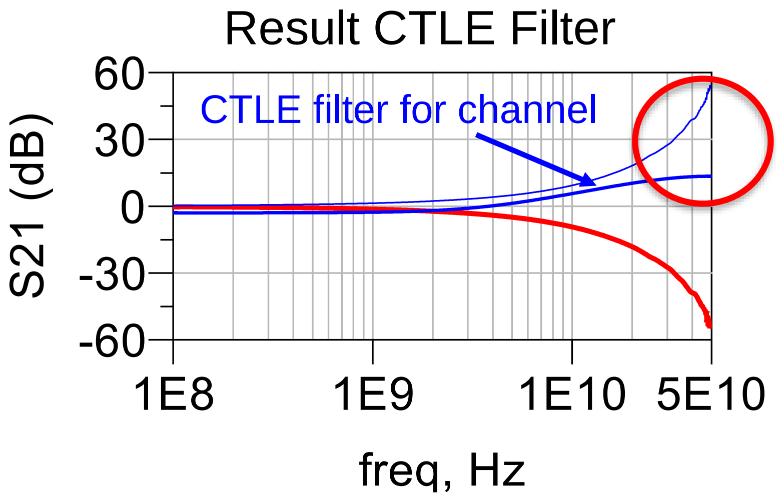


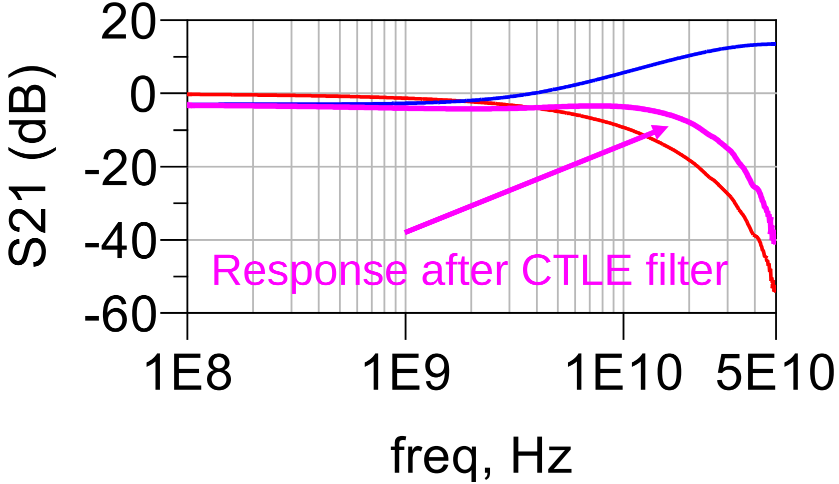
Log scale to exaggerate variation



The goal of CTLE is to create a **high-pass** filter that complements the loss-pass nature of the channel.

Flattened Channel Response after CTLE





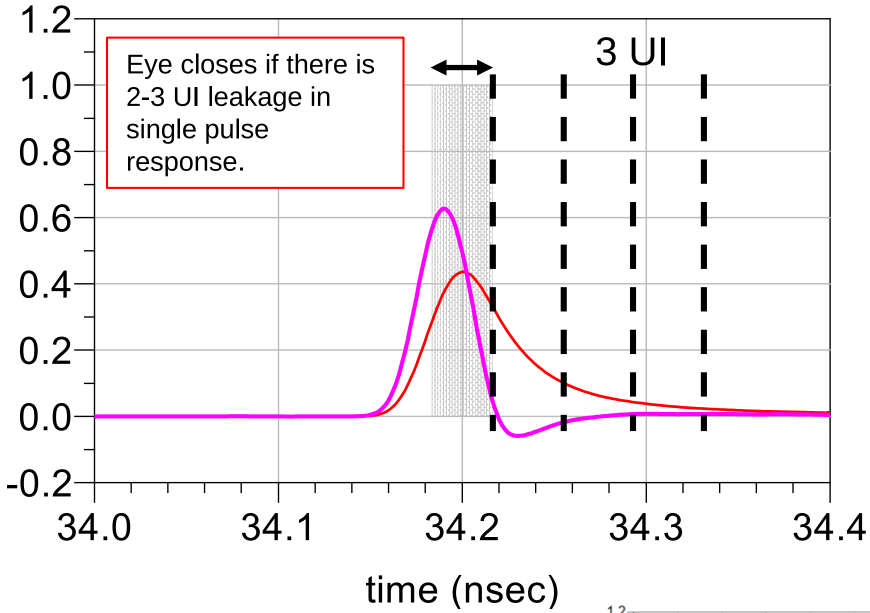
Construct transfer function from high pass filter $1/S_{21}$:

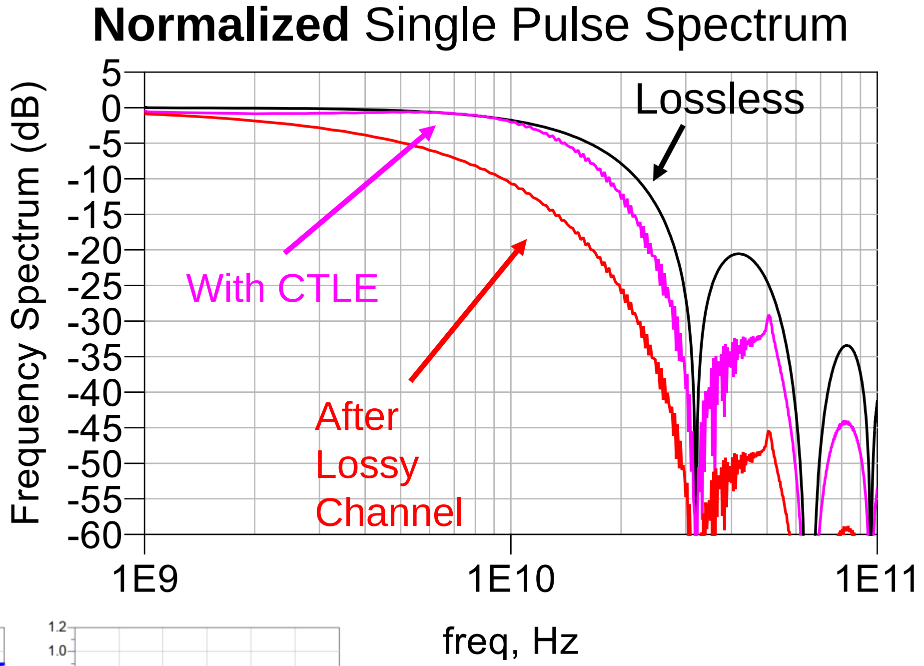
$$H(s) = \frac{A(s)}{B(s)} = K \frac{(s+z_1)}{(s+p_1)(s+p_2)}$$

$$z_1 = 2\pi \cdot (3.8\,\mathrm{GHz})$$
$$p_1 = 2\pi \cdot (50\,\mathrm{GHz})$$
$$p_2 = 2\pi \cdot (51\,\mathrm{GHz})$$

Can use transfer function to construct passive or active analog CTLE filter.

Single Pulse Response and CTLE

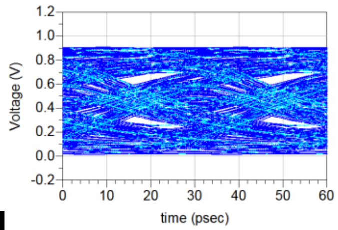


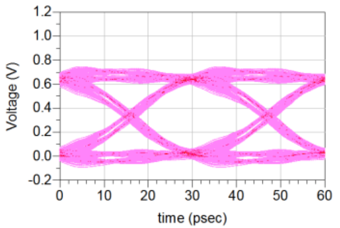


After Lossy Channel

With CTLE

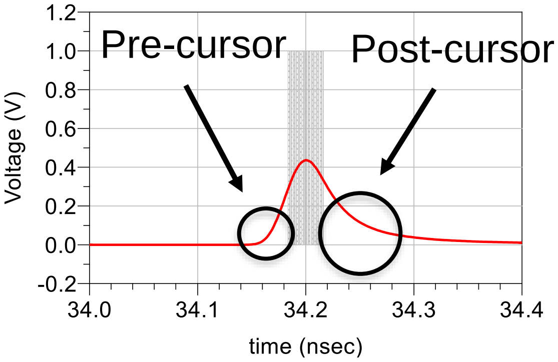
Lossless

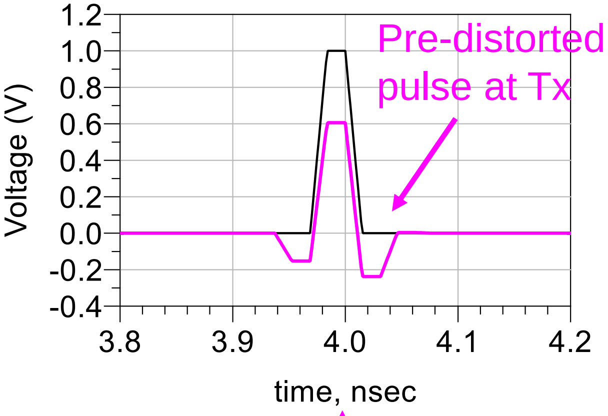




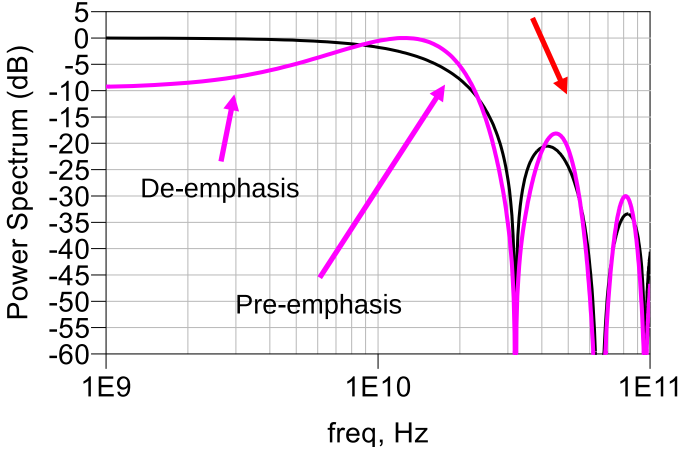
Feed Forward Equalizer at TX

Lossy Channel Single Pulse Resp.

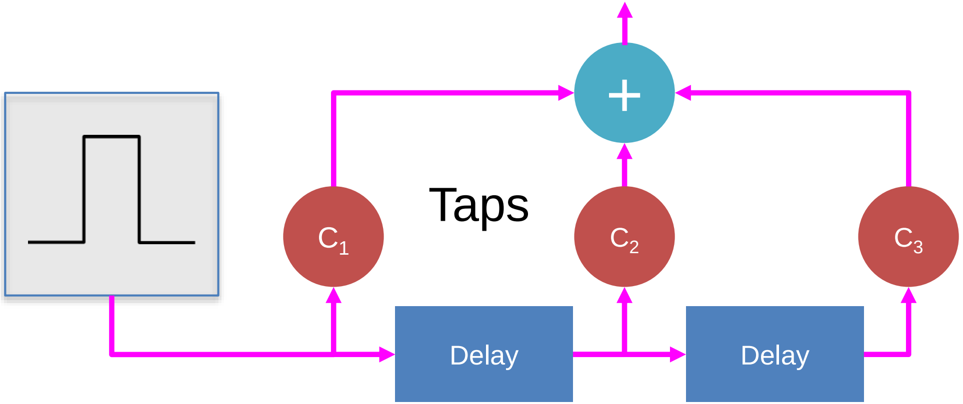




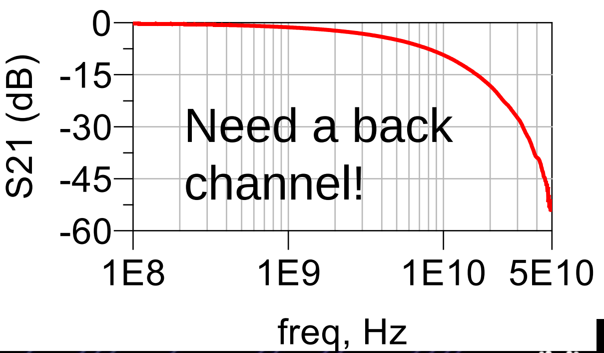
Caution!



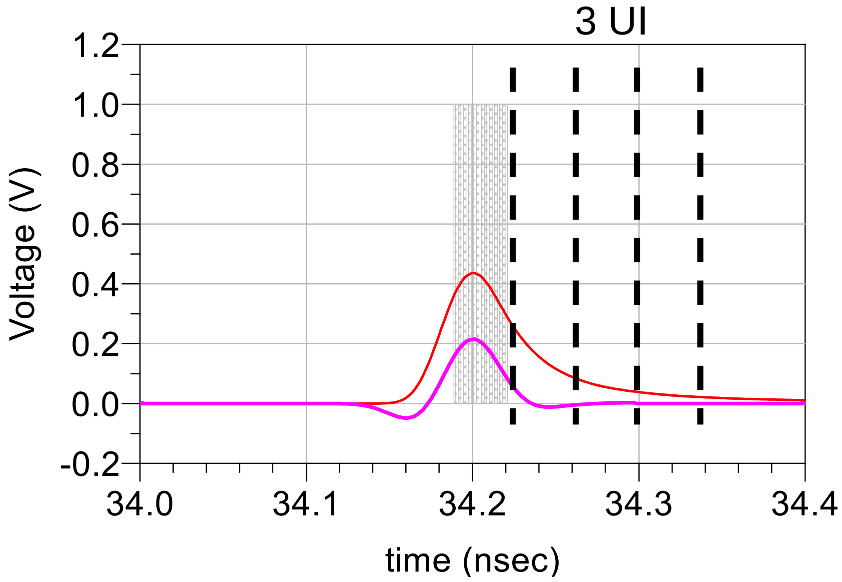
Feed Forward Equalizer Algorithm

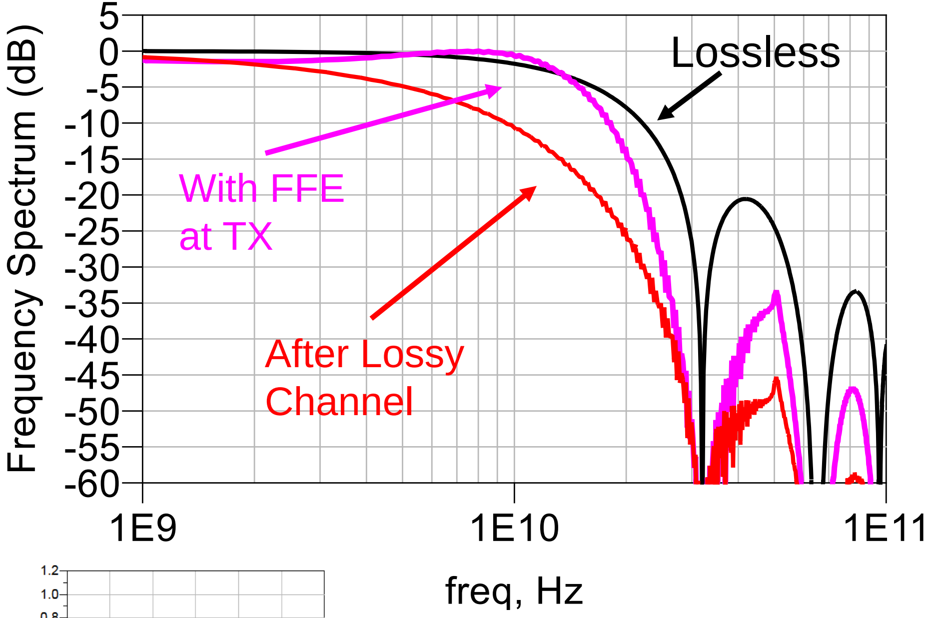


Channel Frequency. Resp.



Single Pulse Response and FFE

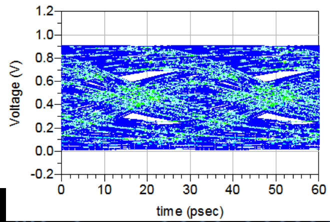


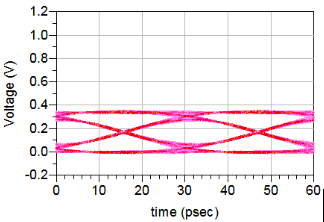


After Lossy Channel

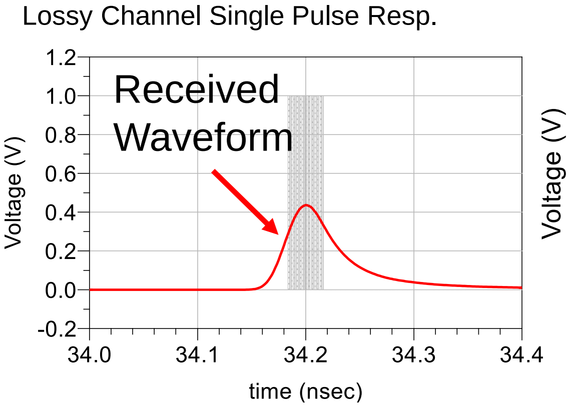
With CTLE

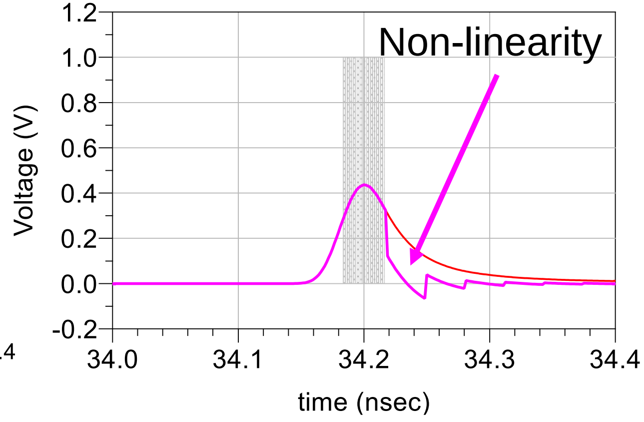
Lossless

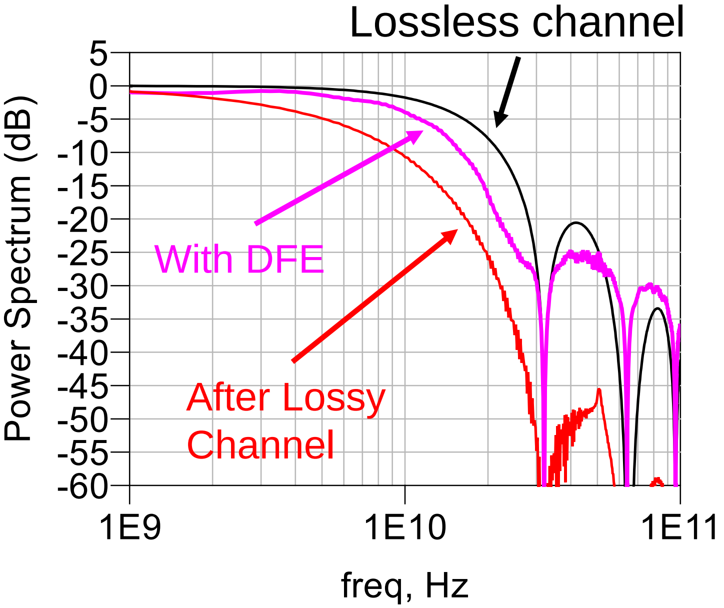


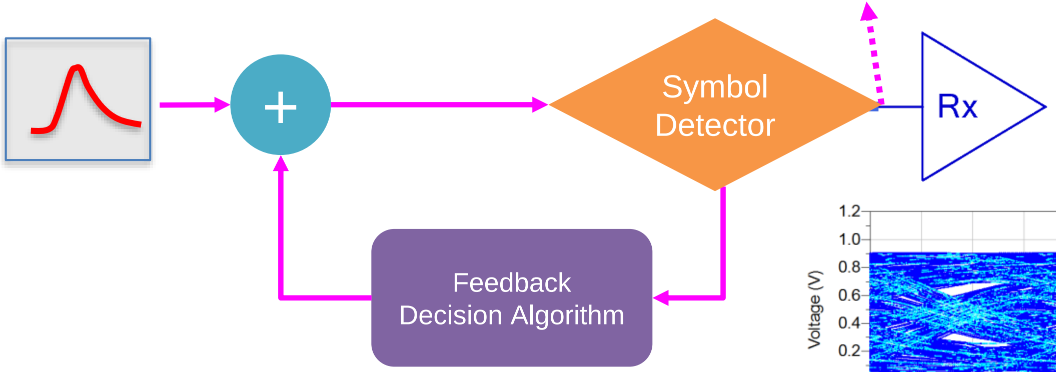


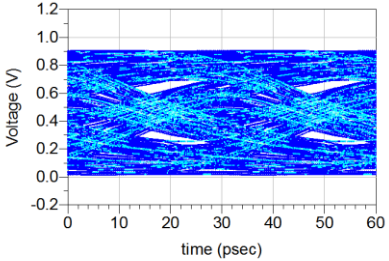
Decision Feedback Equalizer

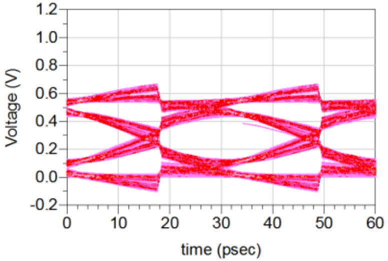




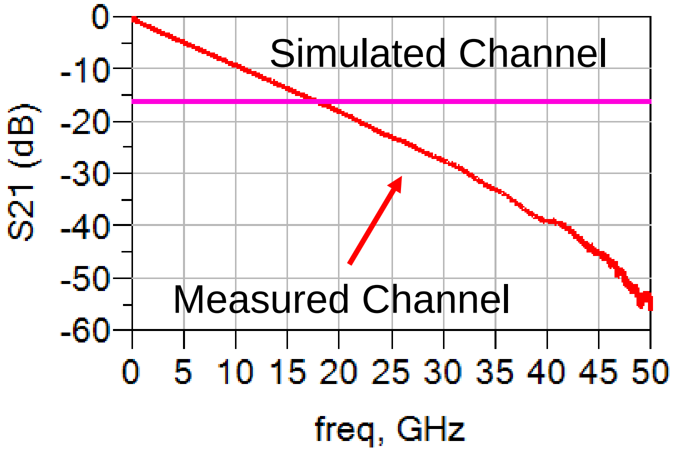


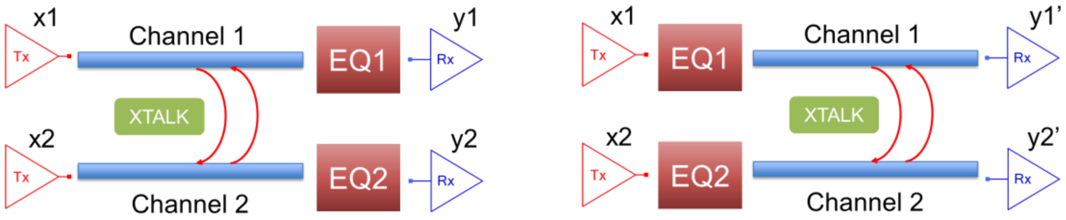




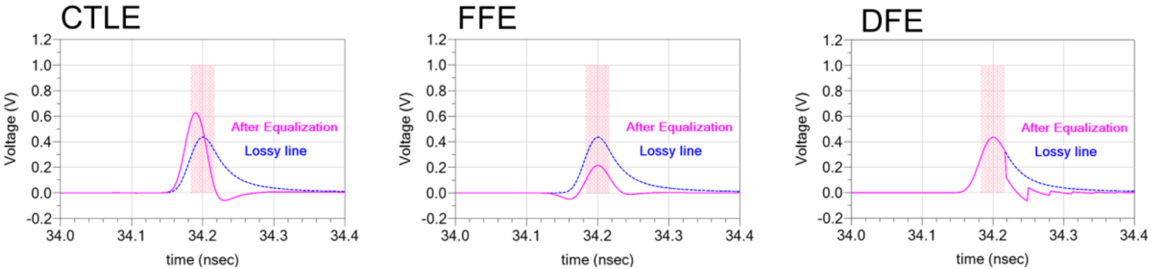


Summary of Equalization





When it comes to EQ, one size does not fit all.

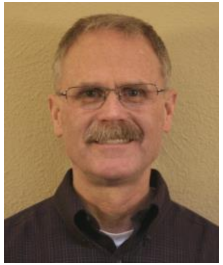


- EQ equalizes the frequency-dependent spectrum.
- Equalization at Tx can affect system crosstalk level.
- Use analysis and simulation with Tx/Rx IBIS-AMI models to determine what EQ to use and where.

Resources

- Wild River Technologies
  - Booth #850
- Equalization Techniques
  - S.H. Hall and H.L. Heck, Advanced Signal Integrity for High-Speed Digital Designs (2009).

Agenda



Jack Carrel

SerDes Apps. Engineer, Xilinx

- Full-Link KR Example
- What is a “Pathological Channel”
- Measuring Pathological Channels
- Band Limited S-Parameters
- Using the Pulse Response to Gain Insight

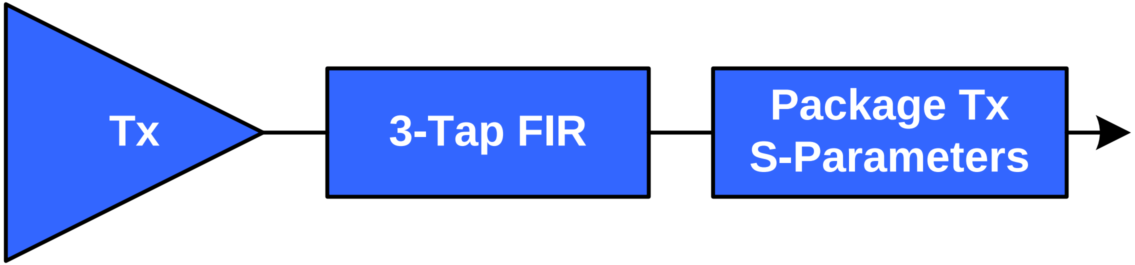
- BREAK

- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- Summary

Simulating with IBIS-AMI Models

- Xilinx UltraScale+ IBIS-AMI Model: TX

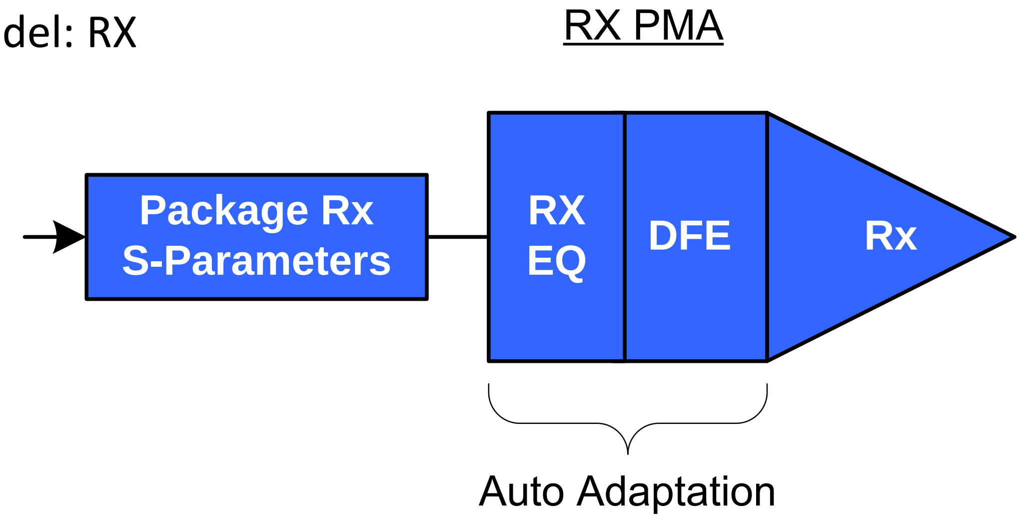
<u>TX PMA</u>



- Pre-emphasis "0 thru 31" – 0 dB to 12.96 dB emphasis - Default: 0
- Post-emphasis "0 thru 31" – 0 dB to 6.02 dB emphasis - Default: 0
- Main Tap “0 thru 31“ – 191 mVpp to 933 mVpp – Default: 28
- TX_PVT "TX_PVT, 0--typical, 1--fast, 2--slow“ – Default: 0

Simulating with IBIS-AMI Models

- Xilinx UltraScale+ IBIS-AMI Model: RX



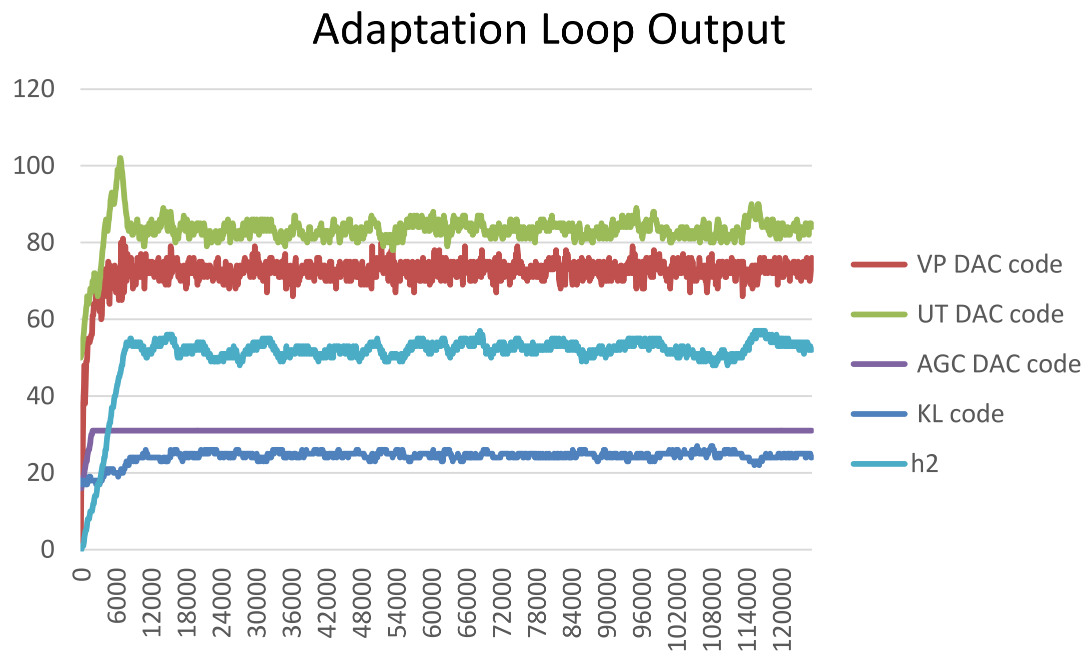
- RXLPMEN "0=DFE mode; 1=LPM mode" – Default: 0
- RX_XMODE_SEL "0= >6.25Gbps; 1= ≤ 6.25Ggbps" – Default: 0
- DFE_RSV_0 "0 thru 127" – Default 0 (Depends on insertion-loss and data rate)
- …

Simulating with IBIS-AMI Models

- Include supplied die and package S-parameter files in simulation.
- Specify
  - Line rate
  - Tx data pattern.
    - Provided PRBS Patterns
    - Custom pattern from external file
- Samples per bit (SPB) of 64 is recommended for data rates of 1 Gb/s and above.
- For data rates 1 Gb/s and below, SPB of 128 or higher is recommended.
- It is suggested to run at least 1,000,000 bits, and ignore first 500,000 bits.

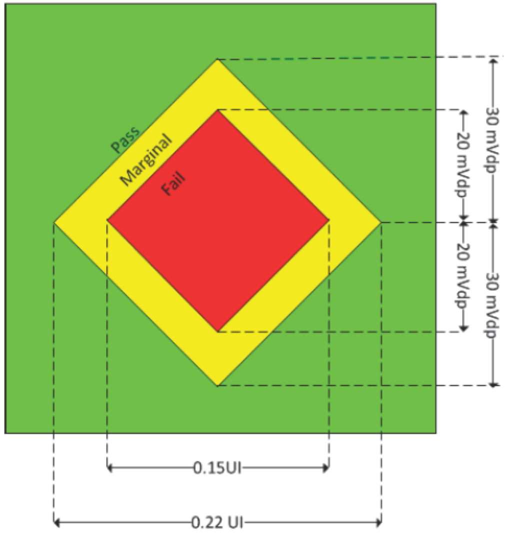
Simulating with IBIS-AMI Models

- Simulation generates Adaptation loop output file:

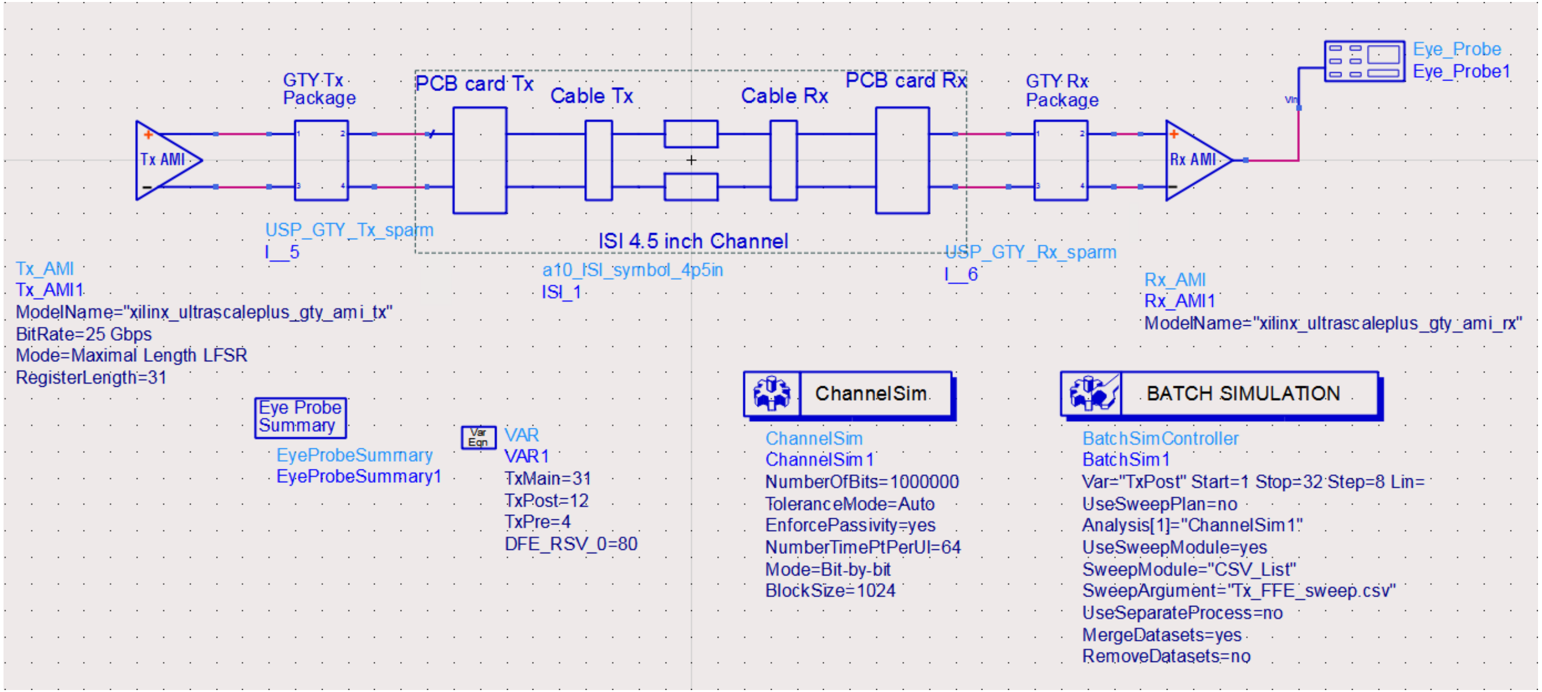


Simulating with IBIS-AMI Models

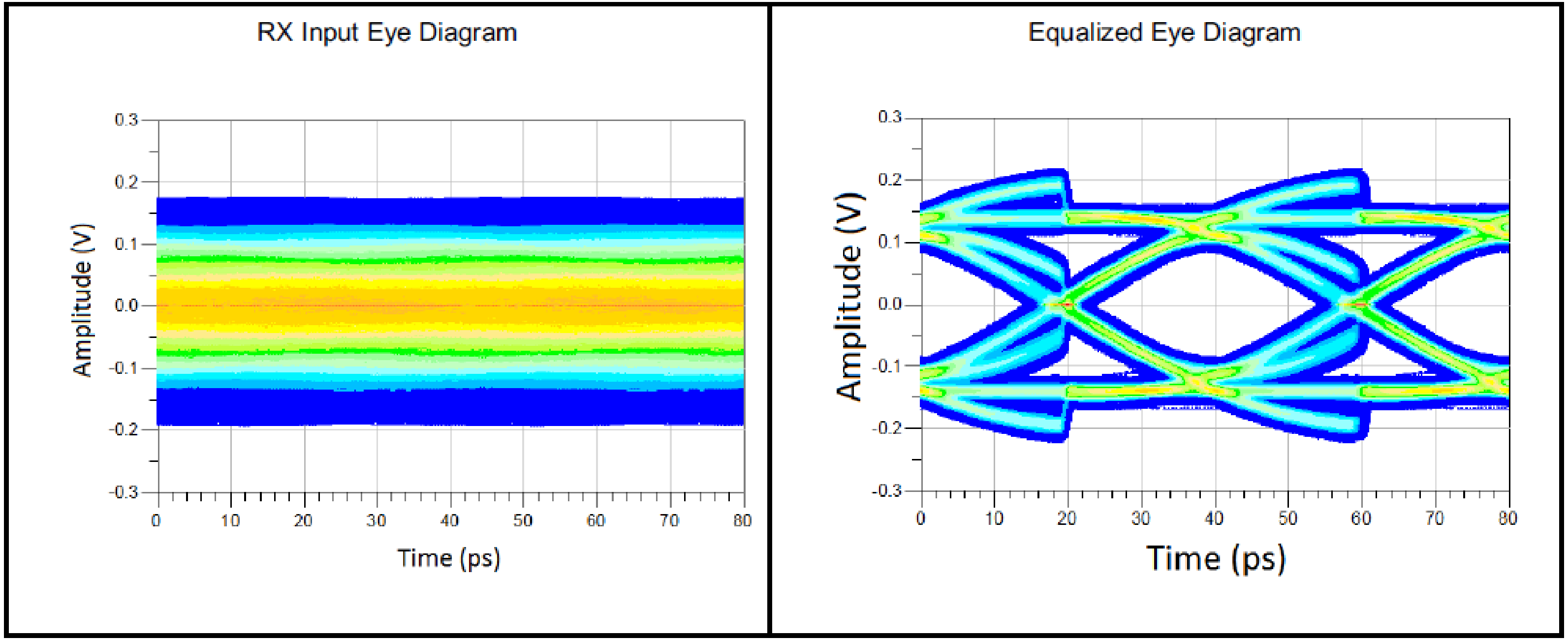
- **Simulation BER Contour Mask for UltraScale+ GTY Transceiver**



Simulating with IBIS-AMI Models



Simulating with IBIS-AMI Models



And now to target simulations for channel diagnosis…

Agenda

- Full-Link KR Example
- What is a “Pathological Channel”
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- Band Limited S-Parameters
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- BREAK

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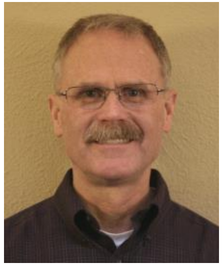


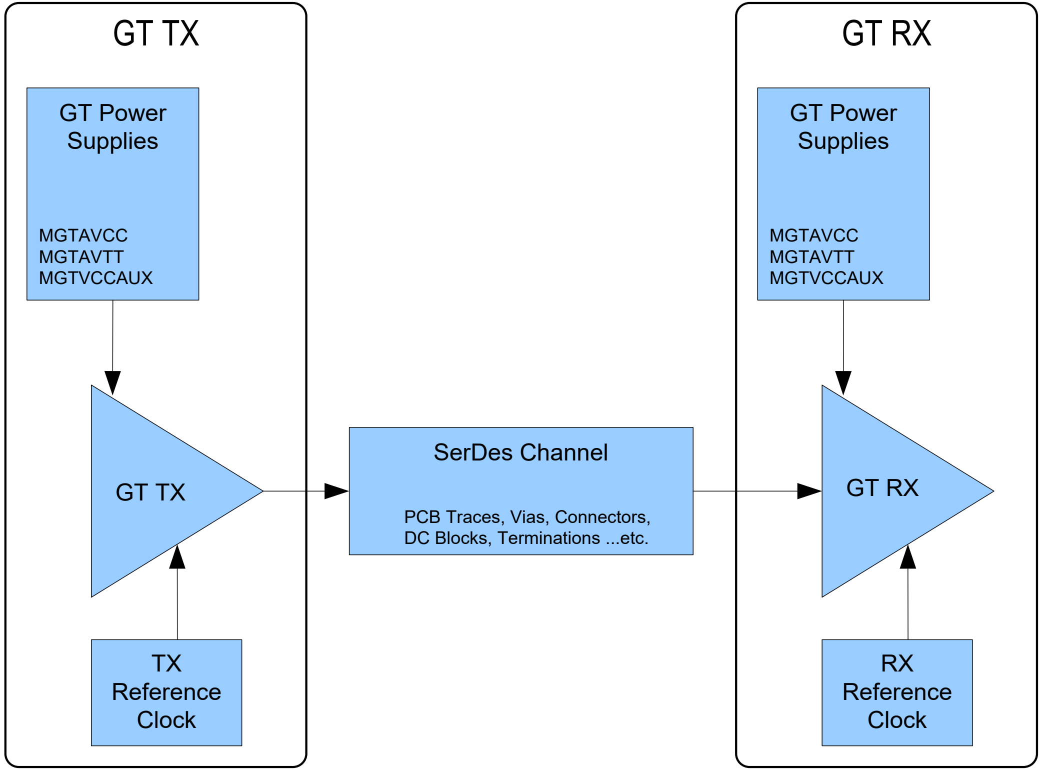
Jack Carrel

SerDes Apps. Engineer, Xilinx

SerDes Link Debug – bits & pieces

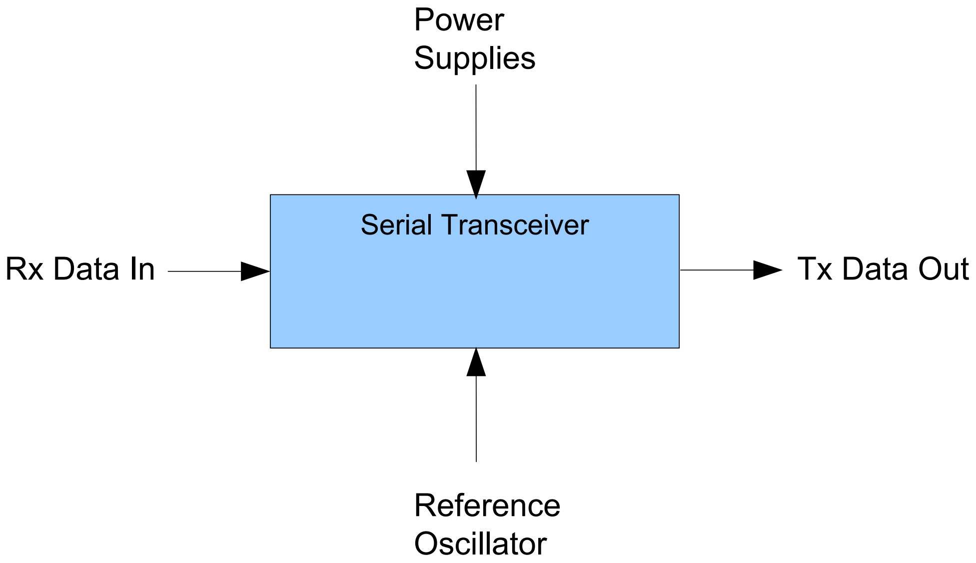
- Power Supplies
  - MGTAVCC
  - MGTAVTT
  - MGTVCCAUX
- Transmitter
- Receiver
- Reference Clock

- *Verify connectivity*
- *Verify compliance*



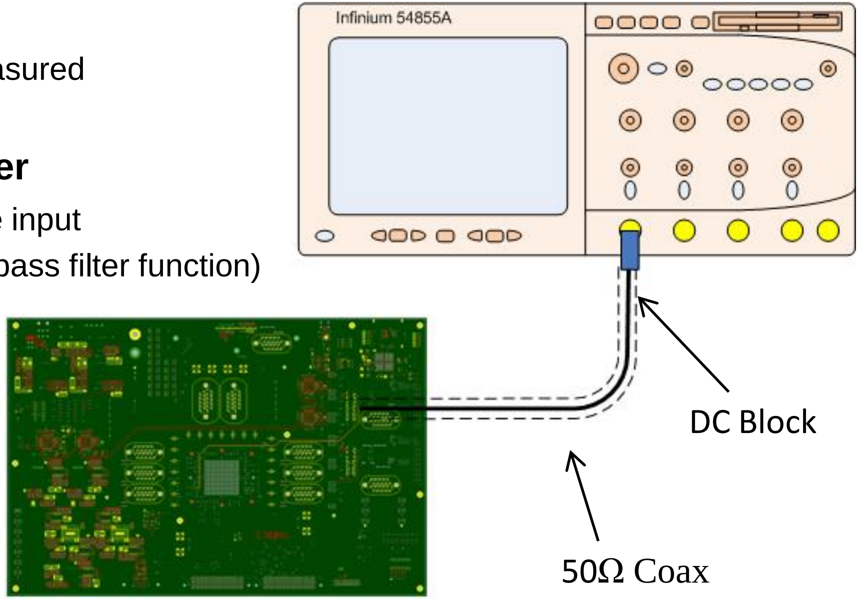
SerDes Link Debug – 4 Port Device

- **Power Supplies**
  - MGTAVCC
  - MGTAVTT
  - MGTVCCAUX
- **Transmitter**
- **Receiver**
- **Reference Clock**



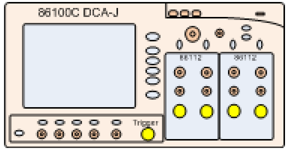
SerDes Link Debug – Power Supply Measurements

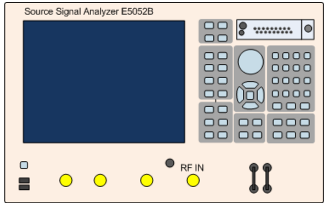
- **Use 50 ohm probing. Using 50 ohms makes it easy to have a constant impedance for the entire path from the DUT to the oscilloscope input.**
- **Band limit the measurement. Limiting the bandwidth will**
  - Reduce confusion from out-of-band energy.
  - Allows for easier detection and interpretation of measured waveform. (i.e. observe only what matters)
- **To band limit, use a low-pass filter by using either**
  - External low-pass filter between the DUT and scope input
  - Math processing function on the oscilloscope (Low-pass filter function)



SerDes Link Debug – Clock Measurements

- **Clock measurements**
  - Use TX output to measure clock frequency and phase quality
  - Use alternating pattern of equal numbers of one’s and zero's to generate ‘square wave’.
    - Frequency dependent channel losses are mitigated with alternating high-low pattern.
    - Pattern dependent distortion is minimized
  - Time Domain
    - Use scope with Jitter analysis package to measure Rj from TX square wave pattern.
    - Besides Rj look for Pj. Existence of Pj may be caused by interference (i.e. power supply noise, crosstalk, etc.)
  - Frequency Domain
    - Use Signal Analyzer or Spectrum Analyzer with phase noise package
    - Measure phase noise
      - Observe noise up to PLL tracking frequency (~1 to 10MHz)
      - Look for significant spurs at higher frequencies.
      - Calculate Rj for sanity check (Most instruments will do this for you.)





SerDes Link Debug – RefClk Phase Noise

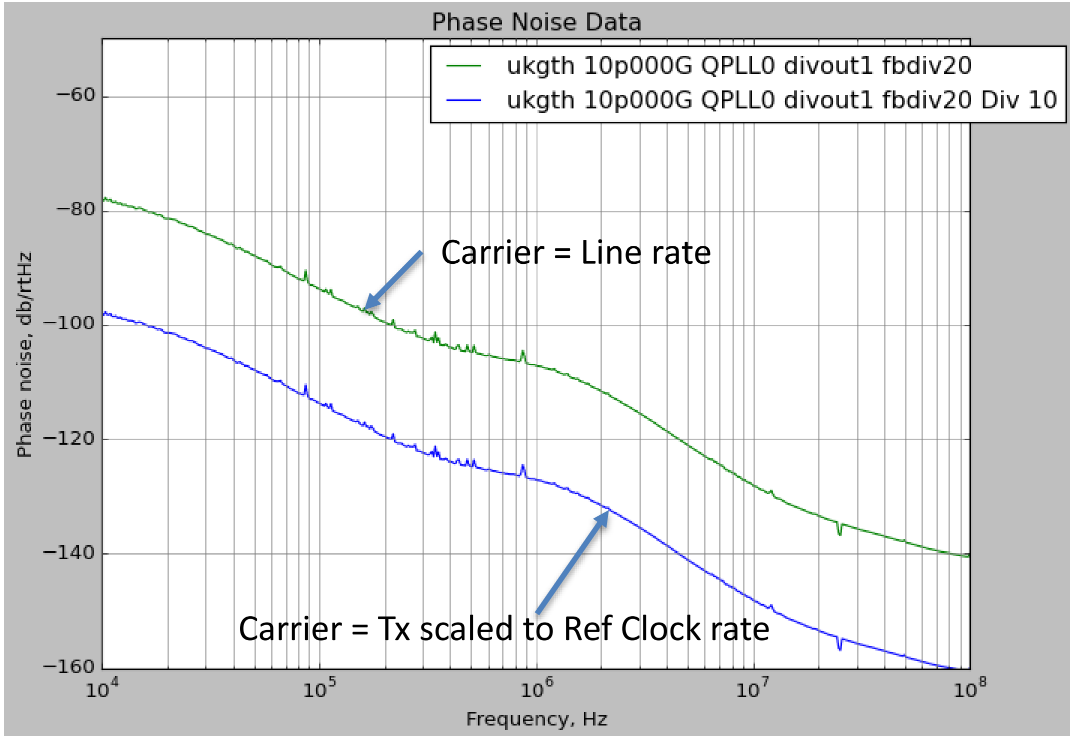
UltraScale GTH

RefClk: 500.0 MHz

Line rate: 10.0 Gb/s

Scale phase noise to carrier Frequency:

$$\mathrm{dB} + \left[20 \bullet \log_{10}\left[\frac{F_{OUT}}{F_{IN}}\right]\right]$$



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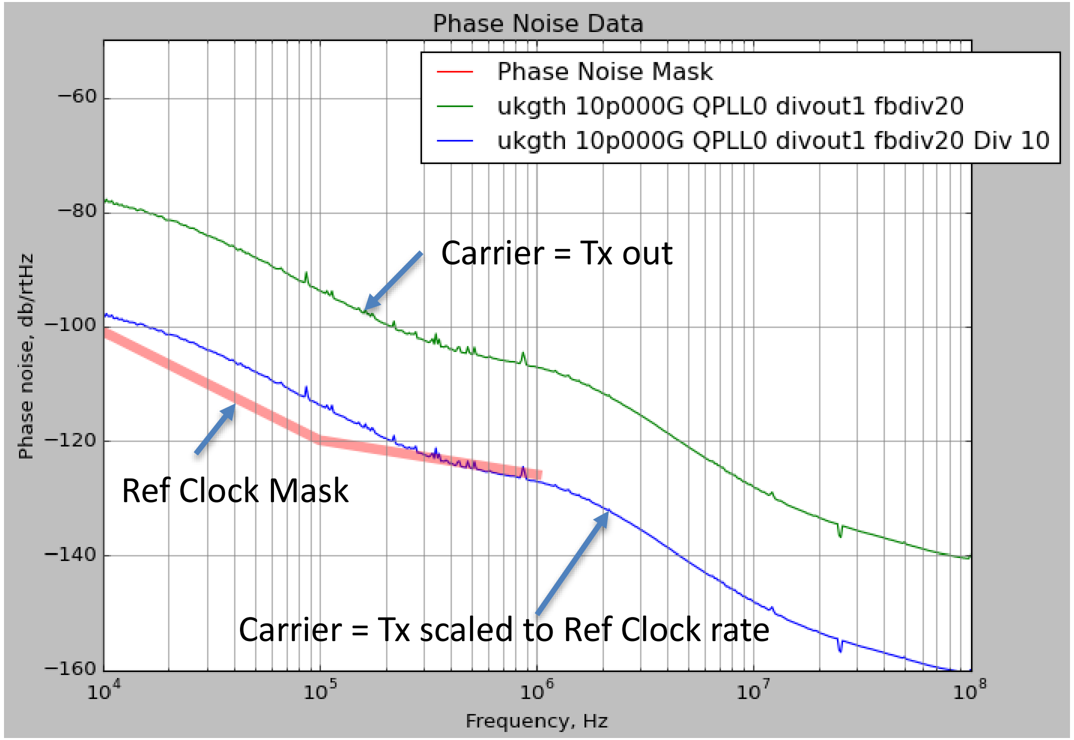

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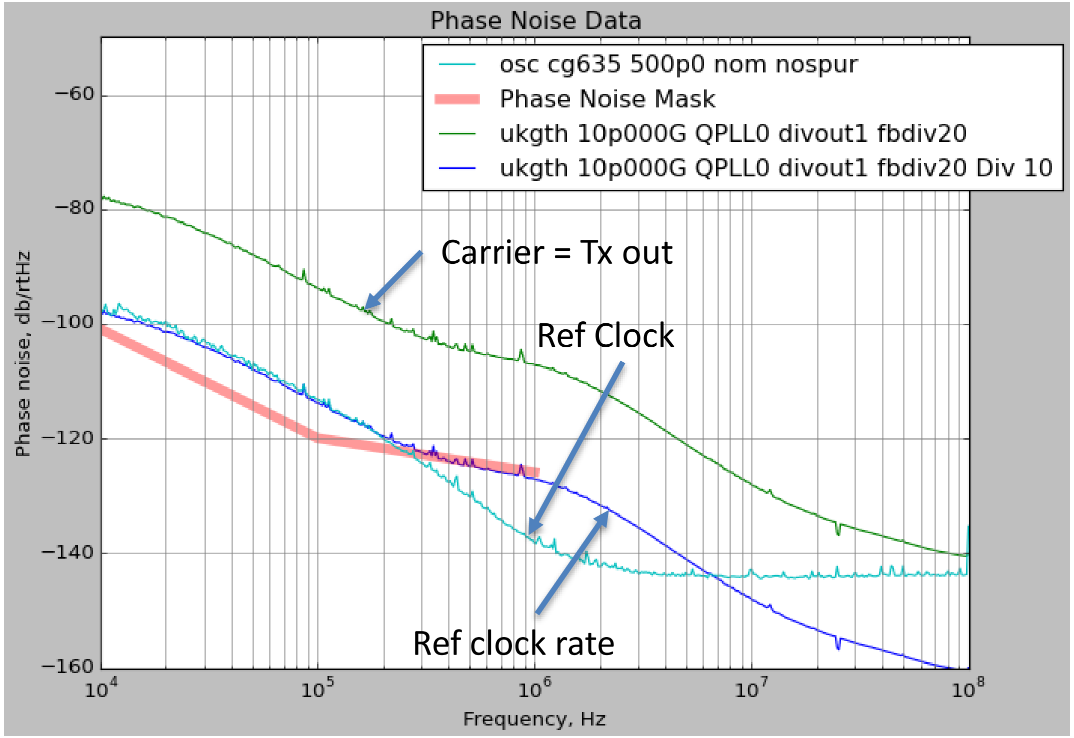

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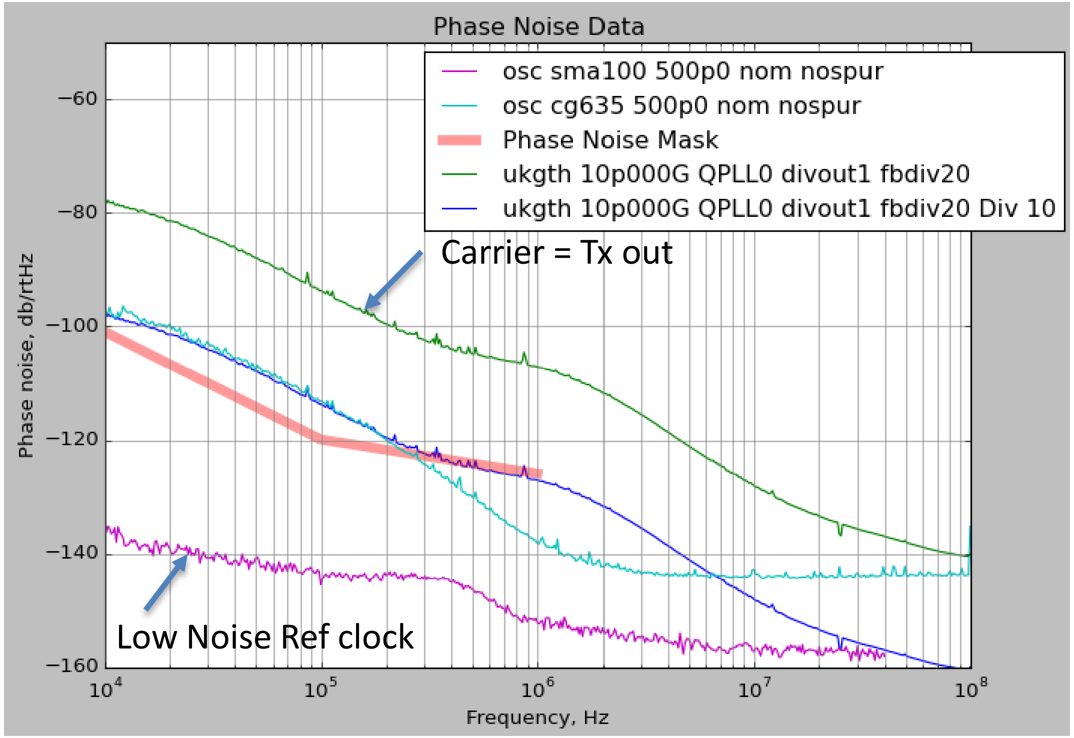

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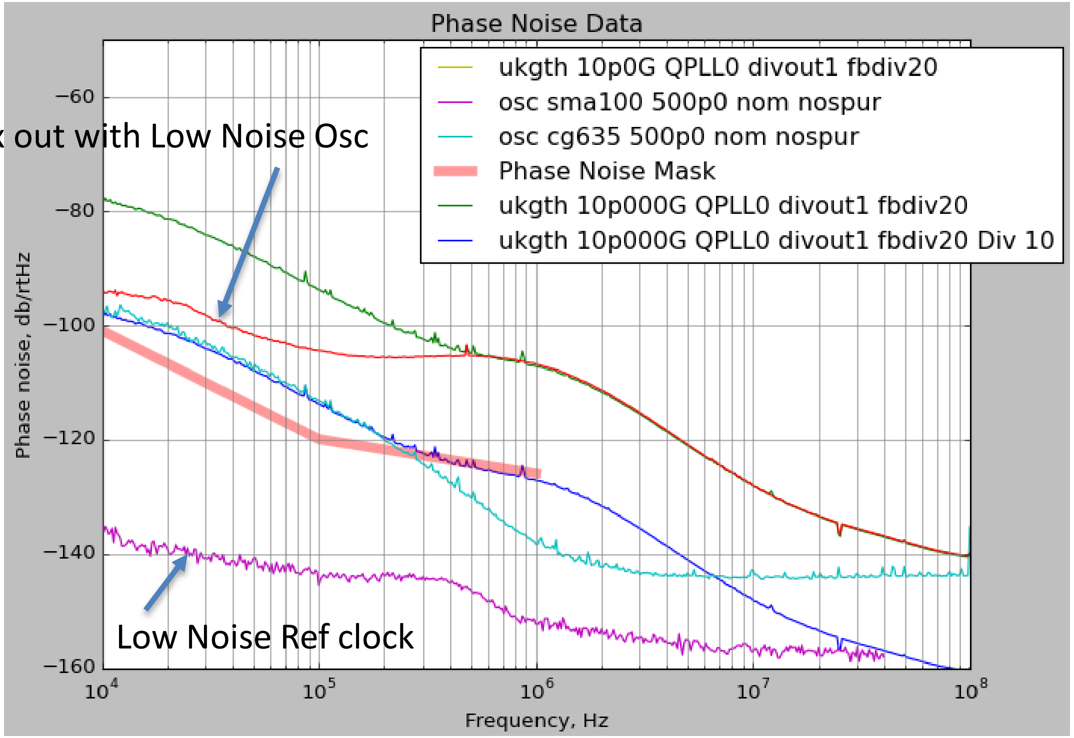

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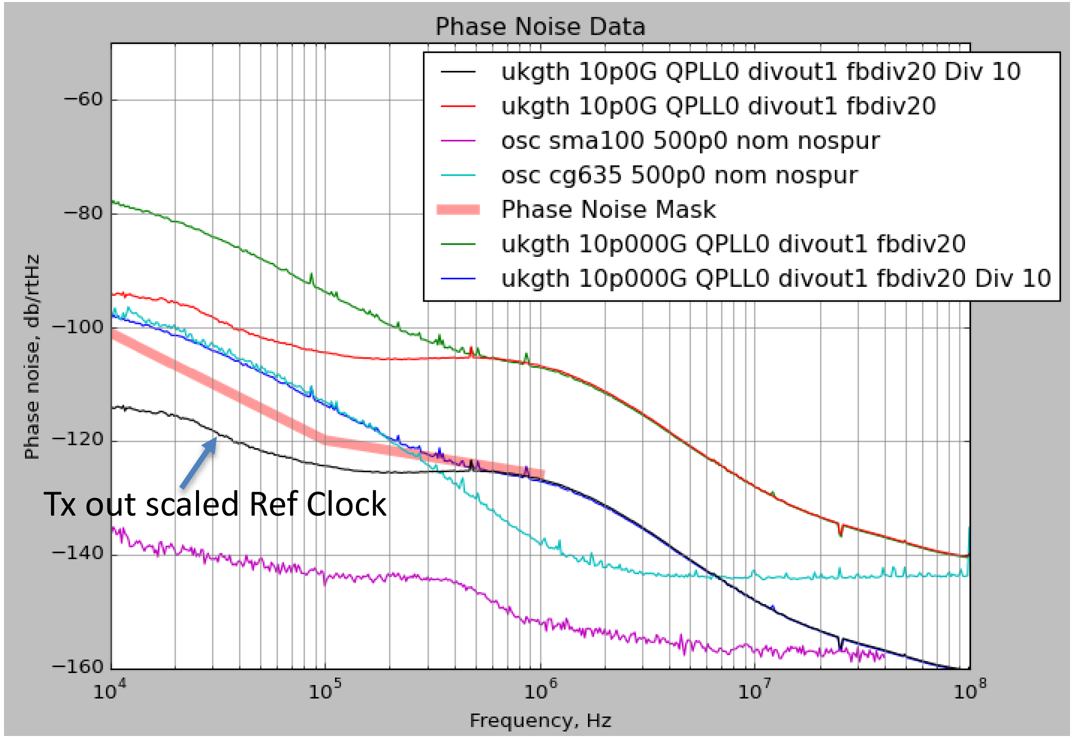
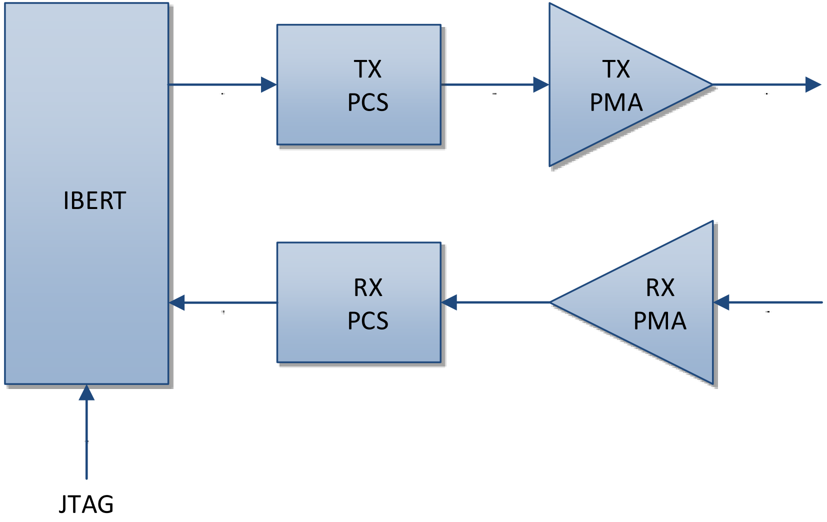


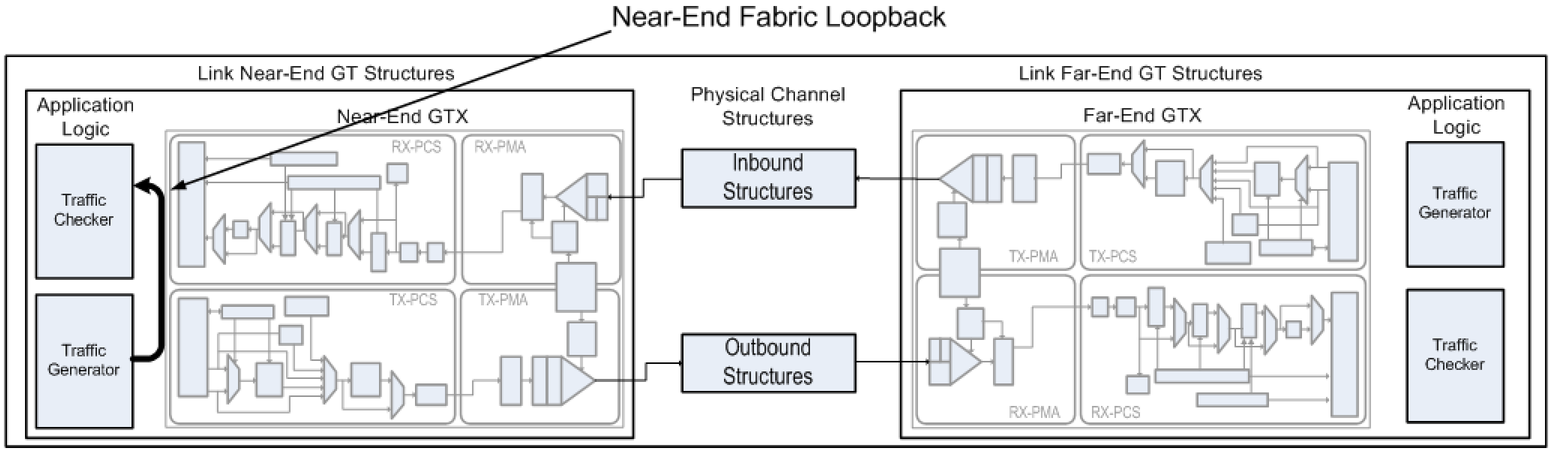
SerDes Link Debug – IBERT

- **IBERT – Integrated Bit Error Rate Tester**
  - Serial I/O Analyzer
  - Full access to transceiver configuration registers
    - TX pre-emphasis and post-emphasis
    - RX equalization
    - Decision feedback equalizer (DFE)
    - Phase-locked loop (PLL) divider settings
  - Pattern Generator/Checker
  - Internal eyescan
  - Runtime accessible thru JTAG
  - Interactive or TCL scripted control



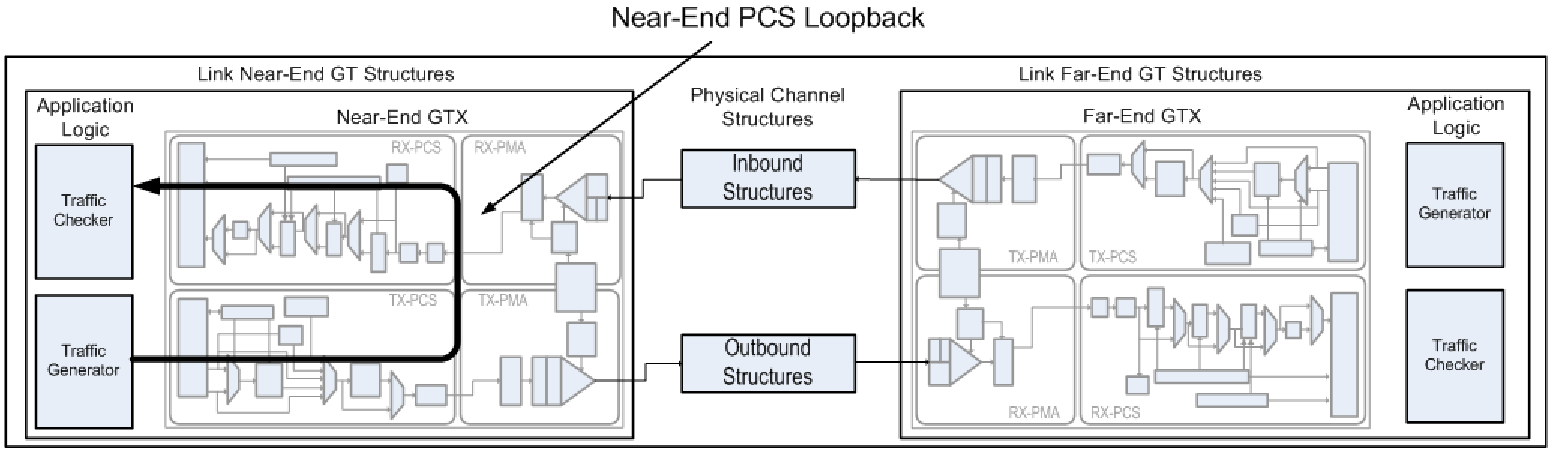
SerDes Link Debug – Loopback Testing

- **Loopback testing (Run bit error test under each condition)**
  - Near-end fabric loopback (verifies fabric logic inbound and outbound)



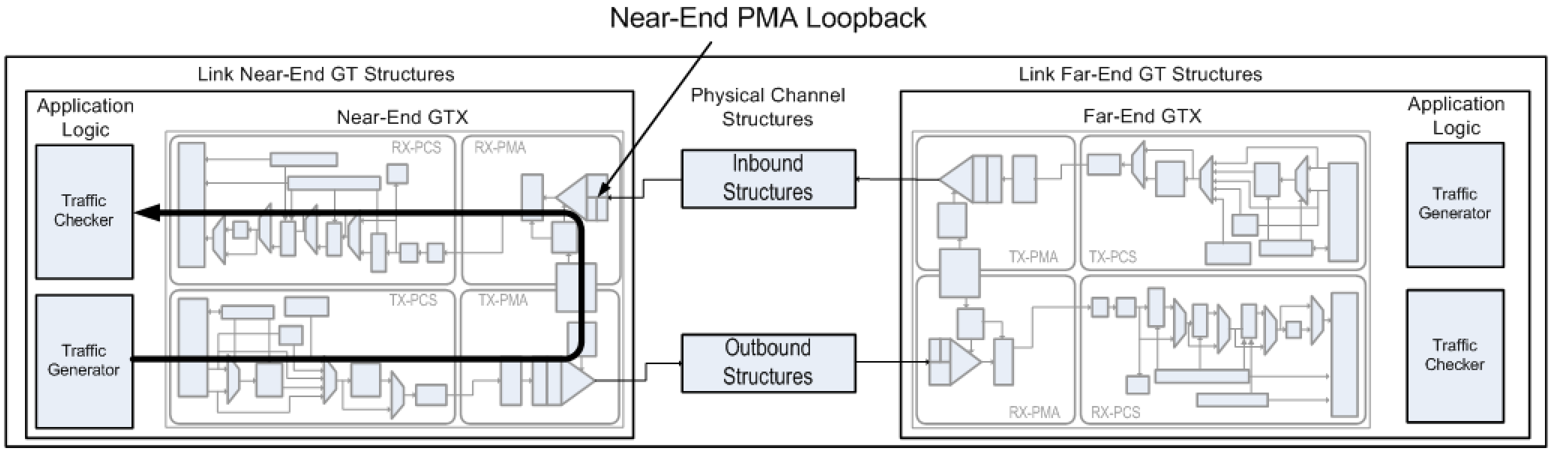
SerDes Link Debug – Loopback Testing

- **Loopback testing (Run bit error test under each condition)**
  - Near-end fabric loopback (verifies fabric logic inbound and outbound)
  - Near-end PCS loopback (verifies fabric to GT interface inbound and outbound)



SerDes Link Debug – Loopback Testing

- **Loopback testing (Run bit error test under each condition)**
  - Near-end fabric loopback (verifies fabric logic inbound and outbound)
  - Near-end PCS loopback (verifies fabric to GT interface inbound and outbound)
  - Near-end PMA loopback (verifies fabric thru PMA path inbound and outbound)



SerDes Link Debug – Loopback Testing

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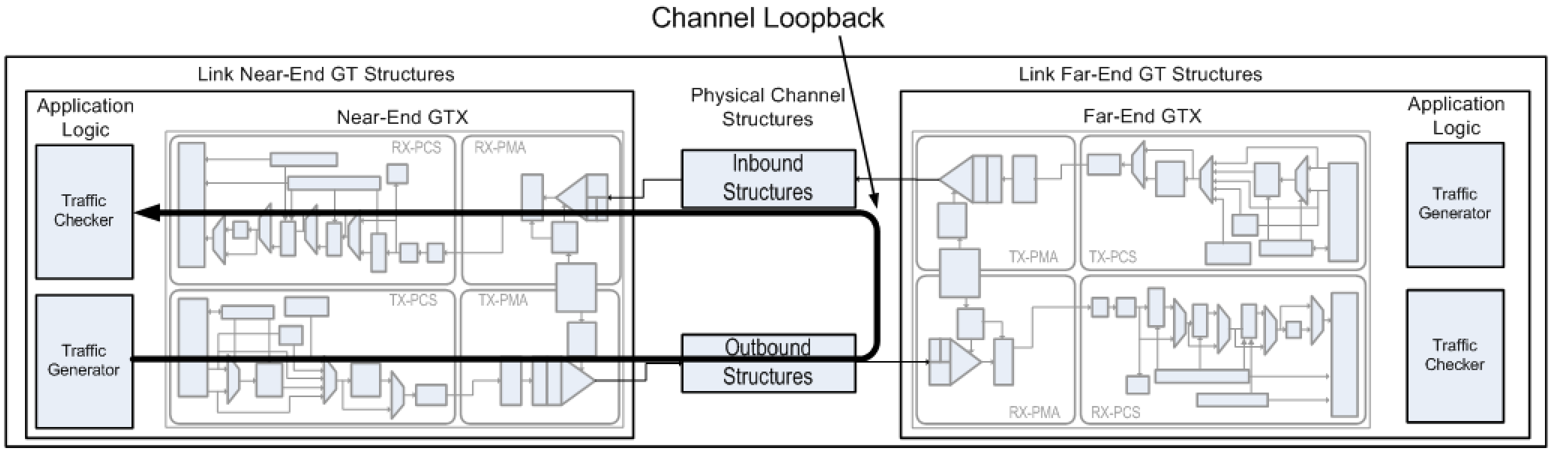
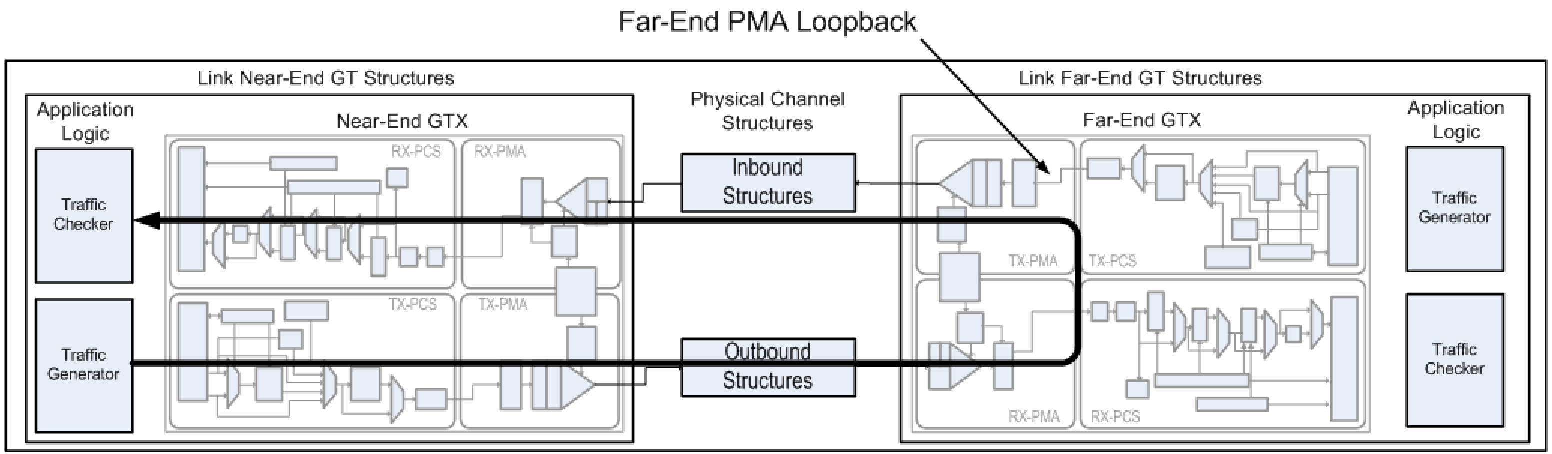
  - Near-end PCS loopback (verifies fabric to GT interface inbound and outbound)
  - Near-end PMA loopback (verifies fabric thru PMA path inbound and outbound)
  - Channel loopback
    - Prefer a loopback thru as much of the channel as possible to verify channel performance



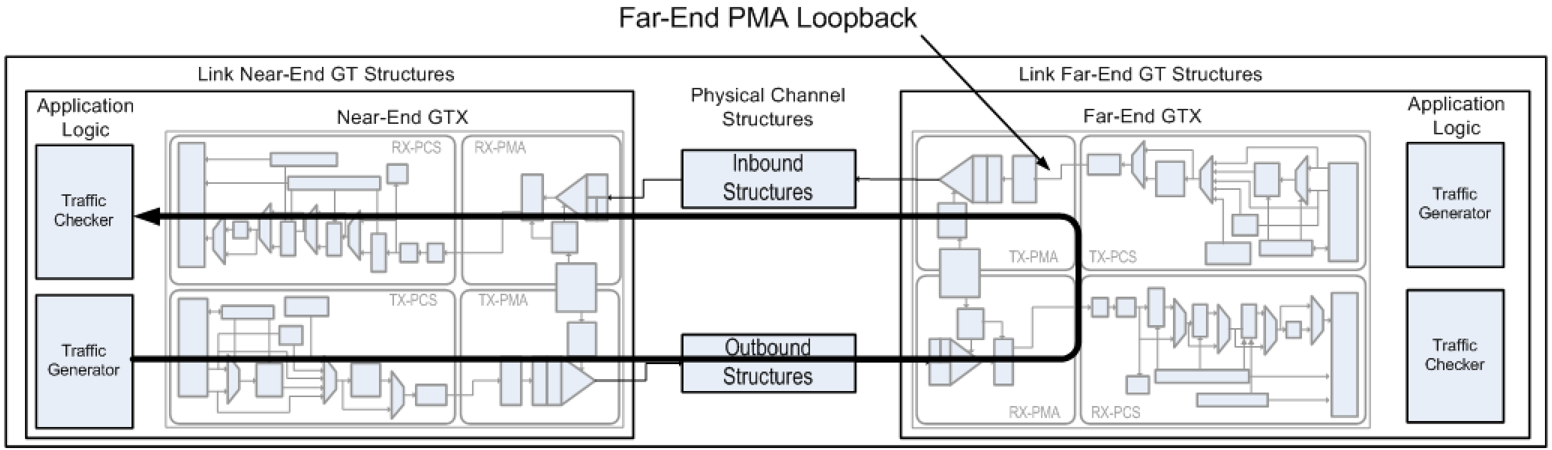
SerDes Link Debug – Loopback Testing

- **Loopback testing (Run bit error test under each condition)**
  - Nearend fabric loopback (verifies fabric logic inbound and outbound)
  - Nearend PCS loobback (verifies fabric to GT interface inbound and outbound)
  - Nearend PMA loopback (verifies fabric thru PMA path inbound and outbound)
  - Channel loopback
    - Prefer a loopback thru as much of the channel as possible to verify channel performance
  - Farend PMA



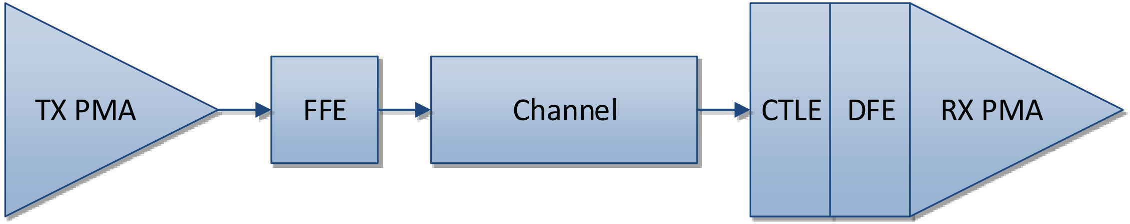
SerDes Link Debug – Loopback Testing

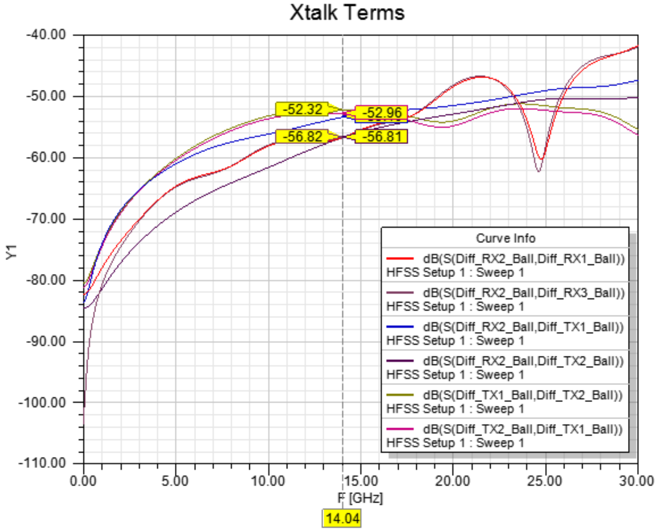
- **Loopback testing (Run bit error test under each condition)**
  - Nearend fabric loopback (verifies fabric logic inbound and outbound)
  - Nearend PCS loobback (verifies fabric to GT interface inbound and outbound)
  - Nearend PMA loopback (verifies fabric thru PMA path inbound and outbound)
  - Channel loopback
    - Prefer a loopback thru as much of the channel as possible to verify channel performance
  - Far-end PMA
  - Far-end fabric loopback, if clocking supports it



SerDes Link Debug – Managing Equalization

- **<u>Resources</u>**
  - Receiver
    - CTLE
    - DFE
    - Auto-adaptation
  - Transmitter
    - Output amplitude
    - FFE
      - Pre-emphasis
      - Post emphasis





SerDes Link Debug

So, how did we do?...

Thank you!

QUESTIONS?

Agenda

Heidi Barnes

SI/PI Apps. Engineer
Keysight Technologies

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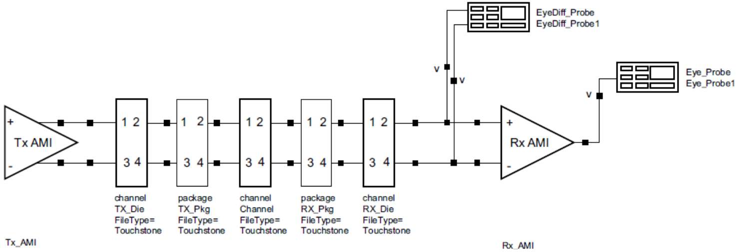
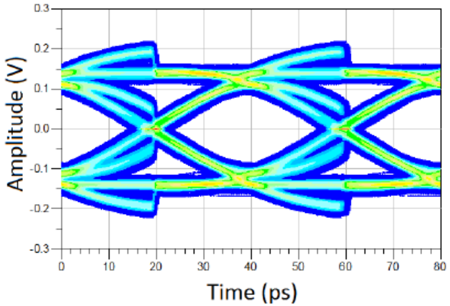
Verify the Simulation Set-up

Good IBIS AMI Models come with an example for comparison

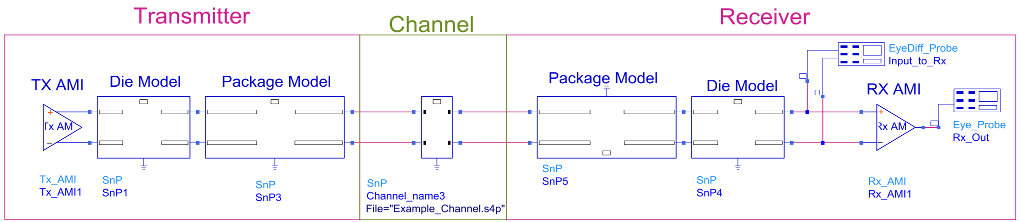
IBIS AMI Kit Example



Equalized Eye Diagram



My Simulator Setup



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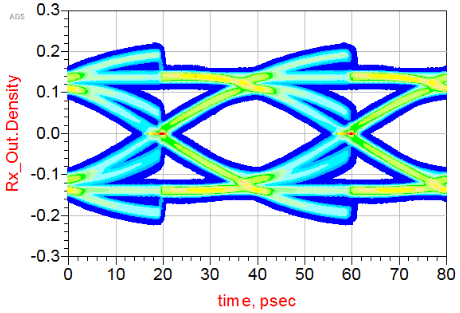
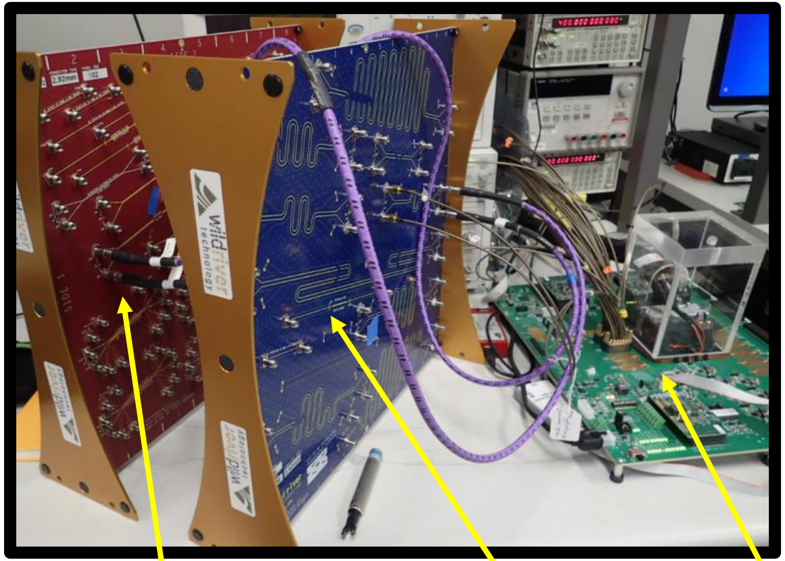


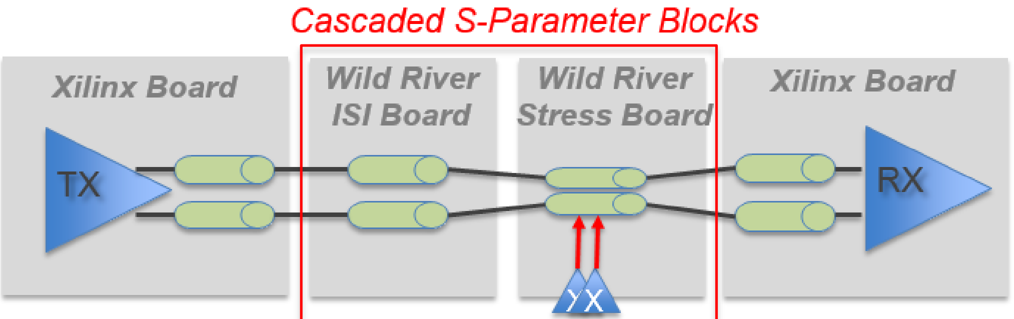
Design of Experiments



Stress
XTALK, Reflection

Material
ISI

Xilinx
UltraSCALE+ Board



Adjustable
Tx Equalizer

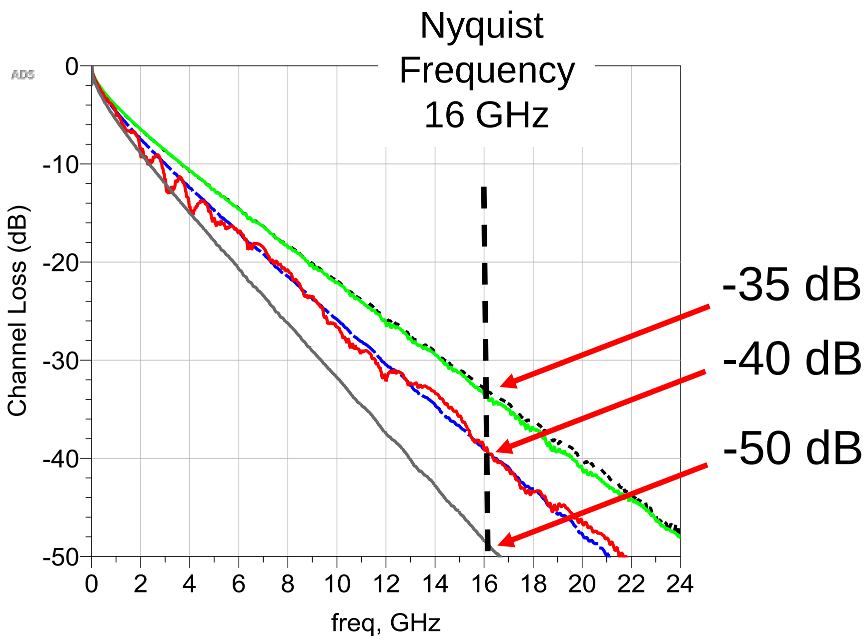
Insert different
signal degradation
pathologies

Auto Adapt
Rx Equalizer

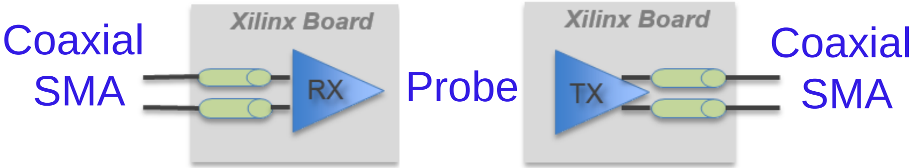
Simulation of High Loss Channel Pathologies for 32 GBaud

Design of Experiments
3 Types of Signal Degradation

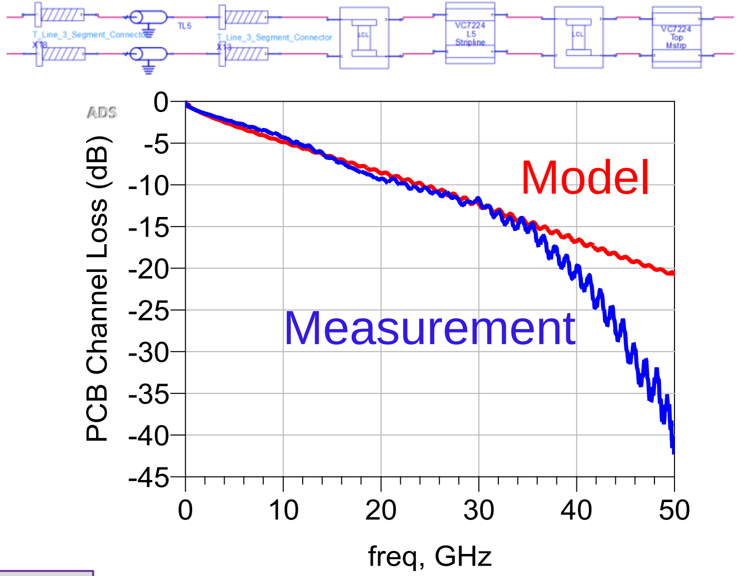
Total Loss	Material Loss	Reflections	XTALK
-35 dB	10in + 4.5in		3W Gap Aggressors
-40 dB	13in +7.25 in	55 and 145 Return Loss	
-50 dB	15.5in + 13in		



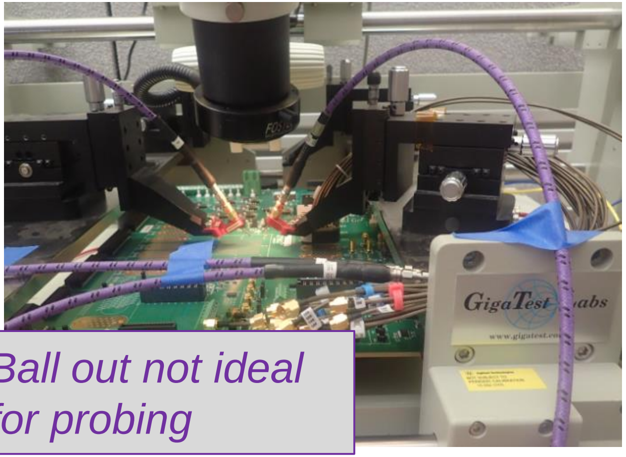
Tx/Rx Model Details and Fixture S-Parameters



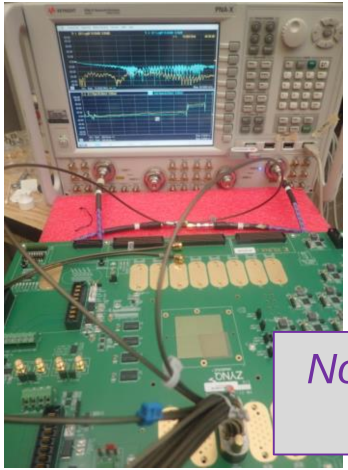
Measurement Based Model



Probing at the BGA Pad



Open at the BGA 1x Reflect



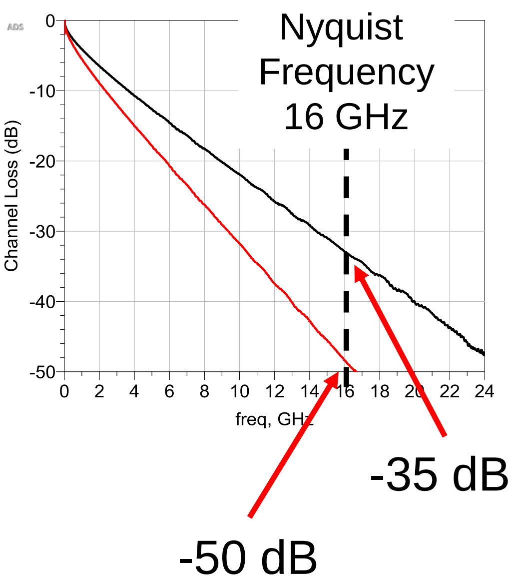
Ball out not ideal for probing

Non-ideal Open

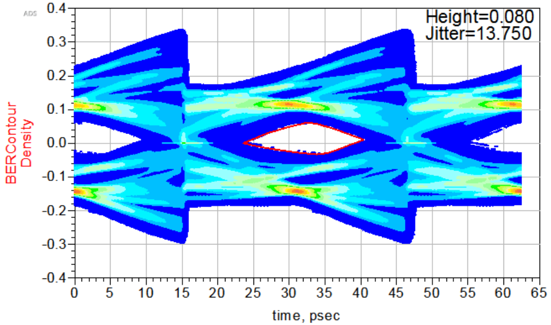
Conservative model to correct for measurement uncertainties.

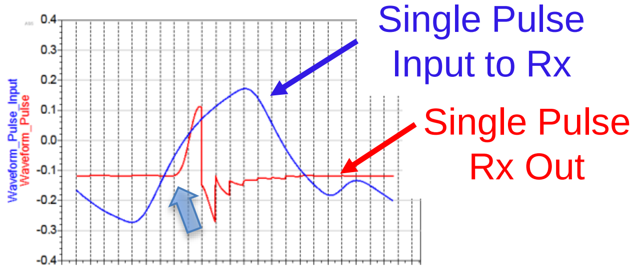
Increasing Tx Equalization Helps ISI Loss

Material Loss ISI



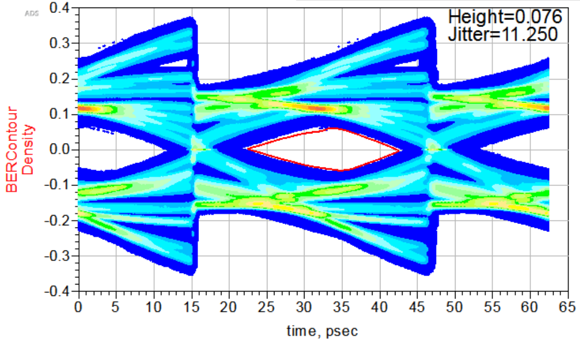
3 dB Tx Precursor, -35 dB Loss

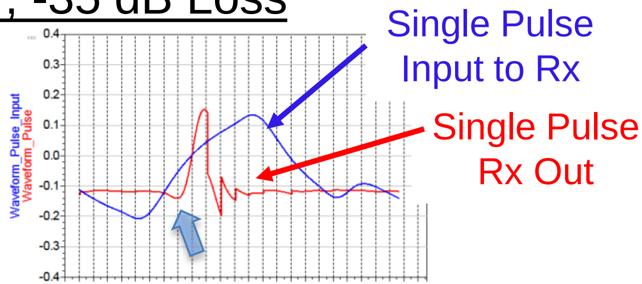




1 UI 31.25 ps per Vertical Grid

6 dB Tx Precursor, -35 dB Loss





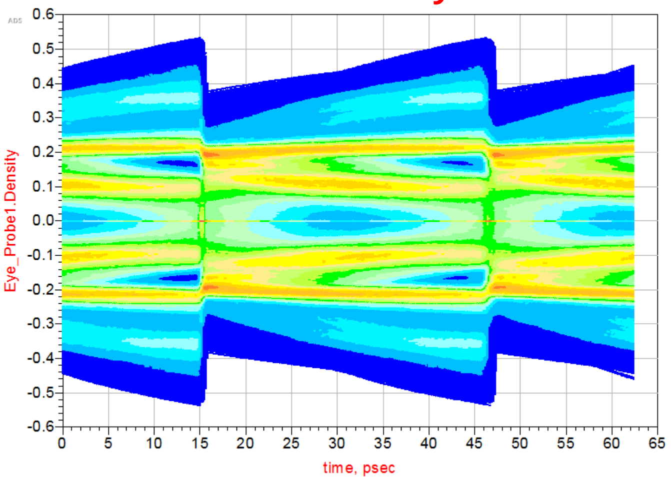
1 UI 31.25 ps per Vertical Grid

Precursor shows up in the leading edge of the pulse.

Maximum Loss – 15.5in + 13in ISI Channels

Tx Precursor = 3 dB

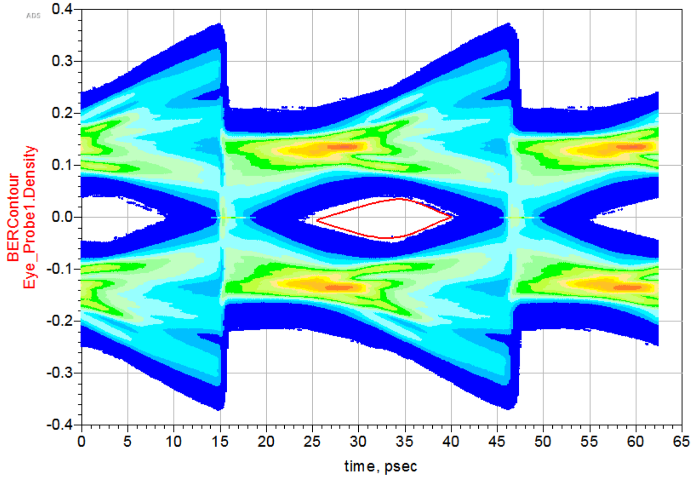
Closed Eye



-50 dB
at
Nyquist
frequency
16 GHz

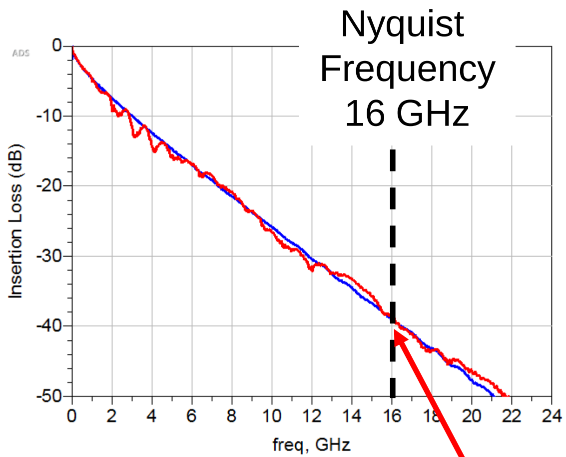
Tx Precursor = 6 dB

Open Eye



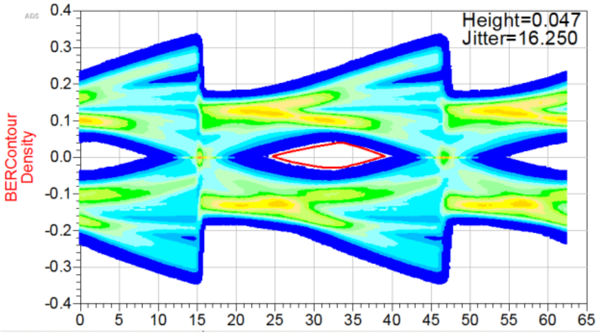
Increasing Tx Equalization Doesn't Help with Reflections

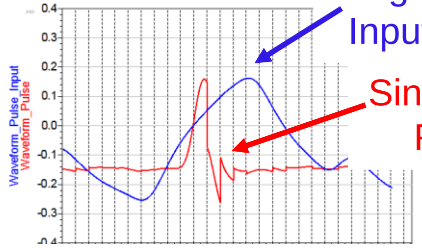
Reflection Loss
Insertion Loss Ripple



-35 dB

3 dB Tx Precursor with Reflections



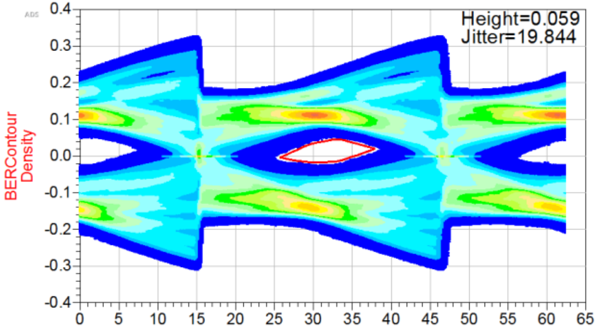


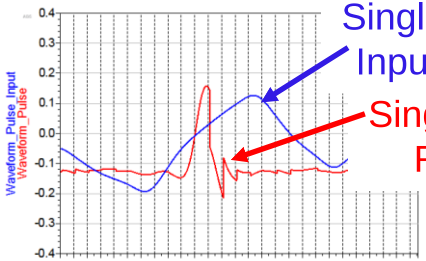
Single Pulse Input to Rx

Single Pulse Rx Out

1 UI 31.25 ps per Vertical Grid

6 dB Tx Precursor with Reflections





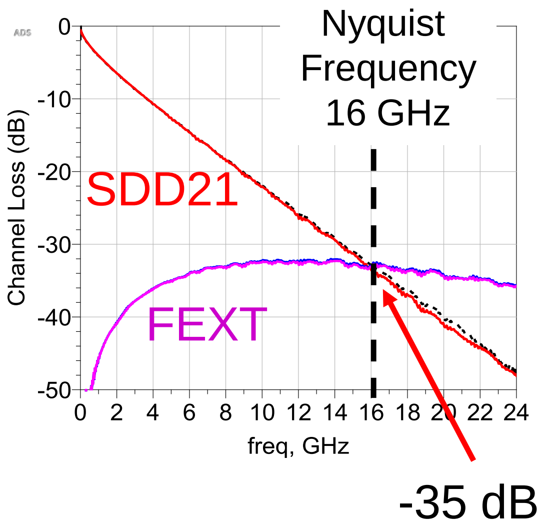
Single Pulse Input to Rx

Single Pulse Rx Out

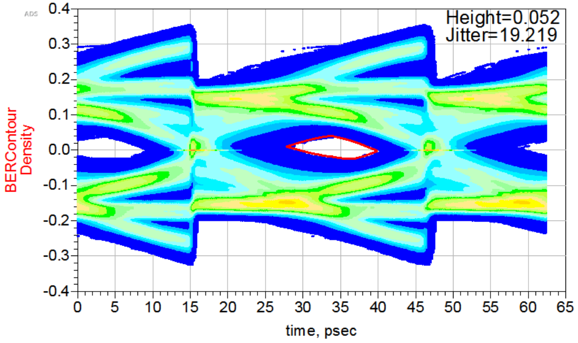
1 UI 31.25 ps per Vertical Grid

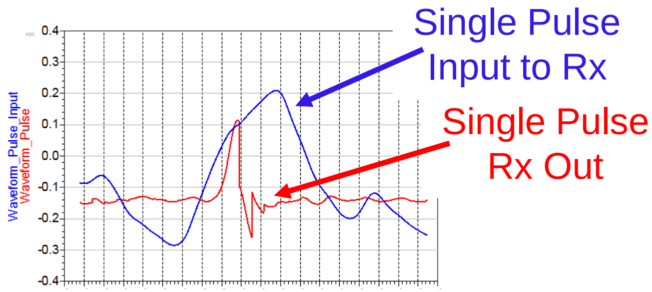
Minimum Tx Equalization Maximizes Signal to Noise

Cross Talk



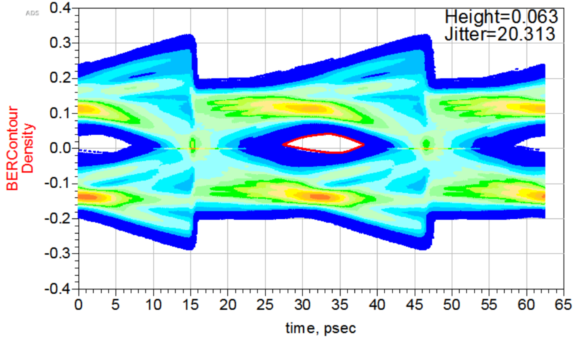
3 dB Tx Precursor with Cross Talk

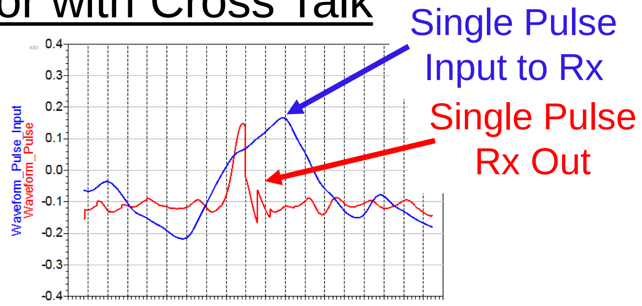




1 UI 31.25 ps per Vertical Grid

6 dB Tx Precursor with Cross Talk



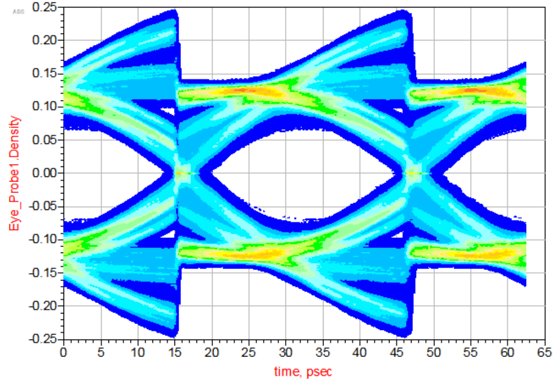


1 UI 31.25 ps per Vertical Grid

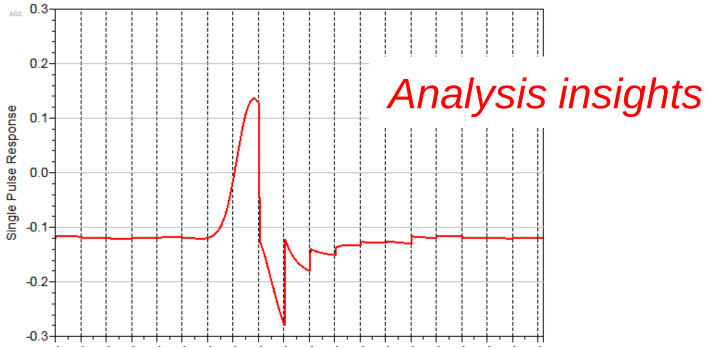
Summary: Minimal Tx FIR with Automated Rx DFE, CTLE

- Real channels have reflections and crosstalk.
- Too much Tx equalization reduces the signal to noise ratio
- Minimize the Tx equalization and maximize the automated Rx DFE equalization.

Equalized Eye



Single Pulse Response



References

- Jack Carrel, et al. “De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement” DesignCon 2014.

- J. Carrel, R. Sleigh, H. Barnes, H. Hakimi, and M. Resso, “Tips and Advanced Techniques for Characterizing a 28 Gb/s Transceiver”, DesignCon 2013 (13-TP5)

- Keysight ADS Simulator
www.keysight.com/find/eesof-sipi-resources

- Xilinx UltraScale+ ArchitectureGTY Transceivers IBIS-AMISignal Integrity Simulation Kit
https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html

- Wild River Technology Modeling Platforms
https://wildrivertech.com/products-2/modeling-platforms/

Agenda

- Full-Link KR Example
- What is a “Pathological Channel”
- Measuring Pathological Channels
- Band Limited S-Parameters
- Using the Pulse Response to Gain Insight

- BREAK

- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Measured Internal Eye
- Summary

Hong Ahn

SerDes Apps. Engineer, Xilinx

Measurement Set up

Using 16nm Xilinx UltraScale+ GTY Transceiver

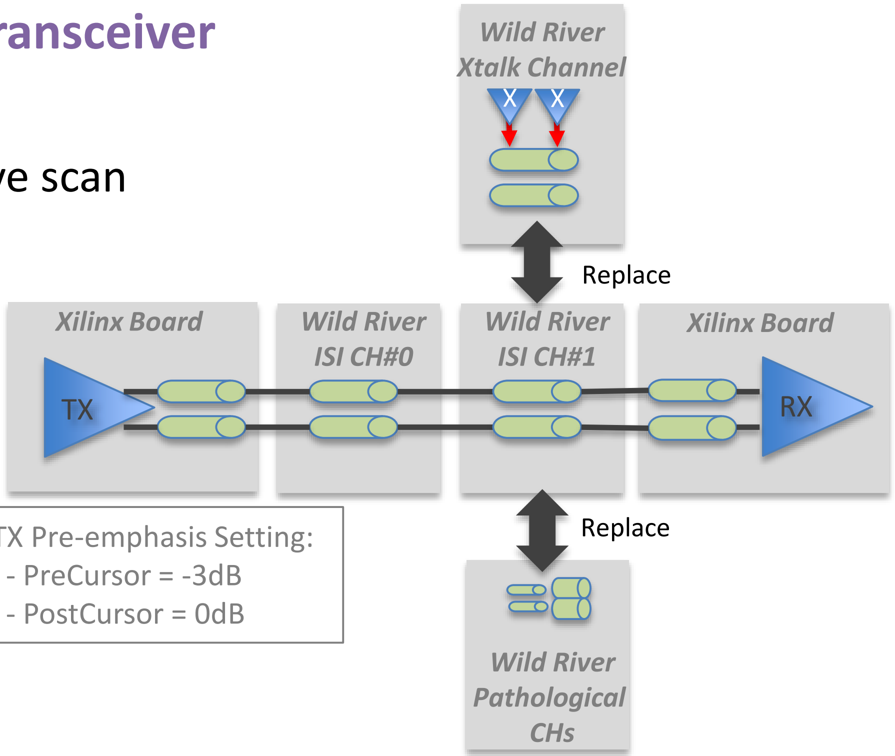
- Line Rate: 32Gbps
- Using Internal non-disruptive 2D eye scan

2D eye scan configuration

- 64 horizontal steps
- 256 vertical steps
- BER is 1E-10

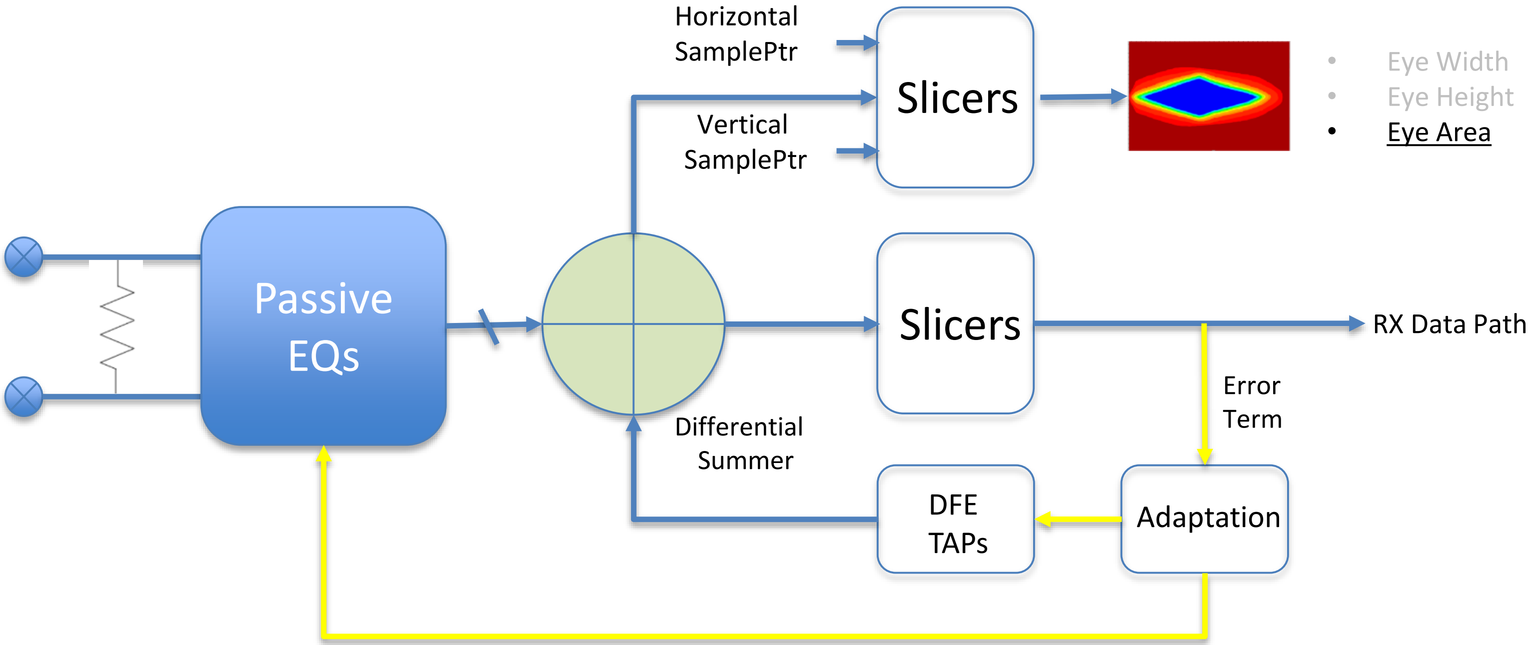
Stress Channel Configuration

- Two Aggressors for NEXT
- Insert Pathological Channel



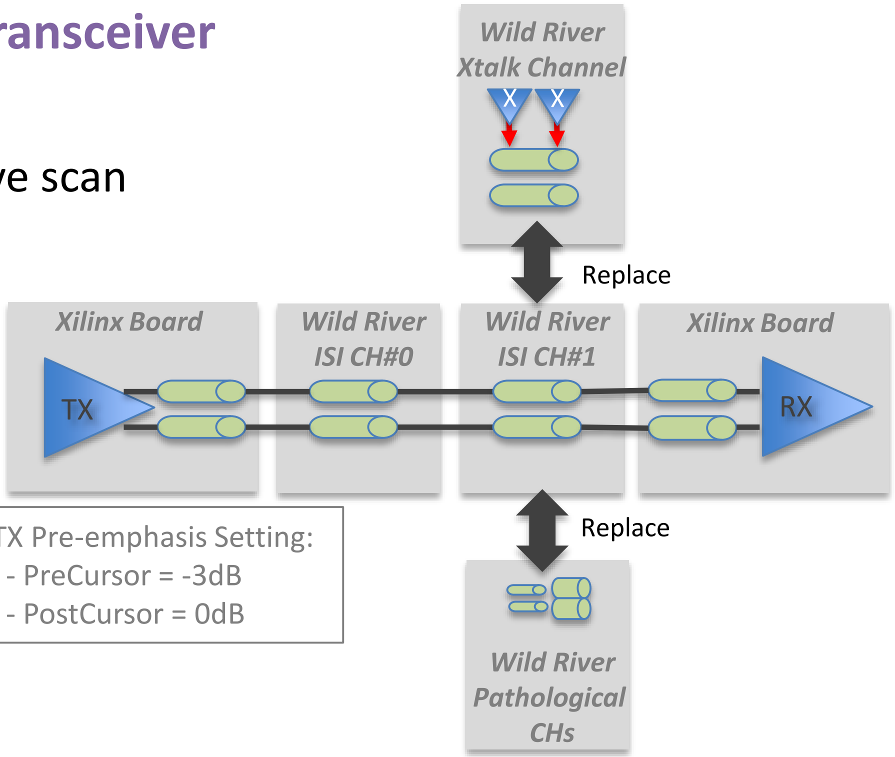
TX Pre-emphasis Setting:
- PreCursor = -3dB
- PostCursor = 0dB

Internal 2-D Eye Scan



Measurement Set up

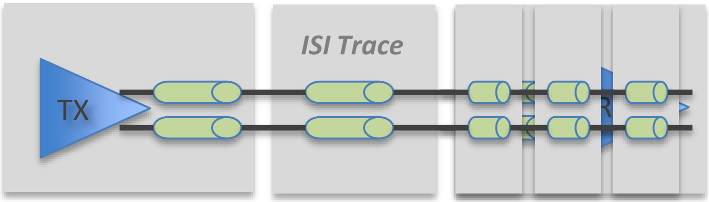
- **Using 16nm Xilinx UltraScale+ GTY Transceiver**
  - Line Rate: 32Gbps
  - Using Internal non-disruptive 2D eye scan
- **2D eye scan configuration**
  - 64 horizontal steps
  - 256 vertical steps
  - BER is 1E-10
- **Stress Channel Configuration**
  - Two Aggressors for NEXT
  - Insert Pathological Channel



TX Pre-emphasis Setting:
- PreCursor = -3dB
- PostCursor = 0dB

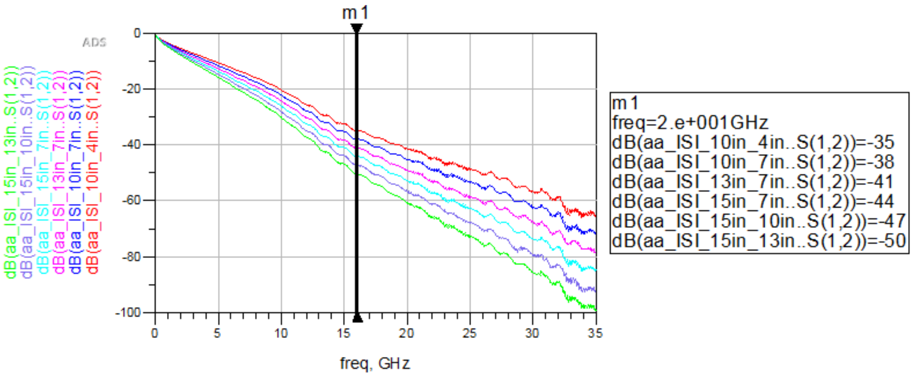
The 1st Pathology: + More Loss

- **Non-intended additional Loss is critical factor in Pathological Space**
  - Loss is treated as a Goal rather than pathology
- **Insert additional trace section to add more loss**

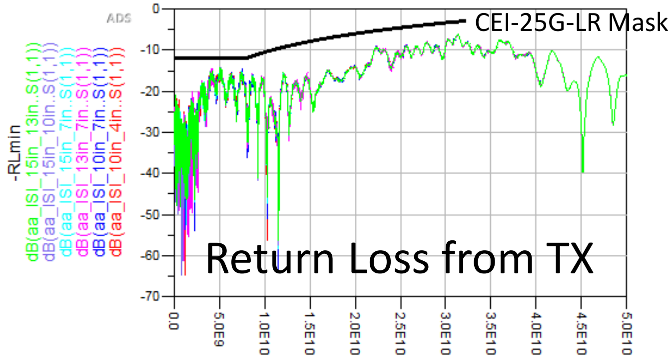


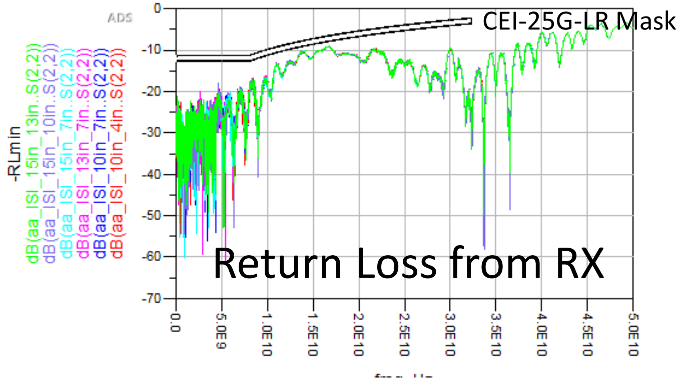
Channel Characteristic by the additional loss

No Crosstalk and Well Optimized Channel



Insertion Loss

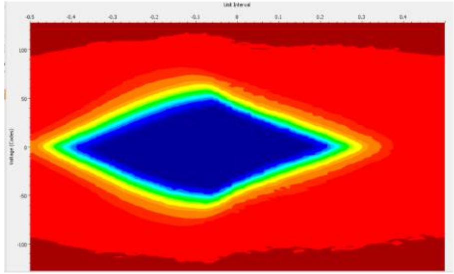




Degradation by the additional loss: 2-D Eye Scan Result

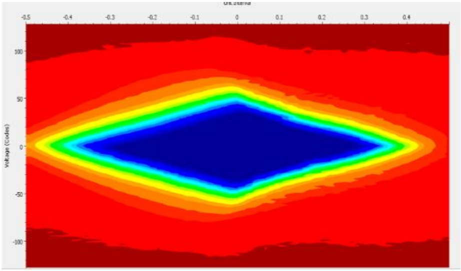
No Crosstalk and Well Optimized Channel

"-35dB" Loss Channel



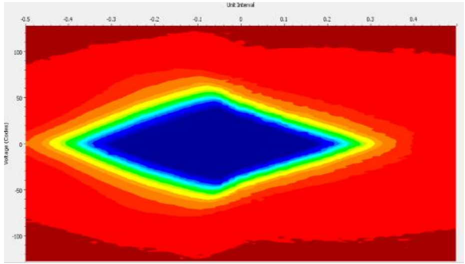
Eye Area = 1320

"-38dB" Loss Channel



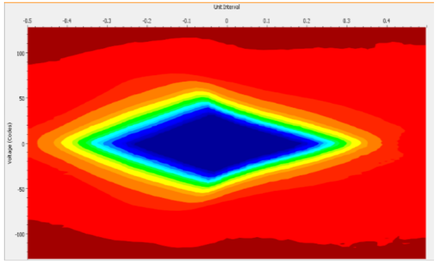
Eye Area = 1004

"-41dB" Loss Channel



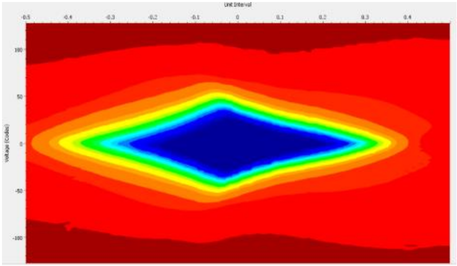
Eye Area = 1048

"-44dB" Loss Channel

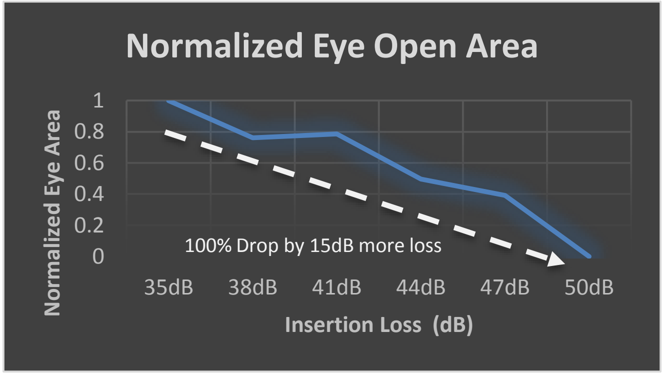


Eye Area = 654

"-47dB" Loss Channel



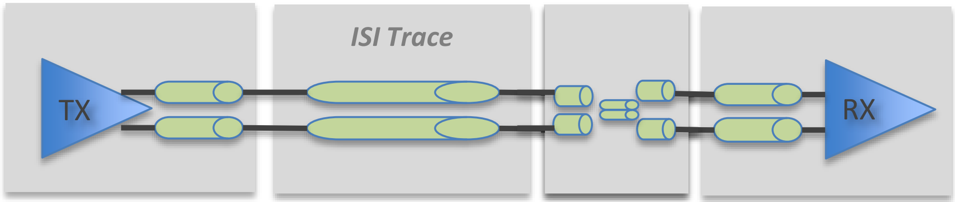
Eye Area = 518



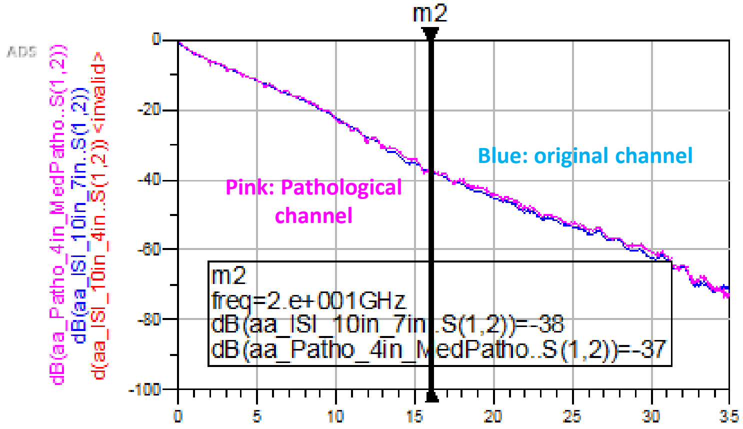
Degradation is not linear
Because of RX EQs

The 2st Pathology: Reflection

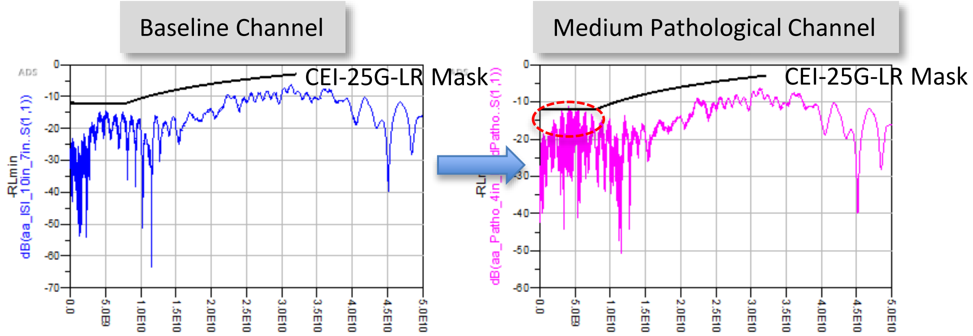
- **Reflection is also critical factor in pathological space**
  - The reflection by non-optimized channel element causes the noticeable degradation
- **Replace the part of trace by the reflective structure**



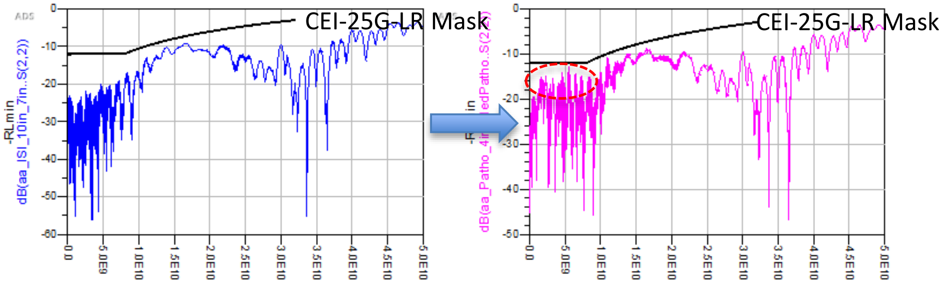
Channel Characteristic by Medium Reflection



Return Loss from TX

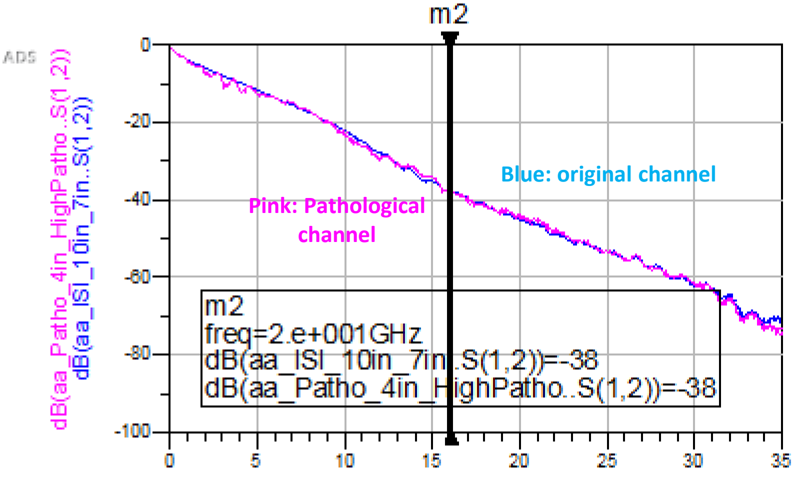


Return Loss from RX

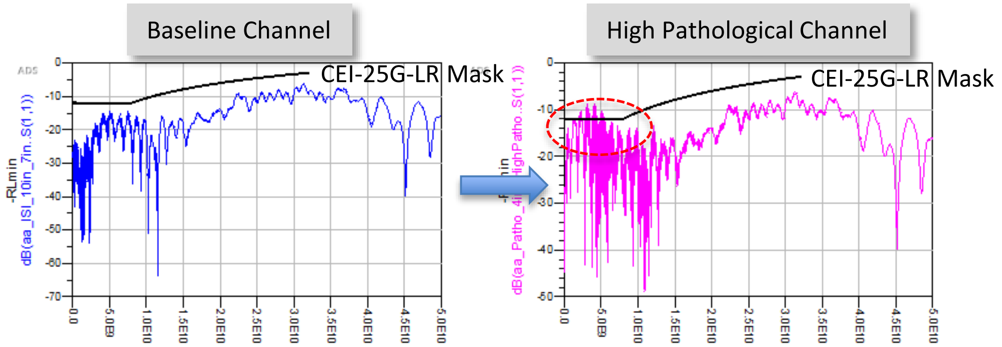


- Insertion Loss is around 38dB
- High Reflection at < 10GHz
- No Crosstalk

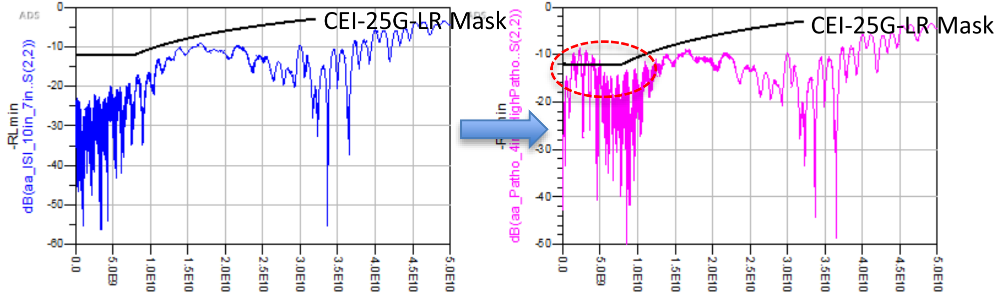
Channel Characteristic by High Reflection



Return Loss from TX



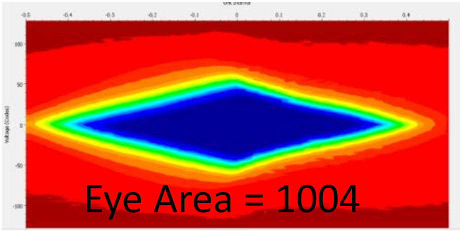
Return Loss from RX



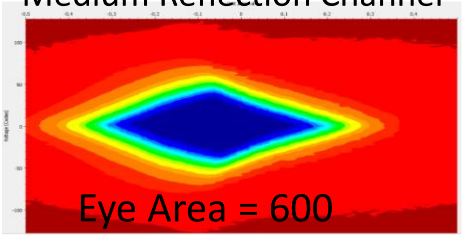
- Insertion Loss is around 38dB
- Severe Reflection at < 10GHz
- No Crosstalk

The Degradation by Reflective Pathological channel

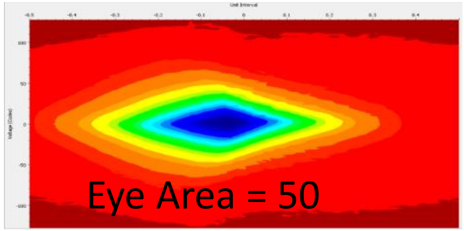
"-38dB" Loss Channel

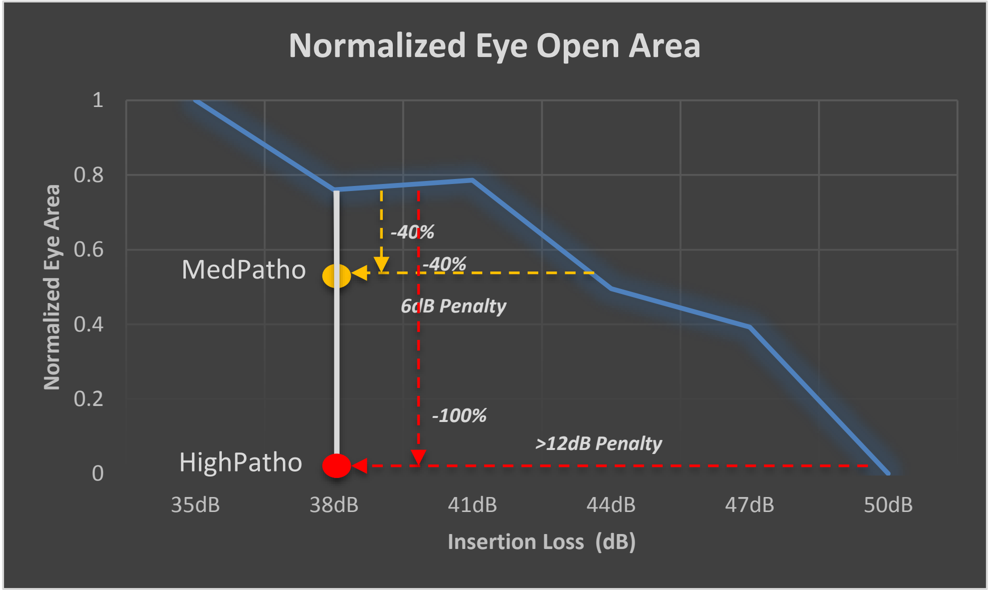


Medium Reflection Channel



High Reflection Channel

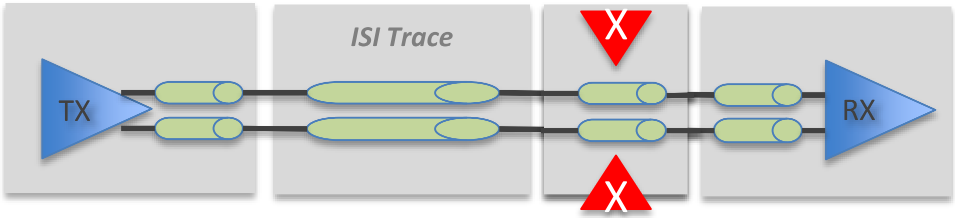




The Reflection steals the margin for the insertion loss

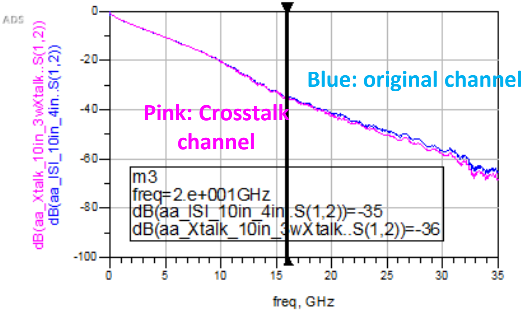
The 3rd Pathology: Crosstalk

- Crosstalk is also one of Critical factor in pathological space
- Replace the part of trace by the coupling structure

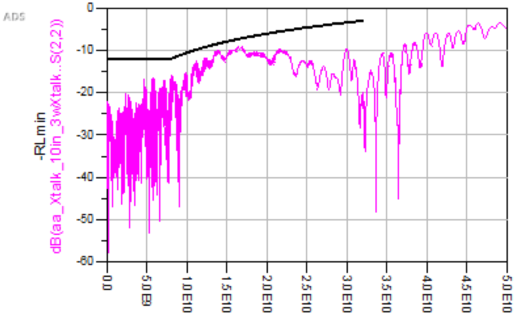


Channel Characteristic by Crosstalk

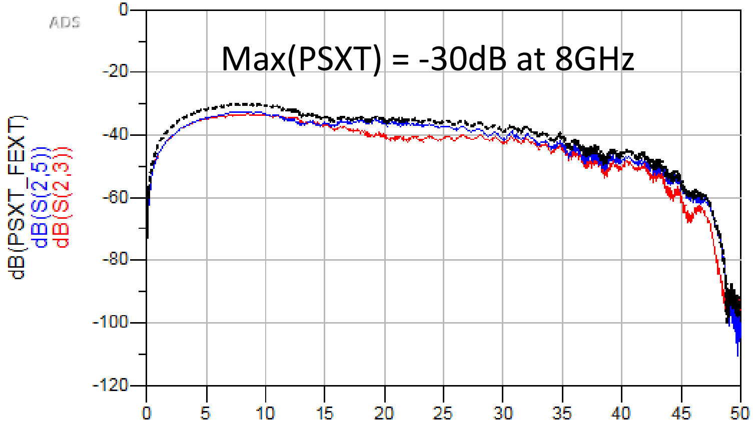
Insertion Loss



Return Loss from RX

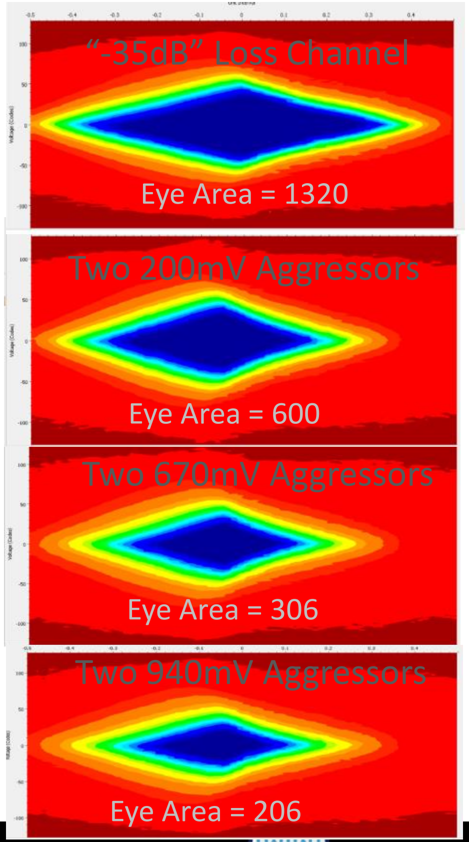


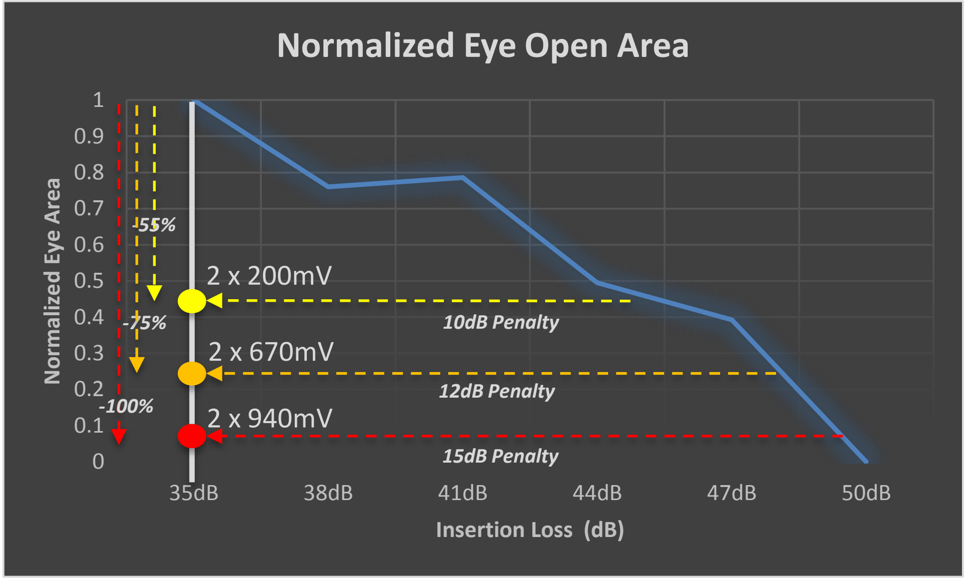
Coupling: Aggressor TX → Victim RX



- Insertion Loss is around 36dB
- The aggressors are located at Receiver side
- Very High Coupling: around -30dB

The Degradation by Crosstalk





The Crosstalk also steals the margin for the insertion loss

Conclusion of Measurement

- **Show Receiver Performance is dropped by any single pathology in Pathological Space**
  - More Loss, Reflection and Crosstalk
- **Well designed channel can achieve dramatic increase in the channel length**
  - By reducing pathological signature
  - By reducing crosstalk
- **Need to find the best combination of “margin eaters” to achieve the longest channel given transceiver performance and architecture**

Spend your margin wisely!

Thank you!

QUESTIONS?

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- Full-Link KR Example
- What is a “Pathological Channel”
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- BREAK

- Serial Link Equalization Techniques
- Simulating with IBIS-AMI Models
- Test Strategies for Pathological Channels
- Test Cases Simulated
- Test Cases Measured Internal Eye
- **Summary**

32 to 56 Gbps Serial Link Analysis and Optimization Methods for Pathological Channels

Top 10 Take-Aways

1. Specifications like 100GBASE-KR are a great plan, but they don’t provide the insights needed to trade off margins or troubleshoot a failed channel.
2. A pathological approach breaks down the signal integrity of a SERDES channel to isolate issues for better optimization of design margins.
3. Expanding tools and methods for S-parameter analysis enable frequency domain, time domain, mixed mode, causality, passivity, and COM visualization of potential signal integrity problems.
4. Measuring S-Parameters to the 3rd Harmonic is conservative for high data rate applications, verifying by simulation can significantly reduce the required bandwidth.
5. The single pulse response gives quick insight to the resulting eye. It identifies loss, mismatch and crosstalk issues and helps with understanding how equalization is able to open the eye.
6. The 3 main types of equalizers are the CTLE, FIR or FFE, and DFE. The pulse response shows how the DFE only works on the falling edge; FIR and CTLE are needed to improve the rising edge.
7. IBIS AMI behavioral models make it fast and easy to simulate high data rate, high loss SERDES Tx/Channel/Rx topologies with sophisticated equalization methods with out divulging vendor IP.
8. The signal integrity of a channel must include analysis of all types of margin eating pathologies such as channel losses, clock noise, and power supply noise.
9. Full link IBIS AMI simulations of separate channel loss pathologies for ISI, Reflection Mismatch, and Crosstalk show that it is best to minimize equalization at the Tx and maximize it at the Rx when reflections and crosstalk are present.
10. Full link measurements of separate channel loss pathologies for ISI, Reflection Mismatch, and Crosstalk show the equivalent ISI loss. Finding the lowest combination of crosstalk and mismatches can greatly increase the working length of the channel.

The End……

Thank you!

QUESTIONS?