

# ALVEO™ U25

2x10/25Gb Ethernet PCIe SmartNIC



## OVERVIEW

For cloud architects building modern data centers, the Alveo U25 provides a comprehensive SmartNIC Platform that brings true convergence of network, storage, and compute acceleration functions onto a single platform.

The U25 SmartNIC platform is based on a powerful FPGA, enabling hardware acceleration and offload to happen in-line with maximum efficiency while avoiding unnecessary data movements and CPU processing. The U25 programming model supports both high-level network programming abstractions such as HLS and P4, as well compute acceleration frameworks such as Vitis™ to enable both Xilinx and 3rd party accelerated applications.

## FEATURES AND BENEFITS

### Enabling the Fastest, Most Secure Networks

#### > A Powerful SmartNIC

The U25 delivers ultra-high throughput, small packet performance and low-latency. The host interface supports standard NIC drivers as well as Onload® kernel bypass to provide both TCP and packet-based APIs for network application acceleration. IEEE1588v2 precision timing protocol (PTP) is provided for applications that require synchronized time stamping of packets with single-digit nanosecond accuracy.

#### > A Programmable Fabric

The U25 SmartNIC contains a programmable FPGA handling all network flows. Each flow can be individually delivered to the host and/or streamed in hardware through bump-in-the-wire network acceleration functions and/or compute acceleration kernels for application processing within the FPGA.

#### > A Platform for Hardware Accelerated Clouds

Cloud service providers are deploying SmartNIC fabrics to achieve virtual switching and micro-segmentation of services that scale linearly with CPU cores and network links. The U25 is a platform for the industry's first converged SmartNIC fabric, including shrink-wrapped applications.



## XILINX ADVANTAGE

- > Combined bump-in-the-wire network, storage, and compute offload and acceleration
- > Complete SmartNIC platform allows full FPGA programmability in HLS/RTL/P4
- > Turnkey solutions and apps provided by Xilinx and 3rd Party
- > Baseline NIC feature parity with market leading XtremeScale™ Ethernet controllers
- > Onload® support for low latency kernel bypass with up to 400% improvement in cloud based applications
- > High precision time-stamping and PTP support

**Acceleration**

- > SDx Compute Acceleration
- > Universal Kernel Bypass
- > DPDK Poll Mode Driver - Packet (Cloud, Telco)
- > Onload® – TCP (Cloud, Telco, Enterprise)
- > Onload®/ TCPDirect - TCP/UDP (Fintech)

**Security**

- > Tamper resistant adapter – Digitally signed firmware

**Time Synchronization and Hardware Timestamping**

- > Hardware timestamping for all packets
- > On-board Stratum 3 stable oscillator
- > Solarflare Software PTP Daemon delivers enhanced stability and clock synchronization accuracy and can be used to synchronize the adapter clock to external time source

**Stateless Offloads**

- > TCP/UDP Checksum Offload (CSO) TCP Segmentation Offload (TSO) Giant Send Offload (GSO)
- > Large Send Offload (LSO) Large Receive Offload (LRO) Receive Side Scaling (RSS)
- > Receive Segment Coalescing (RSC)

**Manageability and Remote Boot**

- > PXE and UEFI
- > NC-SI over MCTP SMBus
- > PLDM over MCTP SMBus MCTP PCIe VDM
- > Management and Utilities
- > Solarflare Boot Manager

**Adapter Hardware**

- > 2x PCIe Gen 3 x8 (x16 connector in bifurcated mode)
- > 2x10/25G SFP28 DA copper or optical transceiver;
- > XtremeScale™ Ethernet Controller
- > Zynq® UltraScale+™ XCU25 FPGA
- > 1x 2GB x 40 DDR4-2400
- > 1x 4GB x 72 DDR4-2400

**Hardware Certifications**

- > FCC, UL, CE
- > RoHS - Complies with EU directive 2011/65/EU

**Traffic Engineering**

- > XtremePacket™ Engine for parsing, filtering, and flow steering
- > TCP/UDP/IP, MAC, VLAN, RSS filtering Accelerated Receive Flow Steering (ARFS) Transmit Packet Steering

**Virtualization**

- > Linux Multiqueue
- > SR-IOV: 16 physical functions; 240 virtual functions 2048 Guest OS protected vNICs
- > VXLAN, tunneling offload; adaptable to custom overlays.
- > VLAN and VLAN Q-in-Q Insertion/Stripping

**Ethernet Standards**

- > IEEE802.3-2018 Ethernet Base Standard
- > IEEE 802.3by Ethernet consortium 25 Gigabit Ethernet
- > IEEE 802.3ad, 802.1AX Link Aggregation
- > IEEE 802.1Q, 802.1P VLAN Tags and Priority IEEE 1588-2008 PTPv2
- > Jumbo Frame support (9000 bytes)

**OS Support**

- > Red Hat RHEL and Linux variants

**Physical Dimensions**

- > L: 6.60 inch (167.65 mm)
- > W: 2.54 inch (64.4mm)

**Environmental Requirements**

Temperature:

- > Operating: 0°C to 55°C (32°F to 131°F)
- > Storage: -40°C to 65°C (-40°F to 149°F)

Humidity:

- > Operating: 10% to 80%
- > Storage: 5% to 90%

**TAKE THE NEXT STEP**

Learn more about the Xilinx Alveo U25, [www.xilinx.com/Alveo](http://www.xilinx.com/Alveo)

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