STAR-Dundee

SpaceWire Engineering Excellence

# SpaceFibre Interface IP Cores

## SpaceFibre

**SpaceFibre** is a very **high-speed serial link** designed specifically for use onboard spacecraft (ECSS-E-ST-50-11C). SpaceFibre provides **multi-Gigabit, point-to-point and networked interconnections** for instruments, mass-memory units, processors and other equipment on board a spacecraft. SpaceFibre carries user data in packets which have the same format as SpaceWire packets (ECSS-E-ST-50-12C), making **SpaceFibre and SpaceWire compatible at the network level**. This means that applications developed for SpaceWire can be readily transferred to and run over a SpaceFibre network or mixed SpaceWire and SpaceFibre network. The packets are carried across each data link in one or more virtual channels which support important **quality of service features** targeted at payload data-handling applications. SpaceFibre provides a **low-latency broadcast capability** which can be used to distribute spacecraft time, signal events, report errors, etc. and carry SpaceWire time-codes. SpaceFibre operates at more than 15 times the data-rate of SpaceWire and can run over fibre optic (long distances) or copper media (several metres).

SpaceFibre Quality of Service (QoS) is independently configurable for each Virtual Channel. The following mechanisms can be configured and combined:

- Scheduling
- Priority
- Bandwidth Reservation

SpaceFibre has an **error recovery mechanism** that automatically recovers from transient errors in less than 3 µsec. It does this without losing user data. As well as providing increased data rates, SpaceFibre Multi-Lane operation provides graceful degradation in the event of a persistent or permanent failure of a lane. Hot and cold lane redundancy are also supported. Combined with SpaceFibre's QoS capabilities, in the event of a lane failure a Multi-Lane link will guarantee that the remaining link bandwidth is allocated to high priority virtual channels, ensuring that even in the event of a failure, critical data is still passed over the link.

SpaceFibre is a data and control plane technology in the updated **VITA 78 standard** (**SpaceVPX**) which is to be issued soon.

## STAR-Dundee IP cores

STAR-Dundee IP cores are fully compliant to the SpaceFibre standard and, where appropriate, industry standard data interfaces, such as AXI-4 stream, are incorporated. The IP cores are highly optimised for performance and size. They have been produced by the design team that created the SpaceFibre standard.

# SpaceFibre Single-Lane IP Core

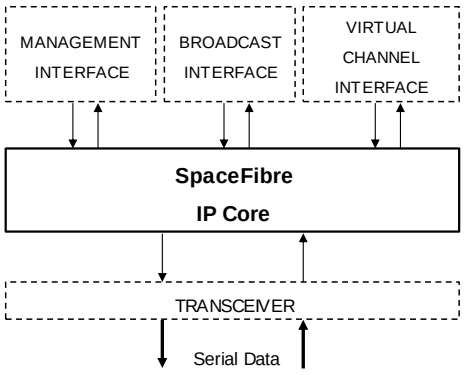
The STAR-Dundee SpaceFibre Single-Lane IP core has the following features:

- Compliant with the SpaceFibre standard.
- Supports lane rates of up to **6.25 Gbit/s in XQRKU060** and **3.125 Gbit/s in Virtex-5QV.** If higher lane data rates are required, please contact STAR-Dundee.
- **Validated in major Xilinx FPGA families** including space-qualified devices (**XQRKU060** and **Virtex-5QV**) and commercial families (Spartan-6, Kintex-7, Artix-7, etc.).
- **Guaranteed timing closure** with EDAC enabled and worst-case conditions.
- Optimised for **low latency** operation.
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit **AXI4-Stream**).
- **Independent, user-defined AXI clocks** for data read and write.
- 80-bit broadcast interface for **ultra-low latency short messages** (< 400 ns).
- **Easy to use** with a protocol agnostic interface. No prior knowledge of the SpaceFibre standard is required. The SpaceFibre packet size, format and content is arbitrary.
- Very **simple management interface**, with optional statistics and debug signals.
- **Highly configurable**, giving flexibility through generics in the VHDL source. The following characteristics can be configured:
  - Number of Virtual Channels,
  - Size of the Virtual Channel buffers and internal buffers.
- The **Quality of Service** parameters can be configured in real time during operation.
- Able to start one end of the link in a **low-power mode** waiting for the other end to become active.
- **Automatic recovery from transient errors** in less than 3 µs, without any significant effect on the user data rate.
- **Data integrity and reliable data delivery** for BER better than $10^{-5}$ and automatic lane disconnection when BER is worse than $10^{-5}$.
- Data and broadcast **babbling node protection**.

The IP is natively compatible with Xilinx devices using the inbuilt transceiver blocks. Only four FPGA pins (two differential pairs) are required per SpaceFibre lane. The transceiver interface uses:

- 8B10B encoding (32-bit interface), clock correction and symbol alignment which are done in the Xilinx transceiver.
- One clock, which is at the lane rate/40.

The interfaces to the Single-Lane IP Core are shown below.



**Resources Required**

The resources required by the SpaceFibre Single-Lane IP including transmit and receive FIFOs are detailed below for different technologies and number of Virtual Channels (VCs).

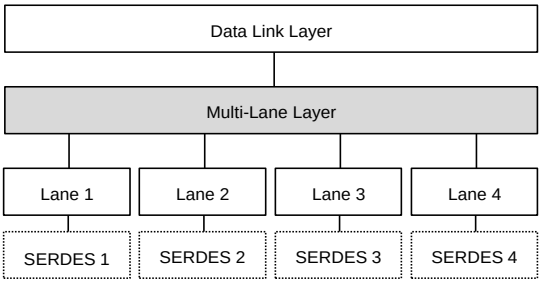
| | XQRKU060 [1] | | | Virtex-5QV | | |
|---|---|---|---|---|---|---|
| | **LUT** | **DFF** | **BRAM** | **LUT** | **DFF** | **RAM Block** |
| **1 VC** | 1615<br>0.5% | 2037<br>0.3% | 4<br>0.2% | 2750<br>3.4% | 2365<br>2.9% | 4<br>1.3% |
| **2 VC** | 1961<br>0.6% | 2467<br>0.4% | 6<br>0.3% | 3138<br>3.8% | 2596<br>3.2% | 6<br>2.0% |

[1] TMR has not been inserted

**Resources used for a SpaceFibre Single-Lane IP Core**

# SpaceFibre Multi-Lane IP Core

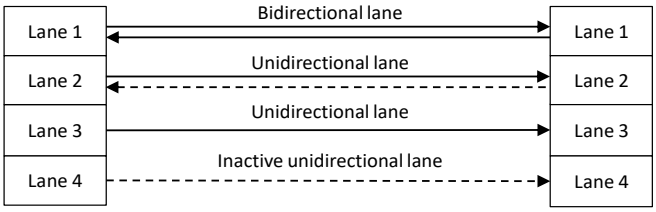
Multi-Lane is an optional capability of the SpaceFibre link defined in the SpaceFibre protocol stack. The Multi-Lane layer is defined between the Data Link layer and the Lane layer implemented for each available lane.




The Multi-Lane layer coordinates the operation of multiple lanes to form a single SpaceFibre link, with higher data throughput and redundancy. Because the logic to initialise a lane and monitor its status is located below the Multi-Lane layer, each lane can be initialised and operated independently of each other.

The Multi-Lane IP core supports automatic graceful degradation, hot and cold redundancy, unidirectional lanes and dynamic management of power versus bandwidth, all essential capabilities for space applications.

Single-Lane SpaceFibre implementations must be bidirectional even when the end-user data flow is unidirectional, because of the feedback required by the protocol. However, in a Multi-Lane implementation, it is sufficient to have only one bidirectional lane, the other lanes can be unidirectional, saving power and mass.




In this 4-lane configuration example, bidirectional lane 2 can be set to a unidirectional lane for power saving reasons. Unidirectional Lane 4 can be enabled when one lane fails or a higher data rate is required. It is also possible to send data using all four lanes and add an additional one configured as a hot redundant lane, which only sends data when another lane fails.

## Multi-Lane Interface IP Core Features

The STAR-Dundee SpaceFibre Multi-Lane IP core has been designed to be easy to use. On top of the features of the Single-Lane IP Core, the Multi-Lane IP also features:

- **Validated in major Xilinx FPGA families**
- Supports lane rates of up to **6.25 Gbit/s in XQRKU060** (e.g. aggregate rates of 12.5 Gbit/s using 2 lanes, 25 Gbit/s using 4 lanes and **50 Gbit/s using 8 lanes**).
- **Guaranteed timing closure** with EDAC enabled and worst-case conditions.
- Wide AXI4-Stream interface which **supports slow user clock**.
- Only a **single clock for all lanes** is required.
- Configurable number of lanes with **hot and cold redundancy**. Any number of lanes supported (up to 16).
- Several configuration options available through generics for **tailoring the IP to the user's needs**, allowing additional resource savings.
- Lanes can be configured as **unidirectional lanes to save power** and mass in asymmetric data flows.
- **Rapid, automatic graceful degradation**.
- Hot redundant lanes recover from lane failures in less than 3 µs without user intervention.

**Resources Required**

The resources required by a SpaceFibre design including transmit and receive FIFOs are detailed below for different numbers of lanes and Virtual Channels.

| | XQRKU060 [1] | | | Virtex-5QV | | |
|---|---|---|---|---|---|---|
| | **LUT** | **DFF** | **RAM Block** | **LUT** | **DFF** | **RAM Block** |
| **2 Lanes 1 VC** | 3216<br>1.0% | 4527<br>0.7% | 8<br>0.7% | 3858<br>4.7% | 3938<br>4.8% | 8<br>2.7% |
| **2 Lanes 2 VC** | 3661<br>1.1% | 5295<br>0.8% | 12<br>1.1% | 4503<br>5.5% | 4382<br>5.3% | 12<br>4.0% |
| **3 Lanes 2 VC** | 4530<br>1.4% | 6367<br>1.0% | 12<br>1.1% | 5416<br>6.6% | 5226<br>6.4% | 12<br>4.0% |
| **4 Lanes 1 VC** | 5767<br>1.7% | 7552<br>1.1% | 16<br>1.5% | - | - | - |
| **8 Lanes 1 VC** | 12432<br>3.7% | 13603<br>2.1% | 32<br>3.0% | - | - | - |

[1] TMR has not been inserted

**Resources used for a SpaceFibre Single-Lane IP Core**

## IP Core Delivery Files

The STAR-Dundee SpaceFibre Interface IP Cores include a reference design for Kintex UltraScale (Vivado) and Virtex-5QV (ISE) that can directly be implemented in the FPGA for easy adoption. The UltraScale reference design includes additional control logic for optimal transceiver operation, which minimises lane and link recovery times in the event of lane transient, persistent or permanent failures.

A comprehensive end-user test bench for ModelSim/Questa simulators is also provided.

## Licensing

STAR-Dundee SpaceFibre Single-Lane and Multi-Lane IP Cores are available under license. For more information on the IP cores, licensing, or if you have specific or custom requirements, please contact us.

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