

# XQ Defense-Grade Versal™ Portfolio

## DEFENSE-GRADE

The defense-grade Versal™ portfolio, inclusive of XQ Versal AI Core, XQ Versal AI Edge, XQ Versal Prime, and XQ Versal Premium, enables designers with a broad selection of devices to advance state-of-the-art integrated Aerospace & Defense solutions. This portfolio includes the industry's first Adaptable Compute Acceleration Platform (ACAP) devices with flexible and dynamically reconfigurable high-performance AI/ML compute engines; DSP engines; programmable logic; 32Gb/s, 58 Gb/s, and 112Gb/s transceivers; dual-core Arm® Cortex®-A72 and dual-core Arm Cortex-R5 embedded processors in every device; and ruggedized packages with support for -55C to +125C operation.

XQ defense-grade devices offer extended temperature range and a package design to enable survivability in harsh environments. AMD invests in these unique packages specifically for the Aerospace and Defense communities.

Each XQ device has a footprint-compatible XC device. AMD has 30+ years of continuous focus and heritage in A&D applications, with a history of government and industry partnership and collaboration, which has led to unique advancements in the capability, reliability, and security of XQ devices.

### Available Defense-Grade Features Include:

- > Ruggedized packaging
- > Military-temperature, -55°C to +125°C
- > Full range extended temperature testing
- > MIL-STD-883 Group D qualification testing
- > Full compliance with MIL-PRF-38535 Pb content standards
- > Mask set control
- > Anti-counterfeiting features
- > Longer-term availability
- > Information assurance (IA) support
- > Anti-tamper (AT) technology

AMD maintains a focus on security and safety, with dedicated support and expertise in these related, yet unique, domains. This defense-grade offering expands on a multi-generational commitment and heritage in IA methodology and AT technology, with the introduction of physically unclonable function (PUF) and differential power analysis (DPA) masking, supported in XQ Versal devices. A functional safety focus assists the advancement of our industry-leading DO-254 and DO-178 solutions.



## AMD DEFENSE-GRADE HIGHLIGHTS

- > Industry's leading defense-grade portfolio, with high performance, maximum integration, and industry-leading AI/ML capabilities
- > Ruggedized packaging
- > Military-temperature, -55°C to +125°C
- > MIL-STD-883 Group D qualification testing
- > Fully compliant with MIL-PRF-38535 Pb content requirements
- > Mask set control
- > Anti-counterfeiting features

## XQ VERSAL PORTFOLIO

- > XQ Versal AI Core
- > XQ Versal AI Edge
- > XQ Versal Prime
- > XQ Versal Premium

## FULL RANGE TEMPERATURE, TESTING AND QUALITY

XQ Versal devices are offered in Military (M) and Industrial (I) temperature grades:

> **Military:** -55°C to +125°C

> **Industrial:** -40°C to +100°C

Full range extended temperature testing is offered on XQ ruggedized devices and includes full functional and parametric testing at room temperature as well as the hot and cold temperature extremes. AMD tests 100% of all die at wafer sort and 100% of all devices at final production testing. AMD continuously improves the test coverage of its products through advancements in design for test (DFT) methods spanning digital logic, IP cores, memory elements, I/O cells, and many other areas. AMD achieves very high test coverage with industry-leading manufacturing and foundry processes, as confirmed by our low PPM failure rate and low customer return rates; for more information see [www.xilinx.com/quality](http://www.xilinx.com/quality).

## MASK SET CONTROL

Mask-set control is valuable for secure and critical applications where any mask-set change may trigger a detailed silicon-level analysis, re-verification, and/or re-certification process. XQ ruggedized products have a locked mask-set throughout the production life cycle. In the event that any change must be made, a formal customer notification process is required for these XQ devices.

## FULLY ADDRESSING MIL-PRF-38535 PB REQUIREMENTS

PACKAGE ELEMENT	XC	XQ RUGGEDIZED
Package Substrate	ROHS	Mitigated
Chip Cap Finish	ROHS	Mitigated
Wafer Bumps	ROHS	Mitigated
Solder Balls	ROHS	Mitigated
Assembly Re-Flow	ROHS	Mitigated

Aerospace and Defense applications may require compliance to government flow downs where materials cannot contain more than 97% tin (Sn), due to a risk that tin whiskers may develop in the case of greater than 97% Sn, such as in ROHS solder interfaces. Components with solder terminals comprised of 3% Pb are not prone to tin whisker growth. AMD XQ ruggedized packages utilize Pb and other assembly methods to address this. All interconnects within the XQ ruggedized package are fully compliant with the Pb requirements of MIL-PRF-38535, and our devices do not have any unmitigated solder finished exposed. In addition, the most commonly used lead-free solders are known to be more brittle than Sn/Pb solders, therefore in high vibration and shock applications, the ductile Sn/Pb solder joints or other mitigations may be required.

## XQ RUGGEDIZED PACKAGE LID

XQ ruggedized packages utilize open lid technologies, such as lidless stiffener ring and bare-die substrate packages. This opened lid simplifies board-level assembly process for applications requiring conformal coating. In the conformal coating process, boards go through a caustic etching process to achieve the required conformal coating adherence. The caustic etching material or other corrosive chemicals can become trapped inside of non-ruggedized packaging, leading to reliability concerns with flip-chip packaging. With the XQ ruggedized package, the selected lid technology significantly simplifies cleaning and manufacturing process, allowing the device to be fully flushed prior to sealing the device/board with conformal coating.

## MIL-STD-883 GROUP D QUALIFICATION TESTING

XQ ruggedized devices include the following tests and qualification prior to production release:

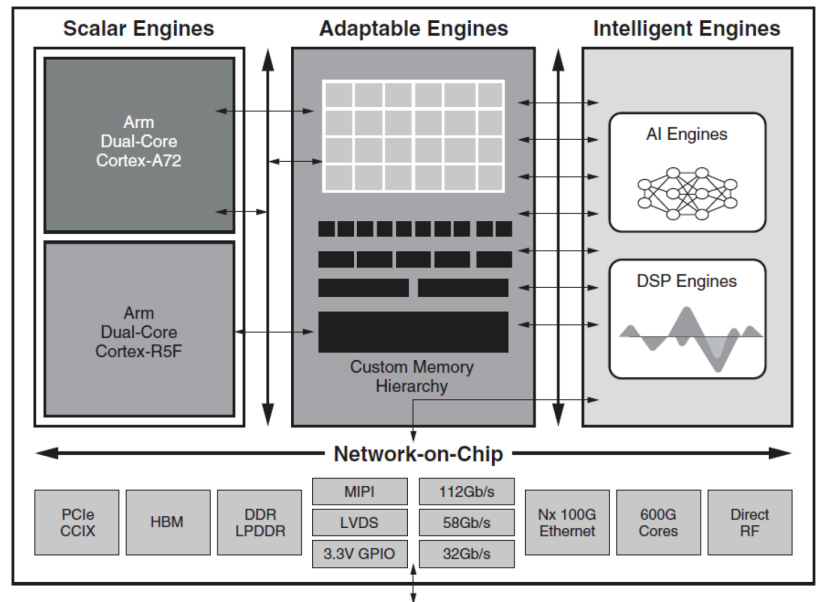
- > Physical Dimensions (TM 2016)
- > Temperature Cycling (TM 1010 Condition C 100 cycles)
- > Vibration - Variable Frequency (TM 2007 Condition A minimum)
- > Salt Atmosphere (TM 1009 Condition A minimum)
- > Thermal Shock (TM 1011 Condition B 15 cycles)
- > Moisture Resistance (TM 1004)
- > Constant Acceleration - Centrifuge (TM 2001 Condition D minimum - Y1 orientation only)

## ANTI-COUNTERFEITING FEATURES

XQ Versal devices offer multiple levels of anti-counterfeiting protection. Protection starts with the device packaging and marking, with limited information marked on the device. Detailed information is only available within the 2D bar code marking. This aspect makes it significantly more difficult for counterfeiters, who can no longer simply re-mark a commercial device and sell it as a defense-grade product. Supplementing this is a unique laser marking, which utilizes micro watermarking characters and complex patterns, whereby certain elements may be verified by the end-user and others only verified by certain AMD staff. This allows for complete supply-chain confidence and virtually eliminates the possibility of counterfeiting of XQ Versal devices.

## XQ VERSAL ACAP ARCHITECTURE

Versal Adaptable Compute Acceleration Platform (ACAP), is a fully software-programmable, heterogeneous compute platform that combines Scalar Engines, Adaptable Engines, and Intelligent Engines to achieve dramatic performance improvements of up to 20X over today's fastest FPGA implementations and more than 100X over today's fastest CPU implementations—for data center, wired network, 5G wireless, and automotive driver assist applications. ACAPs feature a mix of next-generation Scalar Engines, Adaptable Engines, and Intelligent Engines. The NoC connects them all together via a memory-mapped interface with an aggregate bandwidth of 1Tb/s+. In addition to the NoC, the massive memory bandwidth enabled by programmable logic (and integrated RAM blocks) enables programmable memory hierarchies optimized for individual compute tasks (avoiding the high latency and latency uncertainty inherent in other cache-based compute units).



The Scalar Engines are built from the dual-core Arm® Cortex-A72, providing a 2X increase in per-core single-threaded performance compared to AMD's previous-generation Arm Cortex-A53 core. A combination of advanced architecture and power improvements from the 7nm FinFET process yields a 2X improvement in DMIPs/watt over the earlier 16nm implementation. The ASIL-C certified<sup>1</sup> UltraScale+™ Cortex-R5F Scalar Engines migrate forward to 7nm with additional system-level safety features based on learning from AMD's current automotive volume deployments.

The Adaptable Engines are made up of programmable logic and memory cells connected with the next generation of the industry's fastest programmable logic. In addition to supporting legacy designs, these structures can be reprogrammed to form memory hierarchies customized to a particular compute task. This allows AMD's Intelligent Engines to achieve a much higher cycle efficiency and a much higher memory bandwidth per unit compute than the latest GPUs and CPUs. This is key to optimizing for latency and power at the edge and for optimizing for absolute performance in the core.

The Intelligent Engines are an array of innovative very long instruction word (VLIW) and single instruction, multiple data (SIMD) processing engines and memories, all interconnected with 100s of terabits per second of interconnect and memory bandwidth. These permit 5X–10X performance improvement for machine learning and digital signal processing (DSP) applications. These compute functions are mixed in different ratios and magnitudes to form the Versal portfolio of devices.

<sup>1</sup> [www.xilinx.com/news/press/2018/xilinx-announces-availability-of-automotive-qualified-zynq-ultrascale-mpsoc-family](http://www.xilinx.com/news/press/2018/xilinx-announces-availability-of-automotive-qualified-zynq-ultrascale-mpsoc-family)

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