

Alveo U25N SmartNIC: 25Gb Network and Security Acceleration

OVS and IPsec Acceleration

INTRODUCTION

Higher network speeds, ever-increasing bandwidth requirements, the growth and complexity of virtualized workloads, and the prevalence of disaggregated architectures all place a tremendous amount of pressure on data center CPU resources. In practice, a substantial portion of valuable CPU resources is used to process common networking and security functions instead of high-value, revenue-generating business applications. Many Cloud Service Providers (CSPs) are discovering that deploying SmartNICs to handle these networking and security functions deliver a superior return on their infrastructure investment by enabling them to monetize their CPUs to service only critical business applications.

The Xilinx Alveo U25N SmartNIC platform enables CSPs to offload computationally intensive networking and security functions processing onto hardware freeing up expensive CPU cores to service virtual machines running critical business applications.

SOFTWARE DEFINED HARDWARE ACCELERATION

Larger cloud providers often have the resources to develop and deploy their own custom offloads and software solutions on top of programmable SmartNICs. But for the majority of CSPs, and large enterprise data centers, the availability of turnkey, out-of-the-box acceleration solutions that can be readily deployed to offload specific workloads are key to realizing the potential of SmartNICs.

Regardless of their scale, all cloud providers need the flexibility to adapt to rapidly evolving use cases and requirements in their cloud deployments. This requires the need for not only turnkey acceleration solutions via hardware offload but also providing sufficient flexibility for customers to “adapt” their solutions specific to their deployment needs.

ALVEO U25N – DUAL PORT 25Gb SMARTNIC

For cloud and enterprise architects building modern data centers, the Alveo U25N provides a comprehensive SmartNIC platform that brings true convergence of network and security acceleration functions into a single platform.

The U25N SmartNIC platform is based on the fusion of technologies, a powerful System on a Chip (SoC) that includes an FPGA and multi-core Arm processor, and a proven XtremeScale™ X2 Ethernet Controller. The FPGA enables hardware acceleration and offload to happen in line with maximum efficiency. The Arm cores are responsible for managing FPGA and the control plane for the accelerations. The X2 Ethernet Controller provides a basic NIC function for two ports of 25 Gigabit Ethernet via field-proven software drivers.



KEY BENEFITS

- > Improving CPU efficiency with hardware-based offload accelerating networking and security functions
- > Delivering line-rate performance with turnkey accelerations including concurrent Open vSwitch (OVS), IPsec, and Firewall
- > Enabling flexibility to add custom plug-ins and workloads with application customization programmability

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U25N TURNKEY ACCELERATIONS

The U25N has three computational components, the X2 Ethernet Controller, the Arm cores represented by the PS block, and the FPGA programmable logic (PL).

Most of the basic NIC processing tasks of the U25N are handled within the X2, while the advanced functions are handled within the FPGA. Both blocks were designed to handle wire-rate traffic at 25Gbps/port. The X2 processes standard network tasks and Single Root Input Output Virtualization (SR-IOV) requests to set up physical functions (PFs) and virtual functions (VFs) and Receive Side Scaling (RSS).

By leveraging the programmability of the FPGA, the U25N can download bitstreams dynamically to support various features.

The FPGA is home to several data plane pipeline stages. These include the OVS Engine which handles network virtualization tasks like VXLAN, L2GRE, IPsec, and Firewall.

The Internet Protocol Security (IPsec) block on the FPGA offloads compute intense crypto operation, and it provides the open-source Internet Key Exchange (IKE) management solution - strongSwan. There is also a stateless firewall executing within the FPGA that can support rules passed down from the hosts' nftables entries.

The Arm cores of the U25N are primarily used for control plane management of the FPGAs programmable logic. Applications running on the Arm cores update tables used by the OVS, IPsec, and the firewall functions, while these programmable logic blocks are running. They also gather various statistics which are then used to improve the overall processing within the U25N SmartNIC platform.

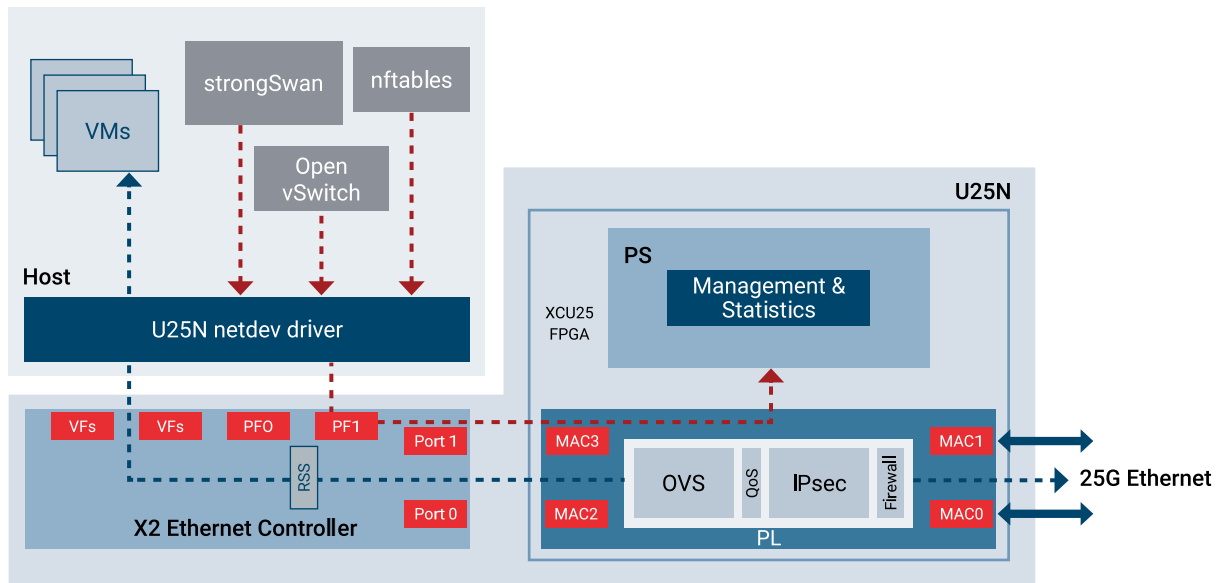


Figure 1: U25N Architectural Block Diagram

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OVS ACCELERATION

The U25N supports full data plane offload and acceleration of virtual switching from the host CPU onto the SmartNIC. This offload enables a high-performance data path that seamlessly integrates with the control plane. All the packet processing operations such as packet classification, match/action/modification processing, and tunneling encapsulation/decapsulation are handled completely on the SmartNIC.

Below is a comparison demonstrating the benefits of offloading OVS onto the SmartNIC vs. running OVS in software on the host CPU.

Figure 2 shows when OVS is run on the host CPU, the maximum throughput achievable was limited to <10Gbps. When OVS was offloaded to the SmartNIC with the same configuration, line-rate performance of 25Gbps was achieved.

Furthermore, by offloading OVS to the SmartNIC zero CPU resources are consumed for OVS data plane processing.

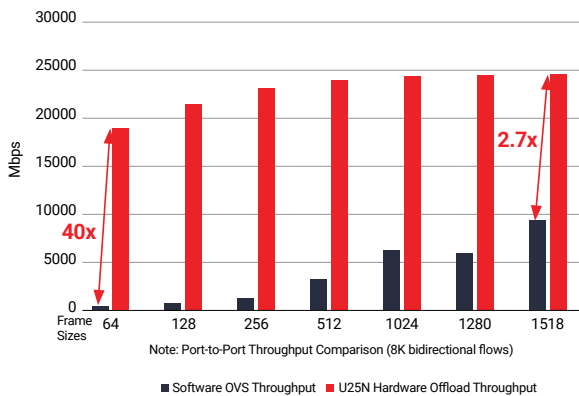


Figure 2: OVS on Host CPU vs. OVS offloaded on the U25N SmartNIC

OVS + IPSEC ACCELERATION

In addition to OVS acceleration, data centers and enterprises also want to enable the secure transmission and receipt of network traffic between two sites. The U25N supports the concurrent operation of offloaded OVS and offloaded IPsec traffic without sacrificing performance.

IPsec tunnels are created between two servers. When IPsec is in transport mode, L2GRE is used to create tunnels. The strongSwan application runs in the userspace. The strongSwan plugin is used to offload rules onto the U25N.

Below is a comparison demonstrating the benefits of running OVS+IPsec in software on the host CPU vs. offloading the same processing onto the SmartNIC.

As shown in Figure 3, when OVS + IPsec is running on the host CPU at large packet sizes, the maximum throughput achievable was limited to <4Gbps. When OVS + IPsec was offloaded to the U25N SmartNIC with the same configuration, full line rate is supported for mid and large packet sizes despite an extra tunneling header and IPsec header.

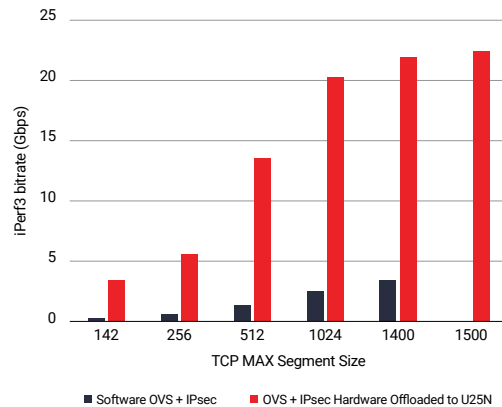


Figure 3: OVS + IPsec on Host CPU vs. OVS + IPsec offloaded on the U25N SmartNIC

IMPROVING INFRASTRUCTURE EFFICIENCY

The U25N SmartNIC enables improved CPU efficiency with hardware-based offload accelerating networking and security acceleration. This SmartNIC delivers line-rate performance with turnkey accelerations including concurrent Open vSwitch (OVS), IPsec, and Firewall.

TAKE THE NEXT STEP

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