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Revision History
The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
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</thead>
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<tr>
<td>11/07/12</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
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Chapter 1

VC7203 IBERT Getting Started Guide

Overview

This document provides a procedure for setting up the VC7203 Virtex®-7 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the ISE® Design Suite. The designs that are required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card that is provided with the VC7203 board. The demonstration shows the capabilities of the Virtex-7 XC7V485T FPGA GTX transceiver.

The VC7203 board is described in detail in UG957, VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide.

The IBERT demonstrations operate one GTX Quad at a time. The procedure consists of:

1. Setting Up the VC7203 Board, page 6
2. Extracting the Project Files, page 7
3. Connecting the GTX Transceivers and Reference Clocks, page 7
4. Configuring the FPGA, page 12
5. Setting Up the ChipScope Pro Software, page 13
6. Viewing GTX Transceiver Operation, page 17
7. Closing the IBERT Demonstration, page 18
Requirements

The hardware and software required to run the GTX IBERT demonstrations are:

- VC7203 Virtex-7 FPGA GTX transceiver characterization board including:
  - One SD card containing the IBERT demonstration designs
  - One Samtec BullsEye cable
  - Eight SMA female-to-female (F-F) adapters
  - Six 50Ω SMA terminators
  - GTX transceiver power supply module (installed on board)
  - SuperClock-2 module, Rev 1.0 (installed on board)
  - Active BGA HeatSink (installed on FPGA)
  - 12V DC power adapter
  - USB cable, standard-A plug to micro-B plug
- Host PC with:
  - SD card reader
  - USB ports
- Xilinx® ChipScope™ Pro software, version 14.3 or higher. Software is available at: [http://www.xilinx.com/chipscopepro](http://www.xilinx.com/chipscopepro)

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx ISE® Design Suite version 14.3 or higher
- PC with a version of the Windows operating system supported by Xilinx ISE Design Suite

Setting Up the VC7203 Board

This section describes how to set up the VC7203 board.

**Caution!** The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

When the VC7203 board ships from the factory, it is configured for the GTX IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default set-up before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in UG957, VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide.
2. Install the GTX transceiver power module by plugging it into connectors J66 and J97.
3. Install the SuperClock-2 module:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the VC7203 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the VC7203 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The ChipScope Pro Software .cpj project files for the IBERT demonstrations are located in vc7203_ibert.zip on the SD card labeled IBERT. They are also available online along with .bit files for all four designs (as collection rdf0271_14_3.zip) at:

www.xilinx.com/support/documentation/vc7203.htm

The zip collection contains seven ChipScope Pro project files: vc7203_q113.cpj, vc7203_q114.cpj, vc7203_q115.cpj, vc7203_q116.cpj, vc7203_q117.cpj, vc7203_q118.cpj and vc7203_q119.cpj. These files are used to load pre-saved MGT/IBERT and SuperClock-2 module control settings for the GTX demonstrations.

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card to the host computer.
2. Locate the file vc7203_cpj.zip on the Secure Digital memory card.
3. Unzip the files to a working directory on the host computer.

Running the GTX IBERT Demonstration

The GTX IBERT demonstration operates one GTX Quad at a time. This section describes how to test GTX Quad 115. The remaining GTX Quads are tested following a similar series of steps.

Connecting the GTX Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTX transceiver Quads Q113, Q114, Q115, Q116, Q117, Q118, and Q119 on the VC7203 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.
All GTX transceiver pins and reference clock pins are routed from the FPGA to a connector pad which interfaces with Samtec BullsEye connectors. Figure 1-2 A shows the connector pad. Figure 1-2 B shows the connector pinout.

**Note:** Q111 and Q112 do not connect to transceivers or reference clocks on the 485T FPGA. See [UG957](https://www.xilinx.com), *VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide* for details.
Running the GTX IBERT Demonstration

The SuperClock-2 module provides LVDS clock outputs for the GTX transceiver reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

**Note:** The image in Figure 1-3 is for reference only and might not reflect the current revision of the board.

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

**Note:** The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTX IBERT demonstration, the output clock frequencies are preset to 156.25 MHz. For more information regarding the SuperClock-2 module, refer to UG770, HW-CLK-101-SCLK2 SuperClock-2 Module User Guide.
Attach the GTX Quad Connector

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it isn’t already inserted (see Figure 1-4).

**Note:** Figure 1-4 is for reference only and might not reflect the current version of the connector.

Attach the Samtec BullsEye connector to GTX Quad 115 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.
Running the GTX IBERT Demonstration

GTX Transceiver Clock Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the CLK1 reference clock inputs. Connect these cables to the SuperClock-2 module as follows:

- CLK1_P coax cable → SMA connector J5 (CLKOUT1_P) on the SuperClock-2 module
- CLK1_N coax cable → SMA connector J6 (CLKOUT1_N) on the SuperClock-2 module

Note: Any one of the five differential outputs from the SuperClock-2 module can be used to source the GTX reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTX TX/RX Loopback Connections

Refer to Figure 1-2, page 9 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters (Figure 1-6), to connect the transmit and receive cables as shown in Figure 1-7 and detailed below:

- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N

Figure 1-6: SMA F-F Adapter

Figure 1-7: TX-To-RX Loopback Connection Example
Figure 1-8 shows the VC7203 board with the cable connections required for the Quad 115 GTX IBERT demonstration.

Configuring the FPGA

This section describes how to configure the FPGA using the SD card included with the board. The FPGA can also be configured through ChipScope Pro or iMPACT software using the .bit files which are available online (as collection rdf0271_14_3.zip) at:

http://www.xilinx.com/support/documentation/vc7203.htm

To configure from the SD card:

1. Insert the SD card provided with the VC7203 board into the SD card reader slot located on the bottom-side (upper-right corner) of the board.
2. Plug the 12V output from the power adapter into connector J2.
3. Connect the host computer to the VC7203 board using a standard-A plug to micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the micro-B plug connects to U8, the Digilent USB JTAG configuration port on the VC7203 board.
4. Select the GTX IBERT demonstration with the System ACE SD controller SYSACE-2 CFG switch, SW8. The setting on this 4-bit DIP switch (Figure 1-9) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTX IBERT demonstration, set ADR2 = ON, ADR1 = OFF, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.

![Configuration Address DIP Switch (SW8)](UG846_v1_09_102612)

**Figure 1-9: Configuration Address DIP Switch (SW8)**

There is one IBERT demonstration design for each GTX Quad on the VC7203 board, for a total of seven IBERT designs. An additional design is provided to demonstrate the USB/UART interface (details of this demonstration are described in the README file on the SD card). All eight designs are organized and stored on the SD card as shown in Table 1-1.

5. Place the main power switch SW1 to the ON position.

### Table 1-1: SD Card Contents and Configuration Addresses

<table>
<thead>
<tr>
<th>Demonstration Design</th>
<th>ADR2</th>
<th>ADR1</th>
<th>ADR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTX Quad 113</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 114</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>GTX Quad 115</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 116</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>GTX Quad 117</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 118</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>GTX Quad 119</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>USB/UART</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

### Setting Up the ChipScope Pro Software

1. Start the ChipScope Pro analyzer tools on the host computer and select **File > Open Project**.

2. When the Project window opens, navigate to the directory where the ChipScope software project files (.cpj) were extracted. Select vc7203_q115.cpj and click **Open**.

   **Note:** The .cpj file loads pre-saved project settings for the demonstration including MGT/IBERT and clock module control parameters. For more information regarding MGT/IBERT settings, refer to **UG029, ChipScope Pro Software and Cores User Guide**.
3. Click the Open Cable button (Figure 1-10).

![Figure 1-10: Open Cable Button](image)

4. When the dialog appears asking to set up the core with the settings from the current project, click Yes (Figure 1-11).

![Figure 1-11: IBERT V7GTX Project Settings](image)

Starting the SuperClock-2 Module

The IBERT demonstration designs use an integrated ChipScope Pro software VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: 1) An always-on Si570 crystal oscillator and, 2) an Si5368 jitter-attenuating clock multiplier. Outputs from either device can be used to drive the transceiver reference clocks. To start the SuperClock-2 module:
1. In the Project Panel, click **VIO Console** below **UNIT 1: SCLK2 Control (VIO)** (Figure 1-12).

![Project Panel - VIO Console (GTX)](image)

**Figure 1-12:** Project Panel - VIO Console (GTX)

2. The clock sources on the SuperClock-2 module are controlled from the VIO Console. Click on the **Si5368 Start** button (Figure 1-13) to enable the clock output.

**Note:** The ROM address values for the Si5368 and Si570 devices (i.e., Si5368 ROM Addr and Si570 ROM Addr) are preset to 60 to produce an output frequency of 156.250 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in **Table 1-2, page 18.**
3. In the project panel, click IBERT Console (Figure 1-14) to view GTX transceiver operation.
Running the GTX IBERT Demonstration

Viewing GTX Transceiver Operation

After completing step 3 in Starting the SuperClock-2 Module, the IBERT demonstration is configured and running. The status and test settings are displayed on the MGT/IBERT Settings tab in the IBERT Console shown in Figure 1-15.

Note the line rate, TX differential output swing, and RX bit error count:

- The line rate for all four GTX transceivers is 12.5 Gb/s (see MGT Link Status in Figure 1-15).
- The GTX transmitter differential output swing is preset to 850 mV.
- Verify that there are no bit errors.

![Figure 1-15: GTX IBERT Console](image-url)
Additional information on the ChipScope Pro software and IBERT core can be found in:

- UG029, ChipScope Pro Software and Cores User Guide
- DS855, ChipScope Pro Integrated Bit Error Ratio Test (IBERT) for Kintex-7 GTX (v2.01.a)

Closing the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the ChipScope application by selecting File > Exit.

   **Note:** Do not save changes to the project.

2. Place the main power switch SW1 in the off position.

SuperClock-2 Frequency Table

`Table 1-2` lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

<table>
<thead>
<tr>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100GE/40GE/10GE</td>
<td>161.130</td>
<td>10</td>
<td>CPRI</td>
<td>491.520</td>
<td>10</td>
<td>CPRI</td>
<td>644.000</td>
</tr>
<tr>
<td>1</td>
<td>Aurora</td>
<td>81.250</td>
<td>11</td>
<td>Display Port</td>
<td>67.500</td>
<td>11</td>
<td>Display Port</td>
<td>205.000</td>
</tr>
<tr>
<td>2</td>
<td>Aurora</td>
<td>162.500</td>
<td>12</td>
<td>Display Port</td>
<td>81.000</td>
<td>12</td>
<td>Display Port</td>
<td>210.000</td>
</tr>
<tr>
<td>3</td>
<td>Aurora</td>
<td>325.000</td>
<td>13</td>
<td>Display Port</td>
<td>135.000</td>
<td>13</td>
<td>Display Port</td>
<td>215.000</td>
</tr>
<tr>
<td>4</td>
<td>Aurora</td>
<td>650.000</td>
<td>14</td>
<td>Display Port</td>
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<td>14</td>
<td>Display Port</td>
<td>220.000</td>
</tr>
<tr>
<td>5</td>
<td>CE111</td>
<td>173.370</td>
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<td>Fibrechannel</td>
<td>106.250</td>
<td>15</td>
<td>Fibrechannel</td>
<td>225.000</td>
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<td>6</td>
<td>CPRI</td>
<td>61.440</td>
<td>16</td>
<td>Fibrechannel</td>
<td>212.500</td>
<td>16</td>
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<td>GigE</td>
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<td>18</td>
<td>GigE</td>
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<tr>
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<td>GigE</td>
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<tr>
<td>11</td>
<td>Display Port</td>
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<td>GigE</td>
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<td>Display Port</td>
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<td>GPON</td>
<td>187.500</td>
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<td>GPON</td>
<td>260.000</td>
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</table>
Creating the GTX IBERT Core

To rebuild the designs shown here, you must have an installation of ISE Design Suite version 14.3 or higher.

This section provides a procedure to create a single Quad GTX IBERT core using CORE Generator software. The procedure assumes Quad 113 and 12.5 Gb/s line rate, but cores for any of the GTX Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, refer to UG029, ChipScope Pro Software and Cores User Guide.

1. Start the CORE Generator tool from either the ISE Project Navigator window or a command line:
   - From the Project Navigator window, select: Tools > Core Generator…
   - From a command line, enter: coregen

2. In the Core Generator window, click the New Project icon (highlighted in Figure. Figure 1-16).

---

**Table 1-2: Si570 and Si5368 Frequency Table (Cont’d)**

<table>
<thead>
<tr>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
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<th>Frequency (MHz)</th>
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<td>SDI</td>
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<td>Generic</td>
<td>425.000</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
3. When the New Project dialog window opens (not shown), name the project and click **Save**.
4. In the Project Options window, click on Part and select the parameters listed here:
   - Family: Virtex-7
   - Device: xc7vx485t
   - Package: ffg1761
   - Speed Grade: -3
   Figure 1-17 shows the correct settings.

   ![Core Generator Project Options](image)

   **Figure 1-17:** CORE Generator Project Options (Part Options)

5. Click OK to close the Project Options window.
6. In the IP Catalog pane of the CORE Generator window (Figure 1-18) select:
   **Debug & Verification → Debug → IBERT 7 Series GTX (ChipScope Pro - IBERT) 2.02.a**

![Figure 1-18: Select IBERT Core](image)

7. Click on the **Customize and Generate** link under the **Actions** heading (Figure 1-18)
8. After a few seconds, page 1 of the IP customization window appears. For Component Name type `ibert_v7_q113` and under Board Configuration Settings select `vc7203 scm2` as shown in Figure 1-19, then click Next.

*Figure 1-19: CORE Generator - IBERT GTX Customization - Page 1*
9. Enter the information shown here and in Figure 1-20, then click **Next**:

- No. of Quads: **1**
- Select Quad: **QUAD 113**
- Max Rate (Gb/s): **12.5**
- Refclk (MHz): **156.25**
- GT count: **4**

*Figure 1-20: CORE Generator - IBERT GTX Customization - Page 2*
10. Enter the information shown here and in Figure 1-21, then click **Next**:

- MGT0_113: **CUSTOM1 / 12.5 Gbps**
- MGT1_113: **CUSTOM1 / 12.5 Gbps**
- MGT2_113: **CUSTOM1 / 12.5 Gbps**
- MGT3_113: **CUSTOM1 / 12.5 Gbps**

*Figure 1-21: CORE Generator - IBERT GTX Customization - Page 3*
11. Enter the information shown here and in Figure 1-22, then click **Next**:

- MGT0_113: MGTREFCLK1 113
- MGT1_113: MGTREFCLK1 113
- MGT2_113: MGTREFCLK1 113
- MGT3_113: MGTREFCLK1 113

![IBERT 7 Series GTX (ChipScope Pro - IBERT)](image)

*Figure 1-22: CORE Generator - IBERT GTX Customization - Page 5*
12. Verify the information shown in Figure 1-23, then click **Generate**.

13. The generation process takes a few minutes. When complete, a **Readme** window appears. The readme contains the location of the resultant `example_ibert_v7_q113.bit` file and provides a summary of the auto-generated example and implementation files.
Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:


For continual updates, add the Answer Record to your myAlerts:


For a glossary of technical terms used in Xilinx documentation, see:


Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the VC7203 kit and its documentation is available on the following websites.

The Virtex-7 FPGA VC7203 Characterization Kit Product Page:

www.xilinx.com/vc7203

The Virtex-7 FPGA VC7203 Characterization Kit Master Answer Record:

http://www.xilinx.com/support/answers/52383.htm

These Xilinx documents provide supplemental material useful with this guide:

UG957, VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide

UG770, HW-CLK-101-SCLK2 SuperClock-2 Module User Guide

UG029, ChipScope Pro Software and Cores User Guide

DS855, ChipScope Pro Integrated Bit Error Ratio Test (IBERT) for Kintex-7 GTX (v2.01.a)
Appendix B

Warranty

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