Virtex-6 FPGA -1L Speed Grade LX75T, LX130T, LX195T, LX240T, LX365T, LX550T, LX760, SX315T, and SX475T Production Errata

EN154 (v1.5) April 11, 2011 **Errata Notification**

Introduction

Thank you for designing with the Xilinx Virtex®-6 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices listed in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	XC6VLX75T	JTAG ID (Revision Code): 4, 6
	XC6VLX130T	JTAG ID (Revision Code): 4, 6
	XC6VLX195T	JTAG ID (Revision Code): 4, 6
	XC6VLX240T	JTAG ID (Revision Code): 4, 6
	XC6VLX365T	JTAG ID (Revision Code): 0, 2
	XC6VLX550T	JTAG ID (Revision Code): 0, 2
	XC6VLX760	JTAG ID (Revision Code): 4, 6
	XC6VSX315T	JTAG ID (Revision Code): 4, 6
	XC6VSX475T	JTAG ID (Revision Code): 4, 6
Packages	All	
Speed Grades	-1L	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

MMCM

Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED

When the Phase Frequency Detector (PFD) frequency (FIN/D) is lower than 135 MHz and the BANDWIDTH attribute of the MMCM is set to HIGH or OPTIMIZED, a phase error between MMCM output clocks can occur, making the output clock signals invalid. This condition can also cause the fractional output counter to fail.

The ISE® software v12.4 and later provides appropriate warnings for possible violations of this restriction.

The ISE software v12.4 and later correctly handles designs set to OPTIMIZED bandwidth for all valid PFD frequencies.

This issue will not be fixed in the devices listed in Table 1.

Work-around

PFD frequencies lower than 135 MHz must use LOW bandwidth mode to ensure correct operation. See Answer Record 38132 for more information.

Restriction of Clock Divider Values

The input clock divider (DIVCLK_DIVIDE) cannot have a value of 3 or 4 when the input clock frequency (F_{IN}) of the MMCM is above 315 MHz.

The ISE software v12.4 and later provides appropriate warnings for possible violations of this restriction.

This issue will not be fixed in the devices listed in Table 1.

Work-around

In all designs in which F_{IN} is above 315 MHz and DIVCLK_DIVIDE is set to 3 or 4, double the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values. See Answer Record 38133 for more information.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) Read_First mode, Simple Dual Port (SDP) mode, or ECC mode with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.3.1 (or later) of UG363, *Virtex-6 FPGA Memory Resources User Guide*.

This description was originally added in UG363 (v1.1), published 9/16/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. The ISE v12.1 software and later provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

The recommended work-around is to configure the block RAM in WRITE_FIRST mode. WRITE_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.2 and later. See Answer Record 34859.

Synchronous Built-in FIFO

When using the Built-In FIFO as a Synchronous FIFO (EN_SYN=TRUE) with asynchronous reset, correct behavior of the FIFO flags cannot be guaranteed after the first write.

All configurations other than EN_SYN=TRUE are not affected by this issue.

Work-arounds

To work around this issue, synchronize the negative edge of reset to RDCLK/WRCLK.

For more information and additional work-arounds see Answer Record 41099.

Configuration

PROGRAM_B Pin Behavior During Power-On

Holding the PROGRAM_B input statically Low prior to the completion of the power-on reset does not hold the FPGA in configuration reset. Instead, the FPGA proceeds with its standard power-on configuration sequence.

This issue will not be fixed in the devices listed in Table 1.

Work-around

For systems that need to delay the FPGA configuration sequence at power-on, hold the INIT_B pin Low.

See Answer Record 38134 for more information.

Configuration Switching Characteristics

The configuration switching characteristics for the devices listed in Table 1 deviate from the specifications listed in DS152: *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*. Table 2 contains the new specifications.

Table 2: **Configuration Switching Characteristics**

Symbol	Description	New Specifications	Units
T_{POR}	Power-on-reset	60	ms, Maximum
F_{MCCK}	Master CCLK frequency, serial mode	70	MHz, Maximum
$F_{MCCKTOL}$	Master CCLK tolerance from nominal	60	%, Maximum
$T_{SMCSCCK}$	CSI_B setup	5.5	ns, Minimum
T_{SMWCCK}	RDWR_B setup	16.0	ns, Minimum
F_{RBCCK}	Readback CCLK frequency	60	MHz, Maximum
F_{TCK}/F_{TCKB}	TCK frequency for configuration/boundary scan	33	MHz, Maximum
T_{MCCKL}/T_{MCCKH}	Master CCLK low/high duty cycle	40/60	%, Minimum/Maximum

Input Logic Resets Using GSR

When coming out of configuration after power-up or after asserting the PROGRAM_B_0 pin, the ILOGIC input registers (IFF, IDDR, and ISERDES) are not guaranteed to be initialized to zero. The same holds true if the GSR input of the STARTUP_VIRTEX6 block is used to reset the ILOGIC input registers. Initializing the registers to a one (using the "INIT=1" attribute) works as expected.

Work-around

If the user application requires the input registers to be initialized to zero, then a separate reset using general interconnect must be implemented.

GTX Transceivers - *Does Not Apply to the LX760 Device*

GTX Transceiver Initialization for Proper TXOUTCLK Functionality

TXOUTCLK can operate at an incorrect frequency or can remain in a static state when the TXPLL_DIVSEL_OUT attribute is set to 2 or 4 and the TXOUTCLK_CTRL attribute is set to "TXOUTCLKPCS", "TXOUTCLKPMA_DIV1", or "TXOUTCLKPMA_DIV2".

An updated reset sequence that ensures proper functionality is documented in version 2.4 of UG366, Virtex-6 *FPGA GTX Transceiver User Guide*. Also see Answer Record 35681 for more information.

RXRECCLK Static Operating Behavior

The RXRECCLK output port might operate at reduced frequency in buffer bypass mode if conditions (1) and (2) persist for more than 15,000 cumulative hours at 65°C Tj, 2,500 cumulative hours at 85°C Tj, or 800 cumulative hours at 100°C Tj:

1. Power has been applied to V_{CCINT}.
2. The device is in one of the following states:
   a. The FPGA is not configured
   b. The FPGA is configured, but the transceiver is uninstantiated
   c. The transceiver is instantiated, but no reference clock is toggling
   d. The transceiver is instantiated, but is held in reset or power-down

Work-around

Transceivers Uninstantiated in User Design but are Planned to be Used in the Future

For transceivers that are not instantiated in the user design but are planned to be used in the future, power must be applied to MGTAVCC, and the user design must be implemented using ISE v12.1 (or later) software for automatic insertion of the work-around circuit.

Transceivers Uninstantiated in User Design but are Not Planned to be Used in the Future

Automatic insertion of the work-around circuit can be disabled for uninstantiated transceivers that will not be used.

Transceivers Instantiated in User Design

Transceivers instantiated in user design do not require a work-around circuit if the reference clock is toggling and the transceiver is not held in reset or power-down.

See Answer Record 35055 for more information.

GTX Transceiver Delay Aligner

The GTX Transceiver Delay Aligner circuit is used when the TX Buffer and/or RX Elastic Buffer are bypassed.

The Transmitter Delay Aligner is no longer supported; additionally, the use model of the Receiver Delay Aligner must be changed.

Applications that use the TX Buffer and RX Elastic Buffer are not affected by this errata item.

Applications currently bypassing the TX Buffer and/or RX Elastic Buffer, including XAUI, RXAUI, CPRI, OBSAI, and PLBv46 RC/EP Bridge for PCI Express® IP cores and the Integrated Block for PCIe, must implement the following work-around.

Work-around

The TX Buffer and RX Elastic Buffer can still be bypassed using work-arounds described in Answer Record 39430 to maximize system margin.

System Monitor

System Monitor Maximum DCLK Frequency

The System Monitor intermittently generates an incorrect analog-to-digital conversion when the clock (DCLK) frequency is greater than 80 MHz. The maximum frequency specification for DCLK is being revised down from 250 MHz to 80 MHz. All designs should be updated to use 80 MHz max.

This issue will not be fixed in the devices listed in Table 1.

System Monitor Internal Reference Voltage

The System Monitor Internal Reference Voltage is not supported in the devices listed in Table 1. The External Reference Voltage must be used. See the System Monitor Dedicated Pins figure in UG370, *Virtex-6 FPGA System Monitor User Guide*.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installations.

- Refer to the Virtex-6 Device Production Software and Speed Specification Release table in DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics* for the Xilinx ISE Design Suite version required for the selected part.
- See Known Issues in Answer Record 32929.

Traceability

The XC6VLX240T is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

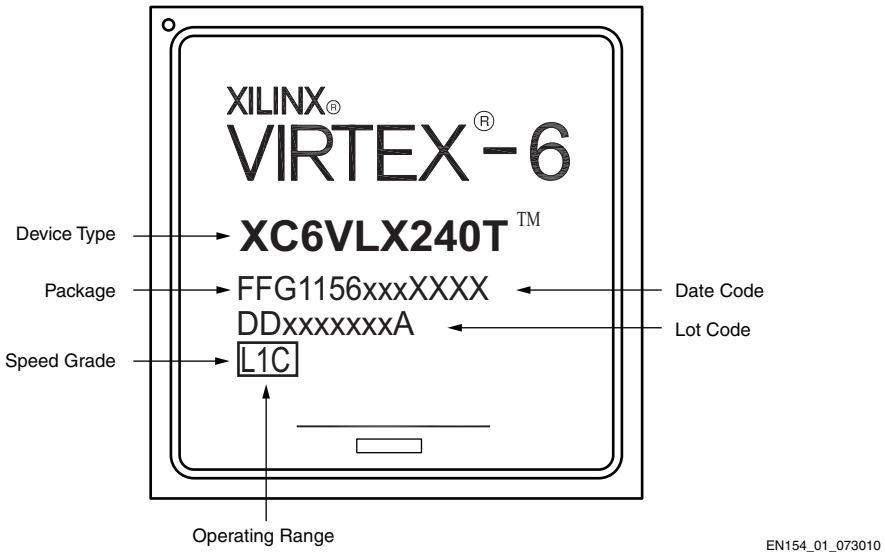

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
07/30/10	1.0	Initial Xilinx release.
09/21/10	1.1	Added the LX75T device to the document, which includes an update to Table 1. Added System Monitor Maximum DCLK Frequency. Updated System Monitor Internal Reference Voltage.
11/16/10	1.2	Updated JTAG ID Revision Codes in Table 1. Added Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED, Restriction of Clock Divider Values, PROGRAM_B Pin Behavior During Power-On, Configuration Switching Characteristics, and GTX Transceiver Initialization for Proper TXOUTCLK Functionality.
12/23/10	1.3	Added the following devices to the document, including an update to Table 1: LX365T, LX550T, LX760, SX315T, and SX475T.
01/17/11	1.4	Updated TXOUTCLK and RXRECCLK Static Operating Behavior; no longer applicable to TXOUTCLK. Added GTX Transceiver Delay Aligner per Xilinx Customer Notice XCN11009.
04/11/11	1.5	Added Synchronous Built-in FIFO and Input Logic Resets Using GSR.

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