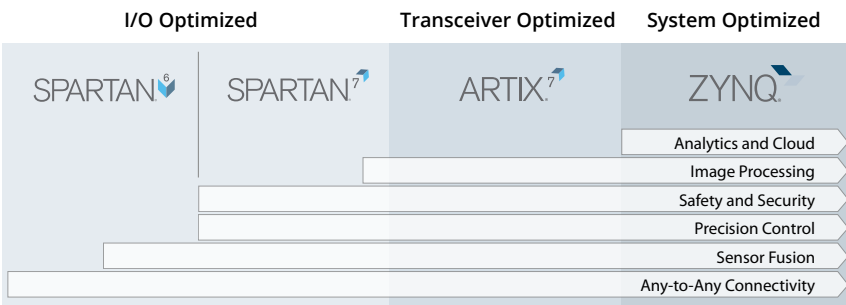


# Cost-Optimized Portfolio

## XILINX DELIVERS A COMPREHENSIVE ALL PROGRAMMABLE COST-OPTIMIZED PORTFOLIO

The Xilinx All Programmable Cost-Optimized Portfolio is comprised of four families: Spartan®-6 FPGAs for I/O optimization, Spartan-7® FPGAs for I/O optimization with the highest performance-per-watt, Artix-7 FPGAs for transceiver optimization and highest DSP bandwidth, and Zynq®-7000 All Programmable SoCs (Artix-7 Based Fabric) for system optimization with scalable processor integration.



Xilinx All Programmable Cost-Optimized Portfolio

## ENABLING CRITICAL FUNCTIONALITY ACROSS A WIDE RANGE OF APPLICATIONS

### Any-to-Any Connectivity

Flexible I/O densities and standards support to connect any media to any machine over any network

### Sensor Fusion

Scalable integration of any digital or analog sensor for data acquisition, aggregation, and pre-processing

### Safety & Security

Multi-level safety & security features ranging from isolation design flow to processor-driven secure boot

### Precision Control

Hardware acceleration and massive parallelism for real-time, highly synchronized connected control

### Image Processing

Highest DSP-to-logic mix for video and image quality enhancements and waveform processing

### Analytics and Cloud Connectivity

ARM®-based processing and hardware offloading for secure, real-time edge-to-cloud intelligence

A PORTFOLIO OPTIMIZED FOR COST, BANDWIDTH, POWER, AND INTEGRATION

**Spartan-6 FPGA**

I/O Optimized for connectivity

I/O Optimized

- High I/O-to-logic & -package ratios
- 800Mb/s DDR3 interface
- 1,080Mb/s LVDS I/O

Power Reduction Techniques

- Suspend and low power modes
- User-based shutdown/wakeup
- Voltage scaling

Cost-Optimized

- Hardened DDR controller, PCIe®
- Wire-bond packaging
- Optimized for 2 PCB layers

**Spartan-7 FPGA**

I/O Optimized for Highest Performance/Watt Connectivity

I/O Optimized

- Up to 400 I/O at 100K logic cells
- 800Mb/s DDR3, 1.25Gbs LVDS
- The only 28nm 8x8mm packages

Highest Spartan Performance/Watt

- Half the power of Spartan-6
- Power binning, voltage scaling
- Best-in-Class QoR with Vivado® Design Tools

Cost-Optimized

- Lowest cost 7 series family
- Integrated analog mixed signal
- Optimized for 2 PCB layers

**Artix-7 FPGA**

Transceiver-Optimized for High Bandwidth Applications

Transceiver-Optimized

- High I/O-to-logic & -package ratios
- 800Mb/s DDR3 interface
- 1,080Mb/s LVDS I/O

Best Signal Processing Performance

- Highest DSP-to-logic ratios
- Best-in-class DSP FMAX at 628MHz
- Wide, efficient 25x18 multipliers

Cost-Optimized

- Integrated PCIe Gen2
- Integrated analog mixed signal
- Low-cost 10x10 packages

**Zynq-7000 All Programmable SoCs (Artix-7 FPGA-Based Fabric)**

System-Optimized for Scalable Processor Integration

System-Optimized

- Scalable, ARM-based platform
- Single or Dual ARM Cortex™-A9
- Scalable FPGA logic densities

Comprehensive Ecosystem

- Extensive OS support
- Familiar embedded tools
- Breadth of boards & kits

Cost-Optimized

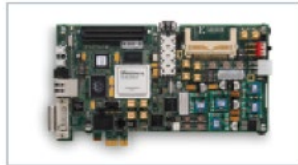
- Portfolio's highest integration
- Low-cost entry to ARM SoCs
- SW & HW field-upgradeable

Take the NEXT Step

See the full selection of boards and kits targeting cost-sensitive applications.



Avnet Spartan-6 Lx9 FPGA Microboard



Spartan-6 FPGA SP605 Evaluation Kit



Zynq-7000 All Programmable SoC Zedboard



Zynq-7000 All Programmable SoC ZC702 Evaluation Kit



Ted Spartan-6 FPGA Consumer Video Kit 2.0



Artix-7 35T Arty FPGA Evaluation Kit



Zynq-7000 All Programmable SoC Video and Imaging Kit



Zynq-7000 All Programmable SoC ZC702 Evaluation Kit



Microzed Evaluation Board



Avnet Artix-7 50T FPGA Evaluation Kit



Diligent Nexys™4 Artix-7 FPGA Board

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