OVERVIEW

Zynq® UltraScale+™ MPSoCs combine a high-performance Arm®-based multicore, multiprocessing system with ASIC-class programmable logic. These devices, equipped with dual- and quad-core application processors, deliver maximum scalability and are capable of offloading critical applications, such as graphics and video pipelining, to dedicated processing blocks, along with a full complement of integrated peripherals and connectivity cores suitable for next-generation systems.

Fully integrated programmable logic enables custom co-processors and custom memory hierarchies to meet application specific needs, including deep learning processing units (DPU) for AI/ML processing. The 16nm FinFET+ programmable logic communicates with the processing system through 6,000 interconnects, enabling bandwidth that is not possible with multichip solutions. Dramatic power savings are achieved through fine-grained control of power domains and gated power islands. With specialized processing elements for different workloads, Zynq UltraScale+ MPSoCs are optimal single-chip platforms for both cost-sensitive and high-performance applications.

HIGHLIGHTS

New ZU1 Device: Lowest-Cost, Lowest Power Entry Point
- Same Arm Multiprocessing subsystem for portfolio scalability
- 40% less static power than ZU2 device, with only 20% less programmable logic
- Highest I/O-to-System Logic Cell ratio to maximize connectivity
- Highest DSP-to-System Logic Cell ratio for maximum compute and AI offloading

Packaging Innovation for Industry’s Highest Compute Density
- Integrated Fan-Out (InFO) packaging for ultra-compact form factor (9.5x15mm)
- 60% less area (than flip-chip packaging) for better thermal & power distribution
- 5X compute density vs comparable ASSPs (DMIPS/mm²)
- Available for ZU1, ZU2, and ZU3 devices

Architectural Advantages vs. ASSPs
- Custom memory hierarchy for highest throughput, lowest latency designs
- Tightly coupled memory enables full isolation of safety critical functions
- Soft co-processors for offloading or extra processing capability
- AI/ML processing capable with custom deep learning processing units (DPU)
- Scalable with the full Zynq MPSoC portfolio – preserve your design investment
### FEATURES

#### PROCESSING SYSTEM

<table>
<thead>
<tr>
<th></th>
<th>CG Devices</th>
<th>EG Devices</th>
<th>EV Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Processing Unit</td>
<td>Dual-core Arm® Cortex®-A53</td>
<td>Quad-core Arm Cortex-A53</td>
<td>Quad-core Arm Cortex-A53</td>
</tr>
<tr>
<td>Real-Time Processing Unit</td>
<td>Dual-core Arm Cortex-R5F</td>
<td>Dual-core Arm Cortex-R5F</td>
<td>Dual-core Arm Cortex-R5F</td>
</tr>
<tr>
<td>Graphics Processing Unit</td>
<td>–</td>
<td>Arm Mali™-400 MP2</td>
<td>Arm Mali-400 MP2</td>
</tr>
<tr>
<td>Video Codec Unit</td>
<td>–</td>
<td>–</td>
<td>Up to 8K @ 15fps Supports H.264/H.265</td>
</tr>
<tr>
<td>Embedded and External Memory</td>
<td>256KB On-Chip Memory w/ECC; External DDR4/3/3L; LPDDR4/3; External Quad-SPI; NAND; eMMC</td>
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#### PROGRAMMABLE LOGIC*

<table>
<thead>
<tr>
<th></th>
<th>CG Devices</th>
<th>EG Devices</th>
<th>EV Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Logic Cells (K)</td>
<td>600</td>
<td>1,143</td>
<td>504</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>2,520</td>
<td>3,528</td>
<td>1,728</td>
</tr>
<tr>
<td>Transceivers</td>
<td>24 @ 16Gb/s</td>
<td>44 @ 16Gb/s</td>
<td>24 @ 16Gb/s</td>
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<tr>
<td>On-Chip Memory (Mb)</td>
<td>44.2</td>
<td>80.4</td>
<td>44.2</td>
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<tr>
<td>PCIe® Gen3 x16</td>
<td>2</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>100G Ethernet Blocks with RS-FEC</td>
<td>–</td>
<td>4</td>
<td>–</td>
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<tr>
<td>150G Interlaken</td>
<td>–</td>
<td>4</td>
<td>–</td>
</tr>
</tbody>
</table>

#### FEATURES OVERVIEW

- **Dynamic Power Management**
  - Multiple power domains with granular gating control
  - Platform Management Unit for power, safety, and reliability

- **Safety and Security**
  - Configuration Security Unit for anti-tamper and lockdown
  - Support for 4096-bit RSA keys with SHA-3 hash functions
  - Secure system boot with AES 256 decryption
  - Full Arm TrustZone support

- **Custom Memory Hierarchy**
  - Up to 10MB of internal local memory for co-processors and custom accelerators
  - Multiple DDR controller capable for lowest latency memory access
  - Tightly coupled memory enables isolated design flows for safety-critical applications

- **Deep Learning Processing Unit (DPU) Compatible**
  - Configurable computation engine dedicated to convolutional neural networks
  - Accelerate AI/ML functions easily with reference designs and pre-built AI models

*Maximum for each device family

### TAKE THE NEXT STEP

Zynq UltraScale+ MPSoCs are supported by comprehensive development tools, reference designs, an IP catalog, and evaluation platforms. For more information about Xilinx Zynq UltraScale+ MPSoCs, visit [https://www.xilinx.com/zynq-ultrascale-plus.html](https://www.xilinx.com/zynq-ultrascale-plus.html). Evaluation kits sold separately; see the Zynq UltraScale+ MPSOC Kit Selection Guide for details and place an order today.