

### Course Description

Learn how to construct, implement, and download a Dynamic Function eXchange (DFX) FPGA design using the Vivado® Design Suite. This course covers both the tool flow and mechanics of successfully creating a DFX design.

The emphasis of this course is on:

- Identifying best design practices and understanding the subtleties of the DFX design flow
- Using the DFX Controller and DFX Decoupler IP in the DFX process
- Implementing DFX in an embedded system environment
- Applying appropriate debugging techniques on DFX designs
- Employing best practice coding styles for a DFX system

#### Level – FPGA 4

#### Course Details

- 2 days ILT
- 17 lectures
- 8 labs
- 2 demos

#### Course Part Number – FPGA-DFX

**Who Should Attend?** – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need to understand Dynamic Function eXchange techniques

#### Prerequisites

- *Designing FPGAs with the Vivado Design Suite 2* course
- *Designing FPGAs with the Vivado Design Suite 3* course
- *Designing FPGAs with the Vivado Design Suite 4* course
- Working HDL knowledge (VHDL or Verilog)

#### Software Tools

- Vivado Design Suite 2020.2
- Vitis™ unified software platform 2020.2

#### Hardware

- Demo board: Zynq® UltraScale+™ MPSoC ZCU104 board\*

\* Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe what Dynamic Function eXchange is
- Define DFX regions and Reconfigurable Modules with the Vivado® Design Suite
- Generate the appropriate full and partial bitstreams for a DFX design
- Implement a nested DFX design
- Use the ICAP and PCAP components to deliver the partially reconfigurable systems
- Implement a DFX system using the DFX Controller IP
- Identify how Dynamic Function eXchange affects various silicon resources, including block RAM, IOBs, fabric, and MGTs

- Implement a Dynamic Function eXchange system using the following techniques
  - Direct JTAG connection, floorplanning, and timing constraints and analysis
- Debug a DFX designs using the Vivado Design Suite
- Implement a DFX system in an embedded environment using the Vitis IDE

### Course Outline

#### Day 1

##### Basics of DFX

##### Introduction to Dynamic Function eXchange (DFX)

Explains what Dynamic Function eXchange is and defines the terminologies used in DFX. Also provides an overview of the configuration and reconfiguration processes. {Lecture, Demo}

##### DFX Tool Flow

##### DFX Flow Using the Vivado Design Suite GUI

Illustrates the steps for creating a DFX project in the Vivado Design Suite and describes various supported and unsupported features. {Lecture, Lab}

##### DFX Flow Using Vivado Design Suite Tcl Commands

Reviews the flow using non-project-based commands, including using implementation constraints and specific characteristics. {Lecture, Lab}

##### Nested DFX

Describes using nested DFX, the process by which a Reconfigurable Partition (RP) can be segmented into smaller regions, each of which is partially reconfigurable. {Lecture, Lab}

##### Abstract Shell for Dynamic Function eXchange

Describes how compilation time can be reduced by using an Abstract shell (UltraScale+ devices only). {Lecture}

##### DFX Design Considerations for Xilinx Devices

##### DFX Design Considerations for All Xilinx Devices

Covers the requirements, characteristics, and limitations associated with DFX designs that can simplify the debug process and reduce the risk of design malfunctions. {Lecture}

##### DFX Design Considerations for 7 Series, Zynq SoC, UltraScale, and UltraScale+ Devices

Discusses DFX design consideration methodologies for various Xilinx device families. {Lecture}

##### DFX Design-Specific IP Blocks

##### DFX Intellectual Property (IP)

Reviews the various IPs that are specifically for use with DFX designs. {Lecture, Lab, Demo}

#### Day 2

##### DFX Configuration

##### Configuring Devices Using DFX

Reviews the basics of configuration and various configuration modes. {Lecture}

##### Configuration Parameters

Covers various configuration parameters, including factors that affect configuration time and configuration debugging. {Lecture}

##### DFX Bitstreams

Describes the different types of bitstreams for DFX compilation, including full, partial, blanking, and clearing. {Lecture}

- **DFX Bitstream Integrity**

Describes partial bit file integrity and implementing DFX through the ICAP for FPGA devices. {Lecture}

**DFX Design Analysis and Debugging**

- **Floorplanning a DFX Design**

Demonstrates how to create Pblocks for various devices and how to create a floorplan for a reconfigurable region. {Lecture, Lab}

- **DFX Timing Analysis and Constraints**

Illustrates how and when to apply different constraint files, the process of performing a DFX timing-level simulation, and the process of performing static timing analysis on a DFX design. {Lecture, Lab}

- **DFX Debugging**

Illustrates DFX debugging techniques using Vivado Design Suite debug cores. {Lecture, Lab}

**DFX Designs in Embedded Systems**

- **DFX in Embedded Systems**

Describes the embedded design flow in the Vivado Design Suite, the advantages of using a processor with DFX, and how to connect a processor to the PCAP to control DFX using the Vitis IDE. {Lecture, Lab}

- **DFX Designs Using the PCIe Core**

Reviews the advantages of using a PCIe core in a DFX design. {Lecture}

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