8051 High-speed 8-bit RISC Microcontroller (R8051XC)

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AllianceCORE™ Facts

Provided with Core	
Documentation	Core Specifications, Instruction set details, test set details
Design File Formats	EDIF or NGC netlist , Source RTL available at extra cost
Constraints Files	r8051xc.ucf
Verification	Test bench, test vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	Example Design Assembler programs
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
ModelSim & NC-Sim	
Support	
Support provided by CAST, Inc.	

Features

- Available under terms of the SignOnce IP License
- Eight-bit instruction decoder for MCS® 51 instruction set
- Executes instructions with one clock per cycle (versus twelve for standard 80C51) for an average 8.1 times speed increase
- ALU performs 8-bit arithmetic and logical operations and Boolean manipulations; additional 8-bit multiplication and division are optional
- Flexible external memory interface can address up to 8 MB of Program Memory and 8 MB of Data Memory Space (when using memory banking)
- SFR interface services 40 to 118 external Special Function Registers (depending on peripherals configuration)
- Extensive core configurability: choose options as needed, or get fully-configurable version

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax[1] (MHz)	Slices[2]	IOB[3]	GCLK	BRAM	MULT	DCM/ DLL	MGT	PPC	Design Tools
Spartan™-3E	XC3S500E-5	65	1829	67	2	3	N/A	0	N/A	N/A	ISE™ 9.2.01i
Virtex™-II Pro	XC2VP4-7	104	1766	67	2	3	0	0	0	0	ISE™ 9.2.01i
Virtex™-4	XC4VLX25-12	126	1872	67	2	3	0	0	0	0	ISE™ 9.2.01i
Virtex™-5	XC5VLX30-3	130	854	67	2	3	0	0	0	0	ISE™ 9.1.03i

Notes:

Results are for the R8051XC-A version without debugging. For other versions please consult CAST.

1) Optimized for speed with 256 Bytes of internal data memory and 4 KB of internal program memory

2) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

3) Additional I/Os required if memory is implemented off-chip

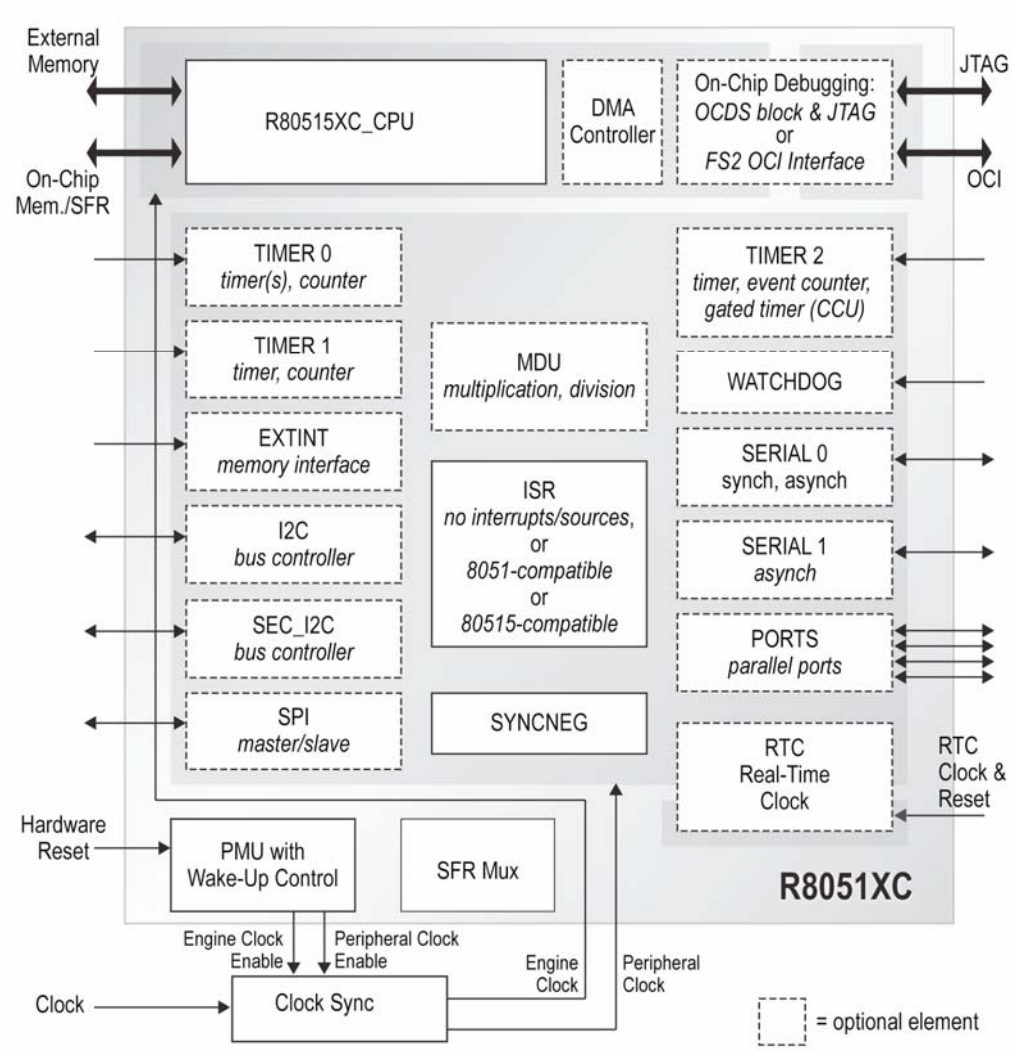

Figure 1: R8051XC Block Diagram

Features (continued)

Optional Functions and Peripherals

- Direct Memory Access (DMA) Controller
  - Up to eight independent channels
  - Read/Write Access to all memory spaces (incl. SFR)
  - Linear addressing (up to 8MB)
  - Address auto-increment/decrement
  - Synchronous/asynchronous Mode
  - Software Trigger/Hardware Trigger
- Register Control Unit
  - Interfaces for 128 B or 256 B internal Data Memory Space
  - Interface for extra on-chip SFRs
- Program memory write mode allows writes to external program memory space
- External Memory Interface

  - Addresses up to 8 MB of Program Memory and up to 8 MB of Data Memory (when using memory banking)
  - One, two, or eight Data Pointers for fast data block transfer
- Interrupt Controller: four priority levels with eighteen interrupt sources, or two priority levels with six source
- Power Management Unit with power-down modes (IDLE and STOP). Interface for on-chip debug: native On-Chip Debug Support (OCDS) or FS2 On-Chip Instrumentation (OCI)
- Multiplication-Division Unit
  - 16 x 16-bit multiplication
  - 32/16- and 16/16-bit division
  - 32-bit normalization and L/R shifting
- 16-bit Timer/Counters: 80C51-like Timers 0 and 1, or the 80C515-like Timer 2
- Timer 2 includes a Compare/Capture Unit with four 16-bit Compare registers for Pulse Width Modulation; four external Capture inputs for Pulse Width Measuring; and a 16-bit Reload register for Pulse Generation
- Input/Output ports
  - Up to four (configurable) 8-bit I/O ports
  - Alternate port functions, such as external interrupts and the serial interface are separated, providing extra port pins when compared with the standard 8051
- Serial 0: a full-duplex serial interface (80C51-like)
- Serial 1: an asynchronous-only version of Serial 0
- 15-bit programmable Watchdog timer
- I2C™ and one or two SPI interfaces

Applications

With numerous options for features and capabilities, designers can readily configure a version that best matches their particular needs, from fitting in the smallest device to controlling complex systems. Suitable application areas include: embedded microcontroller systems; communication systems; data computation and transfer functions; and professional audio and video products.

General Description

The R8051XC is a configurable, single-chip, 8-bit microcontroller core that can implement a variety of fast processor variations executing the MCS® 51 instruction set.

The efficient core design runs an average of 8.1 times faster than the 80C51. A rich set of optional features and peripherals enable designers to closely match the core with their specific application and hardware requirements (FPGA, ASIC, or structured ASIC). These options include hardware interrupts, interfaces for serial communication, I2C and SPI interfaces, a timer system, I/O ports, a power management unit, a multiplication-division unit, a watchdog timer, DMA controller and a real-time clock. Integrated on-chip debugging using either the native OCDS or FS2's OCI is also available.

The R8051XC is an extension of our proven 8051 family of processor cores, which have been successfully implemented in a hundred different customer products. Designers can purchase a custom configuration by selecting a set of options that best meets their needs, or choose from these three prepackaged versions of the core:

R8051XC-F is the fully-configurable version of the core, with all options included.

R8051XC-A matches our earlier R8051, with a set of peripherals making it compatible with the Intel 80C31 (see details in the Configurations section).

R80515XC-B matches our earlier R80515 core, with a set of peripherals making it compatible with the Siemens 80C515 and 80C517.

Developed for easy reuse in ASIC and FPGA implementations, the core is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset.

Functional Description

The R8051XC core is partitioned into modules as shown in figure 1 and described below. A netlist is provided for the core.

Control Processor Unit (CPU)

The CPU fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations, and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64KB to 8MB of Program and Data Memory.

DMA Controller

The Direct Memory Access (DMA) Controller contains up to eight individual channels, each capable of transferring data from or to any addressable location (program memory, internal or external data memory, or SFR). Each channel can work in synchronous mode (when just one byte is transferred at each trigger) or asynchronous mode (when all the data is transferred at once). Transfers can be triggered by software or by a specified interrupt source.

External Memory Interface

The flexible external memory interface can address up to 8 MB of Program Memory and 8 MB of Data Memory Space. It uses a HOLD interface to support any external DMA controller, and it eases the connection to memories using a de-multiplexed address/data bus. The EMI uses variable-length code fetch and MOVC to access fast or slow program memory, and similarly uses a variable-length MOVX to access fast or slow RAM or peripherals.

Ports

The parallel I/O port controller serves up to four parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic Intel™ 80C51, but lacks the multiplexed memory feature and alternate functions. (These could be combined off-core if required).

Serial 0 and 1

The core includes two independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial 0 is capable of both synchronous and asynchronous transmission, while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode, full-duplex operation is available. Received data is buffered in a holding register, which allows the serial ports to receive an incoming word before the software has read the previous value.

Serial 0 offers the following communication protocols:

- Synchronous mode, fixed baud rate

- 8- and 9-bit UART modes, variable baud rate
- 9-bit UART mode, fixed baud rate

Serial 1 has two operating modes:

- 8- and 9-bit UART mode, variable baud rate

Both include an additional Baud Rate Generator.

Timers 0 and 1

Timers 0 and 1 are nearly identical, and they each have these three modes: 13-bit timer/counter, 16-bit timer/counter, and 8-bit timer/counter with auto reload. Timer 0 has an additional mode: two 8-bit timers. Each timer can also count external pulses (1 to 0 transition) on the corresponding `t0` or `t1` pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

Timer 2

Operates as a timer, event counter, or compare/capture unit.

In timer mode, Timer 2 can be incremented every machine cycle or every second machine cycle, depending on the 2:1 prescaler. In event counter mode, Timer 2 is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, Timer 2's incrementing is gated by an external signal.

A Timer 2 reload can be executed in two modes. In Mode 0, the reload signal is generated by a Timer 2 overflow (auto reload), while in Mode 1 it is generated by a negative transition at the corresponding input pin t2ex.

Multiplication Division Unit

This on-chip arithmetic unit performs these unsigned integer operations:

- 16 x 16-bit multiplication
- 32/16-bit division and 16/16-bit division
- 32-bit normalization and L/R shifting

The MDU allows operations to occur concurrently to and independent of the engine activity.

Power Management Unit (PMU) & Reset Control

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates an internal synchronous reset signal (upon external reset or watchdog timer overflow).

IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

Wake-up Control

The Wake-up From Power-Down Mode Control Unit services two external interrupts during power-down modes.

Real-Time Clock

The RTC generates a real-time count with a resolution of 1/256th second and range of 179 years. It can set and read seconds, minutes, hours, day of the week, and the date, represented by a 16-bit number interpreted by software. An alarm function can generate interrupts periodically or at a specific time, and these may be used to wake up from IDLE/STOP mode.

SFR Mux

The SFR Multiplexer provides a common bus multiplexer for all the internal and external Special Function Registers.

On-Chip Debugging

Serves as the interface for On-Chip Debug Support using an IEEE1149.1 (JTAG) port. Implements either native On-Chip Debug Support (OCDS) or FS2's On-Chip Instrumentation (OCI). See their respective datasheets for details.

Watchdog Timer

A 15-bit counter that is incremented every 24 or 384 clock cycles. After an external reset, it is disabled and all registers are set to zeros. It can be started by applying an active input during reset (hardware automatic start) or by setting the enable bit by software. Once started, it cannot be stopped unless the internal reset signal becomes active. This occurs when the Watchdog enters the state 7CFFh, and it can be avoided by refreshing the Watchdog with software before it reaches 7CFFh.

Interrupt Service Routine Unit

The R8051XC provides two types of interrupt controllers: an 8051-compatible with up to six interrupt sources and two priority levels, or an 80515-compatible with up to eighteen interrupt sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

Primary and Secondary I2C™ Interfaces

The primary (I2C) and secondary (SEC_I2C) I2C Bus Controllers each provide a serial interface that meets the Philips I2C bus specification and supports all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. They perform 8-bit oriented, bi-directional data transfers up to 100 kbit/s in the standard mode, or up to 400 kbit/s in the fast mode.

Core Modifications

The R8051XC is a configurable core. A spreadsheet-like Design Configurator is available to help in the selection of the core's many options. The configurable options include:

- Size of external data/program memory: 64 KB to 8 MB
- Number of DPTR registers: 1, 2 or 8
- Two types of interrupt controller: Type 51 or Type 515
  - Interrupt sources: 0 to 6 0 to 18
  - External interrupts: 0 to 2 0 to 13
  - Priority levels: 2 or 4
- Number of 8-bit I/O ports: 0 to 4
- Number of 16-bit timers: 0 to 3
- Number or serial ports: 0, 1, or 2
- Watchdog timer: yes or no

- Multiplication-Division unit: yes or no
- DMA Channels: 0 to 8
- I2C master-slave interface: 0, 1, or 2
- SPI master-slave interface: yes or no
- On-chip debug support: OCDS, FS2 OCI, or none
- For OCDS:
  - Number of hardware breakpoints: 2 to 8
  - Program trace: yes or no
  - Data trace: yes or no
- Rarely used instructions MUL, DIV, DA: yes or no
- Software Reset: yes or no
- Support for external DMA operations: yes or no
- Real Time Clock: yes or no

The 8051-like prepackaged R8051XC-A core includes: two timers, one serial port, four parallel I/O Ports, and a two-level interrupt controller.

The 80515-like prepackaged R8051XC-B core includes: three timers, two serial ports, four parallel I/O ports, a watchdog timer, a multiplication-division unit, and two DPTR registers.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
clkcpu	Input	**Engine Clock**. Pulse for internal circuits, which are stopped when R8051XC is in IDLE or STOP mode.
clkcpuen	Output	**Engine clock enable output**. External control for the “clkcpu” clock, when set to 1 the system clock should be applied to the “clkcpu” input, otherwise the “clkcpu” should be stopped.
clkper	Input	**Peripheral clock**. Pulse for internal circuits, which are stopped when R8051XC is in STOP mode.
clkperen	Output	**Peripheral clock enable output**. External control for the “clkper” clock, when set to 1 the system clock should be applied to the “clkper” input, otherwise the “clkper” should be stopped.
reset	Input	Hardware reset input
ro	Output	Reset output
rtxc	Input	RTC 32,768kHz clock input (optional)
rtcreset	Input	RTC Reset input (optional)
swd	Input	Start Watchdog Timer
port0i	Input	Port 0 input
port0o	Output	Port 0 output
port1i	Input	Port 1 input
port1o	Output	Port1 output
port2i	Input	Port 2 input
port2o	Output	Port 2 output
port3i	Input	Port 3 input

Signal	Signal Direction	Description
port3o	Output	Port3 output
External interrupt inputs		
int0-int12	Input	External interrupts 0 through 6
Compare/Capture inputs		
cc0-cc3	Input	Compare/Capture 0-3 inputs
ccubus0-3	Output	Compare/Capture 0-3 outputs
Serial 0 interface		
rxd0i	Input	Serial 0 receive data
rxd0o	Output	Serial 0 transmit data
txd0	Output	Serial 0 transmit data or receive clock in mode 0
Serial 1 interface		
rxd1i	Input	Serial 1 receive data
rxd1o	Output	Serial 1 transmit data
Timer inputs		
t0	Input	Timer 0 external input
t1	Input	Timer 1 external input
t2	Input	Timer 2 external input
t2ex	Input	Timer 2 capture trigger
I2C Interface		
scli	Input	Serial clock input
sdai	Input	Serial data input
sclo	Output	Serial clock output
sdao	Output	Serial data output
Secondary I2C Interface		
scl2i	Input	Serial clock input
sda2i	Input	Serial data input
scl2o	Output	Serial clock output
sda2o	Output	Serial data output
SPI Interface		
scki	Input	Serial clock input
scko	Output	Serial clock output
scktri	Output	Serial clock tri-state enable (to combine the “sck” bidirectional port)
ssn	Input	Slave select input
misoi	Input	“Master input / slave output” input pin
misoo	Output	“Master input / slave output” output pin
misotri	Output	“Master input / slave output” tri-state enable (to combine the “miso” bidirectional port)
mosii	Input	“Master output / slave input” input pin
mosio	Output	“Master output / slave input” output pin
mositri	Output	“Master output / slave input” tri-state enable (to combine the “mosi” bidirectional port)
spssn0-8	Output	Slave select output register
External Memory interface		
mempsack	Input	Program memory read acknowledge
memack	Input	Data memory acknowledge

Signal	Signal Direction	Description
memdatai	Input	Memory data input
memdatao	Output	Memory data output
memaddr	Output	Memory address
mempswr	Output	Program store write enable
mempsrd	Output	Program store read enable
memwr	Output	Data Memory write enable
memrd	Output	Data Memory read enable
External Memory interface (for posedge-clocked memories)		
memdatao_comb	Output	Memory data output
memaddr_comb	Output	Memory address
mempswr_comb	Output	Program store write enable
mempsrd_comb	Output	Program store read enable
memwr_comb	Output	Data Memory write enable
Internal Data Memory interface		
ramdatai	Input	Data bus input
ramdatao	Output	Data bus output
ramaddr	Output	Data file address
ramwe	Output	Data file write enable
ramoe	Output	Data file output enable
Internal Data Memory interface (for posedge-clocked memories)		
ramdatao_comb	Output	Data bus output
ramaddr_comb	Output	Data file address
ramwe_comb	Output	Data file write enable
ramoe_comb	Output	Data file output enable
External SFR interface		
sfrdatai	Input	SFR data bus input
sfrdatao	Output	SFR data bus output
sfraddr	Output	SFR address
sfrwe	Output	SFR write enable
sfroe	Output	SFR output enable
sfrack	Input	SFR acknowledge
External SFR interface (for posedge-clocked memories)		
sfrdatao_comb	Output	SFR data bus output
sfraddr_comb	Output	SFR address
sfrwe_comb	Output	SFR write enable
sfroe_comb	Output	SFR output enable
sfrack_comb	Input	SFR acknowledge
On-Chip Instrumentation Interface (OCI)*		
debugreq	Input	Debug mode request
degubstep	Input	Debug mode single-step
debugprog	Input	Debugger program select
debugack	Output	Debugger acknowledge signal
flush	Output	Other instruction fetch
waitstaten	Output	Waitstate indicator. Active low when the CPU performs a wait cycle (internally or externally

Signal	Signal Direction	Description
		generated)
acc	Output	Accumulator register output
On-Chip Debug Interface (OCDS)*		
trst	Input	Debug logic reset input (IEEE1149.1 Test Logic Reset)
tck	Input	Debug clock (IEEE1149.1 Test Clock)
tms	Input	Test Mode Select (IEEE1149.1 Test Mode Select)
tdi	Input	Debug Data Input (IEEE1149.1 Test Data Input)
tdo	Output	Debug Data Output (IEEE1149.1 Test Data Output)
tdoenable	Output	Debug Data Output Enable
Trace RAM Interface (OCDS)*		
addr_buf0	Output	RAM0 address bus
datao_buf0	Output	RAM0 data output bus
datai_buf0	Input	RAM0 data input bus
wr_bug0	Output	RAM0 write enable signal
rd_buf0	Output	RAM0 read enable signal
addr_buf1	Output	RAM1 address bus
datao_buf1	Output	RAM1 data output bus
datai_buf1	Input	RAM1 data input bus
wr_buf1	Output	RAM1 write enable signal
rd_buf1	Output	RAM1 read enable signal
Hold Interface		
hold	Input	Hold mode request
holda	Output	Hold mode acknowledge signal
intoccur	Output	Interrupt occurred in Hold mode signal

* OCI and OCDS are mutually exclusive
** Implemented when Trace option of OCDS is enabled

Verification Methods

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models.

The core satisfies the requirements of the Reuse Methodology Manual and the VSIA Quality IP Metric..

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available directly from Xilinx AllianceCORE member CAST, Inc. under the terms of the SignOnce IP License. Please contact CAST for pricing and additional information about this product. Contact information for them is on the front page of this datasheet. The R80515 core

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Related Information

- High-Speed Microcontroller Data Book, Dallas Semiconductor, 1995.
- CMOS single-chip 8-bit microcontrollers, Philips, 1996.
- Addendum to the MCS»51 Microcontroller Family, Intel, 1996.
- 8-bit Embedded Controllers, Intel, 1990

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