Digital Core Design

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Features

• Available under terms of the SignOnce IP License
• Harvard architecture 2 times faster compared to original implementation
• 33 instructions
• 12 bit wide instruction word
• Up to 256 bytes of internal Data Memory
• Up to 4K bytes of Program Memory
• Configurable hardware stack
• Power saving SLEEP mode
• Fully synthesizable, static synchronous design with no internal tri-states
• Scan test ready
• Technology independent HDL Source Code

Table 1: Example Implementation Statistics for Xilinx® FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Slices¹</th>
<th>IOB²</th>
<th>GCLK</th>
<th>BRAM</th>
<th>MULT/DSP48/E</th>
<th>DCM/CMT</th>
<th>MGT</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan®-3</td>
<td>XC3S200-5</td>
<td>58</td>
<td>271</td>
<td>28</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Spartan®-3E</td>
<td>XC3ES100-4</td>
<td>42</td>
<td>284</td>
<td>28</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-2 Pro</td>
<td>XC2VP2-7</td>
<td>106</td>
<td>270</td>
<td>28</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-4</td>
<td>XC4VFX12-12</td>
<td>90</td>
<td>285</td>
<td>28</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-5</td>
<td>XC5VLX30-3</td>
<td>138</td>
<td>204</td>
<td>28</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 10.1.00i</td>
</tr>
</tbody>
</table>

Notes:
1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming all core I/Os and clocks are routed off-chip
Applications
- Microcontrollers based applications.

General Description

The DFPIC165X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with fast memory (typically on-chip). The core has been designed with a special concern about low power consumption.

The DFPIC165X is software compatible with the industry standard PIC16C54, PIC16C55, PIC16C56, PIC16C57 and PIC16C58. It employs a modified RISC architecture (2 times faster than original implementation).

The DFPIC165X have enhanced core features and configurable hardware stack. The separate instruction and data buses allow a 12 bit wide instruction word with the separate 8-bit wide data. The DFPIC165X typically achieve a 2:1 code compression and a 8:1 speed improvement over other 8-bit microcontrollers in its class. The Core has 24 I/O lines and an 8-bit timer/counter with an 8-bit programmable prescaler.

The power-down mode SLEEP allow user to reduce power consumption. User can wake up the controller from SLEEP through an user reset or watchdog overflow. An integrated Watchdog Timer with it’s own clock signal provides protection against software lock-up.
Functional Description

Description of each block in the Figure 1 block diagram.

ALU

Arithmetic Logic Unit performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.

Control Unit

It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.

Hardware Stack

The DFPIC165X configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack when CALL instruction is executed or an interrupt causes a branch. The stack is popped while RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed two times, the third push overwrites the value that was stored from the first push.

RAM Controller

It performs interface functions between Data Memory and DFPIC165X internal logic. It assures correct Data memory addressing and data transfers. The DFPIC165X supports two addressing modes: direct or indirect. In Direct Addressing the 8-bit direct address is computed from FSR(7:5) bits 5 least significant bits of instruction word.

Indirect addressing is possible by using the INDF register. Any instruction using INDF register actually accesses data pointed to by the file select register FSR. Reading INDF register indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation. An effective 8-bit address is obtained from an 8-bit FSR register.

Timer 0

Main system’s timer and prescaler. The DFPIC165X Timer operates in two modes: 8-bit timer or 8-bit counter. In the “timer mode”, timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER prescale ration can be divided by 2, 4 .. 256. In the “counter mode” the timer register is incremented every falling or rising edge of T0CKI pin, dependent on T0SE bit in OPTION register.

Watchdog Timer

It is a free running timer. WDT has own clock input separate from system clock. It means that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode the WDT timeout causes the device to wake-up and continue with normal operation.

I/O Ports

Block contains DFPIC165X’s general purpose I/O ports and data direction registers (TRIS). The DFPIC165X has three 8-bit full bi-directional ports PORT A, PORT B and PORT C. Read and write accesses to the I/O port are performed via their corresponding SFR’s PORTA, PORTB, PORTC. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port’s pin has an corresponding bit in TRISA, TRISB and TRISC registers. When the bit of
TRIS register is set this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

Core Modifications

DFPIC165X can be fully customized accordingly to customer needs.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Signal Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>input</td>
<td>Global clock</td>
</tr>
<tr>
<td>clkwdt</td>
<td>input</td>
<td>Watchdog clock</td>
</tr>
<tr>
<td>por</td>
<td>input</td>
<td>Global reset Power On Reset</td>
</tr>
<tr>
<td>mclr</td>
<td>input</td>
<td>User reset</td>
</tr>
<tr>
<td>prgdata[11:0]</td>
<td>input</td>
<td>Data bus from program memory</td>
</tr>
<tr>
<td>ramdat[i][7:0]</td>
<td>input</td>
<td>Data bus from int. data memory</td>
</tr>
<tr>
<td>t0cki</td>
<td>input</td>
<td>Timer 0 input</td>
</tr>
<tr>
<td>porta[i][7:0]</td>
<td>input</td>
<td>Port A input</td>
</tr>
<tr>
<td>portb[i][7:0]</td>
<td>input</td>
<td>Port B input</td>
</tr>
<tr>
<td>portc[i][7:0]</td>
<td>input</td>
<td>Port C input</td>
</tr>
<tr>
<td>ramdatao[7:0]</td>
<td>output</td>
<td>Data bus from internal data memory</td>
</tr>
<tr>
<td>prgaddr[11:0]</td>
<td>output</td>
<td>Program memory address bus</td>
</tr>
<tr>
<td>ramaddr[7:0]</td>
<td>output</td>
<td>RAM address bus</td>
</tr>
<tr>
<td>ramwe</td>
<td>output</td>
<td>Data memory write</td>
</tr>
<tr>
<td>ramoe</td>
<td>output</td>
<td>Data memory output enable</td>
</tr>
<tr>
<td>sleep</td>
<td>output</td>
<td>Sleep signal</td>
</tr>
<tr>
<td>porta[i][7:0]</td>
<td>output</td>
<td>Port A output</td>
</tr>
<tr>
<td>portb[i][7:0]</td>
<td>output</td>
<td>Port B output</td>
</tr>
<tr>
<td>portc[i][7:0]</td>
<td>output</td>
<td>Port C output</td>
</tr>
<tr>
<td>trisa[7:0]</td>
<td>output</td>
<td>Data direction pins for Port A</td>
</tr>
<tr>
<td>trisb[7:0]</td>
<td>output</td>
<td>Data direction pins for Port B</td>
</tr>
<tr>
<td>trisc[7:0]</td>
<td>output</td>
<td>Data direction pins for Port C</td>
</tr>
</tbody>
</table>

Verification Methods

The DFPIC165X has been verified in simulation using fully automated testbench that includes several test programs. This testbench and set of tests are included in the HDL source package as a standard option.

Recommended Design Experience

The users should be familiar with the using of PIC microcontrollers and skilled in any programming language.
Ordering Information

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