Digital Core Design

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Features
- Available under terms of the SignOnce IP License
- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 9 levels pipelining
- 24-bit accuracy, 6 fractional decimal digits
- Results available at every clock
- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

Table 1: Example Implementation Statistics for Xilinx® FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Slices¹</th>
<th>IOB²</th>
<th>GCLK</th>
<th>BRAM</th>
<th>MULT/DSP48/E</th>
<th>DCM/CMT</th>
<th>MGT</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan®-3</td>
<td>XC3S50-5</td>
<td>89</td>
<td>473</td>
<td>70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Spartan®-3E</td>
<td>XC3ES100-4</td>
<td>70</td>
<td>473</td>
<td>70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-2 Pro</td>
<td>XC2VP2-7</td>
<td>139</td>
<td>473</td>
<td>70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-4</td>
<td>XC4VFX12-12</td>
<td>167</td>
<td>473</td>
<td>70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 7.1.04i</td>
</tr>
<tr>
<td>Virtex®-5</td>
<td>XC5VLX30-3</td>
<td>225</td>
<td>254</td>
<td>70</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>ISE® 10.1.00i</td>
</tr>
</tbody>
</table>

Notes:
1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming all core I/Os and clocks are routed off-chip

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Applications
- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

General Description
The DFPSQRT uses the pipelined mathematics algorithm to compute square root function. The input number format is according to IEEE-754 standard. DFPSQRT supports single precision real numbers. SQRT operation is pipelined up to 9 levels. Input data are fed every clock cycle. The first result appears after latency and next results are available each clock cycle. Precision and accuracy are parameterized.

Functional Description
The DFPSQRT Core is partitioned on the functionally independent blocks as shown in Figure 1. The blocks functionality is described below.

Arguments Checker
Performs input data analyze against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit
Performs floating point square root function. Gives the complex information about the results to Result Composer module.

Result Composer
Performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

Core Modifications
DFPSQRT can be fully customized accordingly to customer needs.
Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Input</td>
<td>Global system clock</td>
</tr>
<tr>
<td>rst</td>
<td>Input</td>
<td>Global system reset</td>
</tr>
<tr>
<td>en</td>
<td>Input</td>
<td>Enable computing</td>
</tr>
<tr>
<td>data[31:0]</td>
<td>Input</td>
<td>Data bus input</td>
</tr>
<tr>
<td>datao[31:0]</td>
<td>Output</td>
<td>Data bus output</td>
</tr>
<tr>
<td>ofo</td>
<td>Output</td>
<td>Overflow flag</td>
</tr>
<tr>
<td>ufo</td>
<td>Output</td>
<td>Underflow flag</td>
</tr>
<tr>
<td>ifo</td>
<td>Output</td>
<td>Invalid result flag</td>
</tr>
</tbody>
</table>

Verification Methods

The DFPSQRT has been verified in simulation using fully automated testbench that includes several test programs. The reference responses have been captured from an original IEEE-754 compliant coprocessor chip. This testbench and set of tests are included in the HDL source package as a standard option.

The DFPSQRT has also been verified using DCD testing board. The several square root set of tests were automatically compared to the reference results computed by PC coprocessor.

Recommended Design Experience

The users should be familiar with the floating point systems and skilled in any programming language

Ordering Information

This product is available directly from Xilinx Alliance Program member Digital Core Design under the terms of the SignOnce IP License. Please contact Digital Core Design for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Digital Core Design or visit the web:

Email: commonlicense@xilinx.com

URL: www.xilinx.com/ipcenter/signonce
DFPSQRT Floating Point Square Root

Related Information

Industry Information

For information on the Digital Core Design’s products and services, contact DCD or your local DCD representative.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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