JPEG 2000 Encoder (JPEG2K-E)

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AllianceCORE™ Facts

Provided with Core	
Documentation	Core specifications, integration manual
Design File Formats	EDIF or NGC netlist, Source RTL available at extra cost
Constraints Files	jpeg2k-e.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL
Reference designs & application notes	Application notes
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
ModelSim and NC-Sim	
Support	
Support provided by CAST, Inc.	

Features

- Available under terms of the SignOnce IP License
- ISO/IEC 15444-1 JPEG 2000 Image Coding System compliance
- Both lossless and lossy compression
- Error-resilient compression
- Rate control
- Headers syntax
- Performs both Tier-1 and Tier-2 operations; external processing not required
- Flexible Input Image Format:
  - Sub-sampling factors up to four for each component
  - Image/Tile size up to 4096x4096.
  - Up to four color components
  - Eight up to fourteen bits per sample
- Output format:
  - Proprietary attributes/coded data format
  - Standard compliant stream (jpc)
  - Standard compliant file (.jp2)
- Programmable JPEG 2000 options
  - 2D-DWT filter type (5/3 or 9/7)
  - Number of 2D-DWT levels
  - Quantatization tables

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax[1] (MHz)	Slices[1]	IOB[2]	GCLK	BRAM	MULT	External Memory (Mbytes)	Supported Video Format	Design Tools
Virtex™-4	XC4VFX80-12	100	27161	255	1	120	36	21.4	HD 720p, 30 fps	ISE™8.2.03i
Virtex™-5	XC5VLX85-3	120	11598	255	1	62	18	21.4	HD 720p, 30 fps	ISE™9.1.03i

Notes:

1) Results are only indicative as the core can be configured for higher/lower processing speed and higher/lower frame format support .

2) Assuming all core I/Os and clocks are routed off-chip.

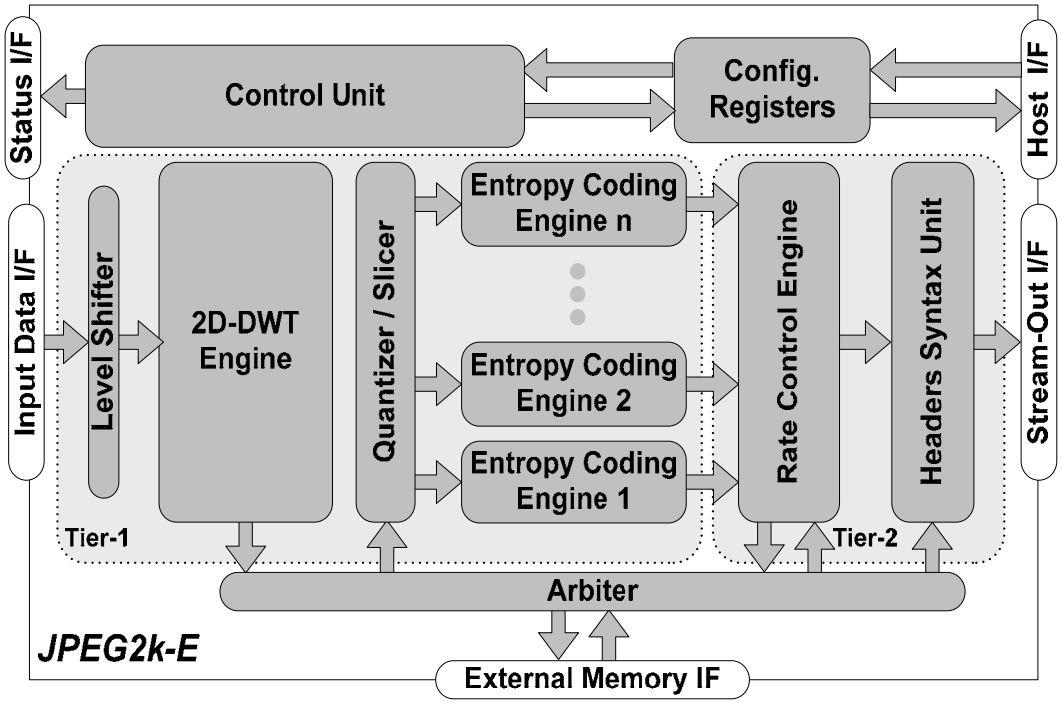

Figure 1: JPEG2K-E Function Controller Block Diagram

Features (continued)

- Entropy-coding switches (reset, restart, segmark)
- Input format (pixel depth, image/tile size, number of components, sub-sampling factors)
- Code-block size (64 or 32 or 16 on each dimension)
- Target compression ratio
- Architecture can be tuned during synthesis
  - Configurable number of Entropy Coding Units
  - Configurable maximum image/tile size
- Flexible Interfaces
  - 16-bit synchronous SRAM-style host interface
  - Dedicated pixel-in and stream-out interfaces
- Flexible, external memory interface, independent of memory type - supporting SRAM, SDR SDRAM, DDR/DDR2, SDRAM, and DQR SRAM - pin compatible with CAST's memory controller cores
- Fully synchronous single-clock domain design
- Sophisticated self-checking
- Bit accurate model in C

Applications

- Satellite, military, and other extreme surveillance systems
- Medical and other highest-quality video and image systems
- Digital still cameras and camcorders
- Networked video and image distribution systems
- Wireless video and image distribution systems
- Digital CCTV and surveillance systems
- Image and Video editing systems

General Description

The JPEG2K-E core is a complete, high-performance JPEG 2000 (ISO/IEC 15444-1) image compression solution targeted for video and high-bandwidth image compression applications. The core implements both Tier-1 and Tier-2 JPEG 2000 encoding — including rate control — in efficient custom hardware. Once programmed, the core operates independently to receive pixel data and output a fully-compliant video stream at the desired compression ratio. It can process individual frame or tile sizes up to 4096 x 4096 pixels, depending only on the external memory provided. Its high-performance processing achieves rates over 200 MSamples/sec in ASICs and over100 MSamples/sec in FPGAs. This competitive capacity and speed eliminate the need for parallel processing for even the most demanding applications such as HDTV.

The JPEG2K-E is a reliable and easy-to-integrate core as it is carefully designed, and rigorously verified. A complete verification environment eases integration, and a software bit-accurate model plus additional aids for system-on-chip simulation are included.

Functional Description

The JPEG2K-E operates either on an entire image or on a rectangular section of an image called a tile. The maximum supported image or tile size depends on the size of the external memory. With enough external memory, the core can support up to 4096x4096 images.
The core implements a simple and flexible external memory interface, making JPEG2K-E independent of memory type—supporting SRAM, SDR and DDR SDRAMAM, or QDR SRAM
The JPEG2K-E consists of several functional blocks, as shown in the block diagram and briefly explained here.
As encoding begins, the input pixels are first level-shifted and then transformed using either the reversible 5/3 or the irreversible 9/7 two-dimensional discrete wavelet transform. The transformed coefficients are stored in the external memory.
After an entire tile has been transformed, the transformed coefficients are quantized. The quantized coefficients are fed to the *Entropy Coding Engines* in a code-block per code-block basis.
The coded-segments along with the code-block attributes (truncation lengths and distortion metrics) produced by the *Entropy Coding Engines* are fed to the *Rate Control Engine*. If enabled, the *Rate Control Engine* implements a proprietary PCRD algorithm that outputs a code-stream at the required compression ratio with the minimum possible loss of quality.

Finally the *Headers-Syntax Unit* forms global, tile and packet headers, and outputs a compliant stream or file. This may be omitted from the core if it is not needed.

Core Modifications

JPEG2k_E can be modified so that it fits almost any applications needs in terms of processing speed. This is achieved by instantiating 1, 3, 6, 9 or 12 entropy-coding units. Furthermore, modifications regarding the core interface are also feasible.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Global Controls		
clk	Input	Clock
rst	Input	Asynchronous reset
clr	Input	Synchronous clear
Host Interface		
h_select	Input	Core select
h_r_wb	Input	Transfer direction
h_addr[7:0]	Input	Address bus
h_data_in[15:0]	Input	Write data bus
h_w_rdy	Output	Write ready: Core available for write
h_data_out_v	Output	Read data valid
h_data_out[15:0]	Output	Read data bus
Data-In interface		
i_pixel_v	Input	Pixel indicator. Indicates that pixel data reside in the i_data bus.
i_header_v	Input	Header indicator. Indicates that header/comment data reside in the i_data bus.
i_data[15:0]	Input	Input data bus.
i_data_rdy	Output	Data ready. Indicates that the core is ready to accept data.
Stream-Out interface		
s_data_rdy	Input	Stream ready. Indicates to the core that it can output stream data
s_data[15:0]	Output	Stream data bus
s_data_v	Output	Stream data valid. Mask valid data in output stream data.
s_sot	Output	Start of tile. Masks first word of a stream corresponding to a tile.
s_eot	Output	End of tile. Masks last word of a stream corresponding to a tile.
Status Interface		
busy	Output	Busy. Indicates that the core is busy processing image data.
cfg_error	Output	Configuration error. Indicates that some erroneous value has been found in the configuration registers.
External Memory Interface		
xtmem_clk	Input	Clock.
xtmem_rst	Input	Asynchronous reset line of the xtmem_clk clock domain.
xtmem_clr	Input	Synchronous reset line of the xtmem_clk clock domain.
xtmem_req_rdy	Input	Memory controller ready to receive a new request.
xtmem_req_val	Output	Access request valid.
xtmem_req[SP:0][1]	Output	Access request.
xtmem_wdata_rdy	Input	Memory controller ready to receive new write data.
xtmem_wdata_val	Output	Write data valid.
xtmem_wdata [15/31/63/127:0][1]	Output	Write data.
xtmem_wdata_mask	Output	Write data mask (1 bit per 16bit1 in the xtmem_wdata bust).
xtmem_rdata_rdy	Output	Core ready to receive new read data.
xtmem_rdata_val	Input	Read data valid.
xtmem_rdata [15/31/63/127:0][1]	Input	Read data.

[1] Configurable during synthesis

Verification Methods

The core has been verified through extensive simulation and rigorous code coverage measurements. The SDF model of the core has been fed with a number of images that have been efficiently decoded by the standard's reference software and the common Kakadu software. Furthermore, the core has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available directly from Xilinx AllianceCORE member CAST, Inc. under the terms of the SignOnce IP License. Please contact CAST for pricing and additional information about this product. Contact information for them is on the front page of this datasheet. The JPEG2K-E core is licensed from Alma Technologies, S.A. To learn more about the SignOnce IP License program, contact CAST or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Industry Information

- "JPEG2000: Image Compression Fundamentals, Standards and Practice", D. Taubman, M. Marcellin, Kluwer Academic Publishers, 2002

Xilinx Programmable Logic

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URL: www.xilinx.com/products/logicore/alliance/tblpart.htm