All Programmable: from Silicon to System

Ivo Bolsens,
Senior Vice President & CTO
Moore’s Law: The Technology Pipeline

**LOGIC DEVICE ROADMAP**

<table>
<thead>
<tr>
<th>$V_{dd}$</th>
<th>1.0/1.1V</th>
<th>0.9/1.0V</th>
<th>0.8/0.9V</th>
<th>0.7/0.8V</th>
<th>0.6/0.7V</th>
<th>0.5/0.6V</th>
<th>&lt; 0.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Gate Stack Engineering</td>
<td>Fully-depleted Channel Electrostatics</td>
<td>Band-Engineered Channel for Enhanced Transport</td>
<td>New Transport &amp; Extreme Channel Electrostatics</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Tech Node</th>
<th>32/28nm</th>
<th>14nm</th>
<th>7nm</th>
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<tbody>
<tr>
<td>imec</td>
<td>22/20nm</td>
<td>10nm</td>
<td>5nm</td>
</tr>
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</table>

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**XILINX ALL PROGRAMMABLE.**
Industry Debates Variability

Industry Debates Variability

EE Times
IMEC looks at variability beyond 10 nm
Anne-Françoise PELE
6/1/2012 5:10 PM EDT
PARIS - CMOS technology scaling will go on for the foreseeable future but, as we enter the 10nm node, process complexity reduction and variability control will become crucial and drive technology decisions, said An Steegen, senior vice president process technology at imec, at the annual IMEC Technology Forum last week at the Square meeting center in Brussels, Belgium.

EE Times
Intel FinFETs vary, may need SOI for shrink, says GSS
Peter Clarke
6/6/2012 7:01 AM EDT
LONDON - Intel's 22-nm FinFETs show physical variability according to cross-sectional photographs from engineering consultancy Chipworks Inc. (Ottawa, Ontario) and EDA company Gold Standard Simulations Ltd. (GSS) has attempted to model electrical characteristics of various examples.

One conclusion drawn by Professor Aern Asenov, CEO of GSS (Glasgow, Scotland), is that Intel may need to turn to silicon-on-insulator wafers to scale its FinFETs below 22-nm. This may also have implications for foundries which are yet to introduce FinFET technology into their chip manufacturing processes.

Variability Impact
14nm Bulk FinFET Case

Normalized delay - l; SVT

Supply voltage - [mV]
Industry Debates on Cost

COST PER GATE REDUCTION TRENDS

IBS

ARM 20nm Processors Expected to Arrive Next Year

Douglas Perry
6/5/2012 6:00 PM EDT

The chip manufacturing race is heating up and Intel could be putting pressure down the road.

Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless

Joel Hruska
March 23, 2012 at 12:13 pm

One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia

TSMC raises capex to record $8.5 billion, pulls in 20-nm

Peter Clarke
4/26/2012 12:23 PM EDT

LONDON – Taiwan Semiconductor Manufacturing Co. Ltd. has raised its planned capital expenditure for 2012 to between $8 billion and $8.5 billion. The move accompanied the announcement of first quarter financial results and strong second quarter outlook by the foundry.
Nothing New: Power Challenge

Challenge 1: Power

Power Density Race

- Sun’s Surface
- Rocket Nozzle
- Nuclear Reactor
- Hot Plate
- Pentium® processors

Multi-Core

Source: Intel

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Nothing New: Productivity Gap

![Graph showing the productivity gap between Logic Transistors/Chip and Transistor/Staff Month. The graph illustrates the 58% Yr. compound growth rate in complexity and the 21% Yr. compound growth rate in productivity.]

ESL Design Flow

IP Re-Use

Source: SEMATECH

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Nothing New: I/O Bandwidth Gap

Multi-Gigabit SerDes

Source: Xilinx, Inc.
“Doubt is not an agreeable condition, but certainty is absurd.”

François-Marie Arouet de Voltaire,
French Philosopher
“Don’t believe everything you read on the Internet.”

Abraham Lincoln,
U.S. President
Extending and Leveraging Moore’s Law

Add Value: Programmable System Integration
- Programmability
- 3D Integration

Collaborate
- Supply Chain
  - Wider – more Complexity
  - Deeper – earlier Engagement
- From System to Silicon
Value of Programmability: Configurability

Partial Reconfiguration
- Time-multiplexing hardware

Lower Power
Value of Programmability: I/O

- 28.05 Gb/s
- 13.1 Gb/s
- 12.5 Gb/s
- 6.6 Gb/s

Diagram showing connections between SFP+ Test Board, Optical, and Backplane with labels for Quad A and Quad B channels TX and RX.

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Value of Programmability: GOPS/Watt

From 100 Watt to 2 Watt
10x Performance Acceleration
Future Challenge: HW + SW co-design

Exploit Parallelism and Heterogeneity

OpenCL

C
Compile / Debug

AD9

Commercial Software Ecosystem

C-HLS
Accelerator synth

FPGA

Video codec
Encryption
Packet Processing
FFT
Search

Application-Specific

Exploit Parallelism and Heterogeneity
3D Integration: Add Value
Value of 3D Integration: Bandwidth/Watt

100x bandwidth/watt advantage over conventional methods
Value of 3D Integration: Cost/Gate

Big Single Monolithic Die

Multiple Small Die Slices

Greater capacity, faster yield ramp
Value of 3D Integration: Heterogeneous ICs

Mixed functions

Mixed processes
Value of 3D Integration: Heterogeneous ICs

- Highest bandwidth FPGA with 2.78 Tbps serial connectivity
- Electrically-isolated 28G transceivers for optimal signal integrity

![Diagram showing 3D integration with heterogeneous ICs, passive interposer, and noise isolation.](image)
Value of 3D Integration: Lower Power

**Silicon Interposer with 28nm FPGA Slices**

- 28 nm FPGA Slice
- 28 nm FPGA Slice
- 28 nm FPGA Slice
- 28 nm FPGA Slice

**7 Series Static Power vs. Logic Cells at Tj=85C and Max Process**

- Virtex-7 Monolithic
- Virtex-7 Multi-Slice

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3D Integration: Challenges Ahead

➢ Improve Cost
  – Wafer backside processing is complicated
  – “Device quality” wafers used for interposers
  – KGD methodologies still emerging

➢ Scalability
  – Micro-bump scaling is limited
  – Super-sized interposers.
  – Improve TSV aspect ratio

➢ Design Support
  – Multi-die analysis without Multi-mode
    Multi-corner explosion
  – Thermal modeling based on vertical hotspots
## 3D Integration: Industry Call-to-Action

<table>
<thead>
<tr>
<th>Design Enablement</th>
<th>Manufacturing Standards</th>
</tr>
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<tbody>
<tr>
<td>- Models</td>
<td>- DFM rules for TSV, µ-bump</td>
</tr>
<tr>
<td>- 3D Process Development Kit</td>
<td>- Materials TSV, µ-bump</td>
</tr>
<tr>
<td></td>
<td>- Thermal budget</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Test</th>
<th>Interoperability of Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Test HW</td>
<td>- Thin wafer handling</td>
</tr>
<tr>
<td>- Known-good-die method</td>
<td>- Shipping methods</td>
</tr>
<tr>
<td>- µ-bump probing</td>
<td>- Chip-to-chip interfaces</td>
</tr>
<tr>
<td>- Burn-in bare die</td>
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</tbody>
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Supply Chain Collaboration: Early Engagement

3D Integration

- Stacked Silicon Interconnect Development Started
- 90nm Process Integration And Modular Development Completed
- 90nm Test Vehicle Completed
- 65nm Test Vehicle Completed
- 28nm Test Vehicle Completed
- Design Tools Available
- Initial Reliability Assessment
- Design Enablement and Supply Chain Validation
- Process Qualification
- Design Validation
- World’s First 3D Stacked Silicon Interconnect Device

Heterogeneous Stacked Silicon Interconnect Technology

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Supply Chain Collaboration: Early Engagement

28nm Process Technology

- **2008**: Technology path finder
- **2009**: Integration and basic devices
- **2010**: Basic elements: RAM, RF, Std Cell, etc.
- **2011**: Circuit blocks, process-design interactions, pilot prep
- **2011**: More circuit blocks, & later products

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Continuous, early feedback loop for initial ramping
Enables accelerated learning – days vs. months
Supply Chain Collaboration: Mutual Benefit

FPGA architecture drives yield & quality improvements

The FPGA is a powerful yield learning vehicle with multiple layers of programmable features

Defect Reduction: quick to detect defects
If you can’t find it, you can’t fix it

Process Control: powerful to measure variations
If you can’t measure it, you can’t improve it
Today’s Supply Chain

R&D Consortia
- EDA
- Equipment Suppliers

Chip-on-Die
- Top side proc.
- Bot side proc.
- Bump
- Interposer
- I-poser attach
- 3rd party die
- Die stack
- Pkg assy
- Bump
- Bot side proc.

Chip-on-Wafer
- Top side proc.
- Interposer
- 3rd party die
- Die stack

Test
- Outside
- In-house

Mark
- Bin
- Std eFuse1 eFuse2
- FG

Wider and Deeper
From Silicon to System

- System Company
  - System Architecture
  - Applications SW

- Fabless Vendor
  - Product Features
  - Product IP/HW/SW
  - DFM

- Supplier
  - Package
  - Wafer

Questions:
- How to monetize SW?
- Power, performance, cost, integration
- How to ramp yield faster?
- Who controls 3D supply chain?
Conclusions

➢ Moore’s Law:
  - From mostly cost reduction to more value-based innovation

➢ System figure of merit defines value

➢ Xilinx programmable system integration
  - Programmability
  - 3D integration

➢ Supply chain partnerships to enable
  - Efficiency
  - Standardization
  - Innovation
What Xilinx Makes Possible:

ALL PROGRAMMABLE

ALL Programmable Electronic Systems

ALL Programmable Technologies

ALL Programmable Devices
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