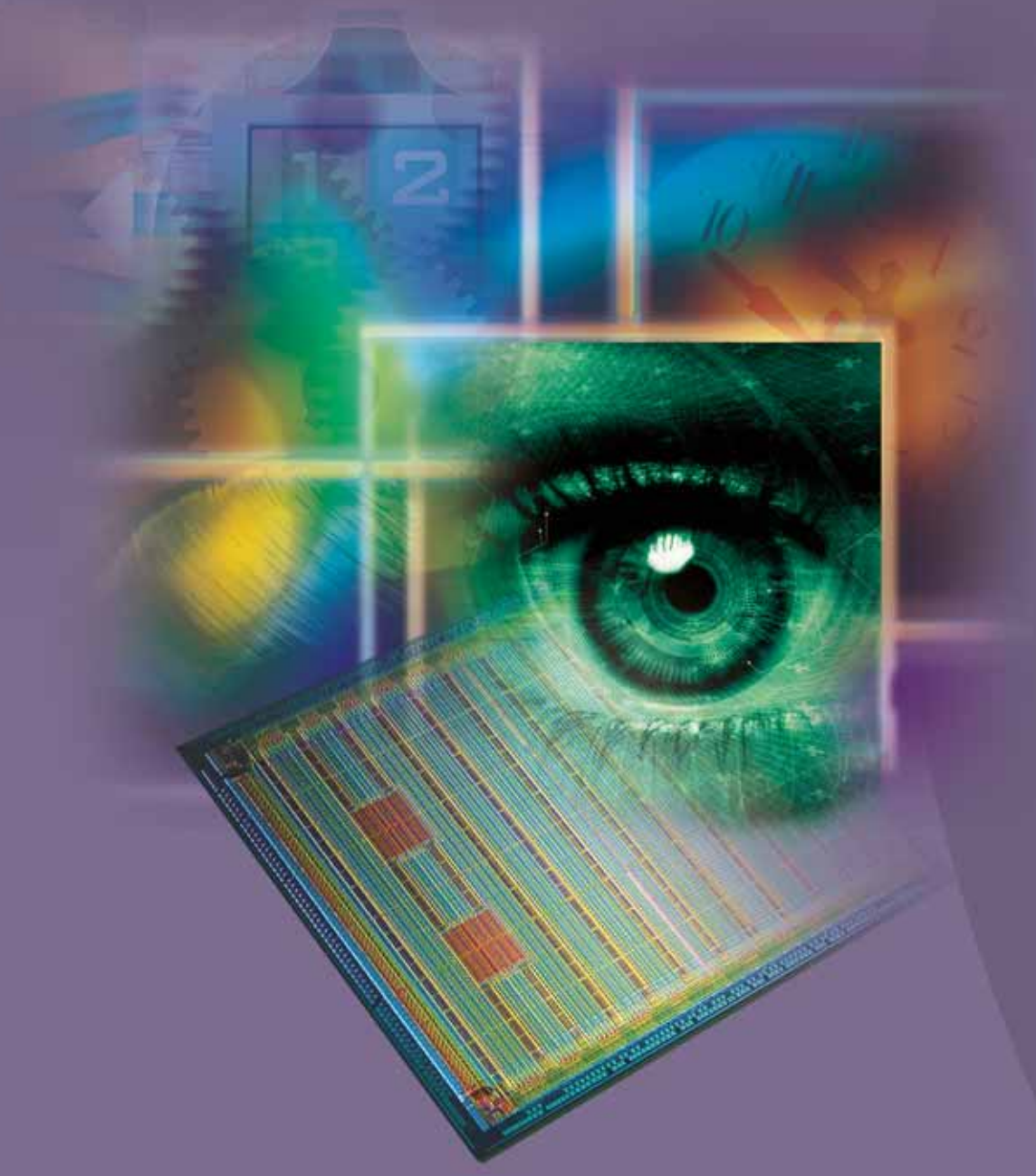
Issue 1
September 2005

Broadcast

Solution Guide



Seeing the Future of Broadcast Applications

INSIDE

XILINX®

Broadcast
Solution Guide

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Welcome to the first edition of the Xilinx *Broadcast Solutions Guide.*

At Xilinx® we understand the challenges that broadcast system architects and designers are facing. With many emerging new standards for connectivity, video processing, and video compression, you are left with difficult challenges when designing a broadcast system, especially with increasing time-to-market pressures. By offering solutions that are prevalent throughout the broadcast chain, our goal is to assist you with drop-in building blocks that will solve system-level design issues. Our goal is to support you with cost-effective solutions that will help you get to market faster, while helping you differentiate your product from your competition.

This guide offers a wealth of information dealing with broadcast-specific solutions and applications, including a variety of resources relating to connectivity, to help you with the challenges involved in designing high-speed serial digital video interfaces and data communication networks, and bridging between these previously unrelated domains. Additionally you'll find our IP and reference design guide, and application notes on our SDI, HD-SDI, DVB-ASI solutions, and many more. Also, read about the PCI-Express standard that is being adopted by many in the industry, and particularly our new low-cost solution based on the Spartan™-3 FPGA.

For video processing algorithms, this issue provides information that addresses color space conversion (RGB-to-YCbCr and YCbCr-to-RGB), compression elements including Huffman coding, variable length coding, DCT (discrete cosine transform), and traditional broadcast alpha keying using our DSP48 DDR technique. Our DSP solutions also extend to the communications side of broadcasting, with IP for various forward error correction techniques, and modulator components for satellite, cable, and terrestrial transmission.

We also offer a suite of validation platforms that can quickly and easily test your video processing algorithms or verify connectivity performance, including our new family of Virtex™-4 development boards. Talk to your local distributor about getting one of these boards so you can test your new algorithms long before you have your proprietary board back from fabrication and assembly.

We hope that you find this solutions guide valuable. It is, however, just a small sample of the information available to the broadcast engineer on designing with Xilinx programmable logic devices. For access to all the latest information on these subjects and more, please visit our website at *www.xilinx.com/esp/broadcast*.

Paolo Masini

Audio Video
Broadcast Marketing

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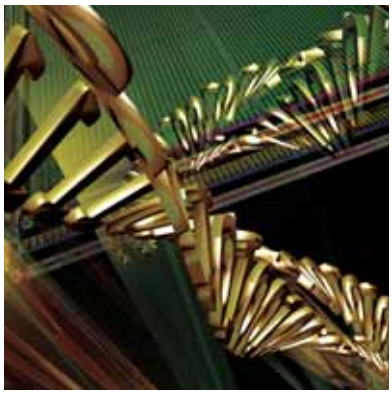

Learn more about broadcast solutions from Xilinx at: *www.xilinx.com/xcell/broadcast1/*

Developing Image Processing Algorithms with System Generator

System Generator allows you to easily implement and analyze any image processing algorithm.

by Daniel E. Michek
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Converting image processing algorithms to FPGA implementations can be tedious. The algorithm may be proven in software but with no direct link to actual implementation. Additionally, it can be difficult to subjectively verify the implementation.

Using a mathematical simulator to verify and create HDL implementation files bridges the gap from the algorithm architect to the FPGA engineer. Xilinx® System Generator for DSP allows for high-level mathematical verification and converts the heart of the algorithm into ready-to-use HDL.

Simulation inside of The MathWorks Simulink® tool enables you to easily verify the image algorithm qualitatively and subjectively when used with the Image Processing Toolbox, also from The MathWorks. Using System Generator to develop and implement image processing algorithms allows for a thoroughly verified and easily executed design; plus, you save time on subjective analysis of the HDL. The high-level block diagram allows for easy communication between team members, resulting in less time spent crossing skill boundaries when determining implementation trade-offs.

The Basics

The Image Processing Toolbox is an excellent starting point with which to develop image processing algorithms for FPGAs. It allows you to easily load and view many image types. Although not directly usable within System Generator, it can also rotate, resize, filter, convert to and from the frequency domain, and operate on the image mathematically and morphologically. You can use these latter functions as a qualitative measure against the actual System Generator implementation.

Exchanging Data

Images are often stored and manipulated as two-dimensional arrays that can be quite large. For example, a 1,024 x 1,024 x 8-bits-per-pixel image is 1 MB. Typically, a portion of the image is moved into the FPGA one pixel at a time and aggregated into a larger unit (often a line), with manipulations performed on these points.

An example pre-processing MATLAB® m-file script might contain:

- Reading in a source test image using the IMREAD function in the Image Processing Toolbox.
- Analyzing variables such as width, height, and color depth of the image to pass as arguments to Xilinx block set tokens. This enables easy parameterization and scaling of the application.
- Storage and creation of other variables necessary to the application. Examples include rotation angle, resizing percentages, and bit precision within the algorithm.
- Converting the matrix data from an m x n array to a 1 x (m*n) with "for loops" and concatenation. This allows The MathWorks DSP block set "Signal From Workspace" token to pass elements as samples to the Xilinx block set "Gateway In" token.
- Viewing the source test image for later subjective analysis using the IMSHOW function in the Image Processing Toolbox.

An example post-processing m-file might contain:

- Conversion of "ToWorkspace" variables from a 1 x (p*q) array to a p x q array for easy manipulation by using "for loops."
- Displaying the resulting matrices using IMSHOW for subjective analysis.
- Computing qualitative analysis of the results versus the original image or an algorithm developed with the Image Processing Toolbox.

Using M-Files

You can use m-files to model the algorithm before implementation with System Generator. Although this step is optional, it can be a highly effective aid in the slight paradigm shift from matrix operations in software to raster scan operations in a highly parallel architecture.

Some of the key benefits include:

- Deconstruction proofs of Image Processing Toolbox functions as an aid to understand the algorithm.
- Creation of intermediate variables to assist in debugging the System Generator version of the design. Try to set variables similar to how they will appear in the design. Two-dimensional matrices should be used as memory, while raster order works better between blocks.
- Making algorithm trade-offs. Ask yourself if you should place the bi-linear interpolation stage before or after the sending of data to memory.
- A fast proof that the algorithm is on the right track.
- Qualitative analysis from the deconstruction m-file to the corresponding Image Processing Toolbox function.

Design Considerations – An Example

Real-time image rotation has many challenges when going from the algorithm architect at a high level to the FPGA engineer at the HDL and board level. The algorithm level choices that you will make about how to implement the design in the FPGA will affect device utilization. Conversely, board and system requirements may place limitations on your design, such as number, width, and type of frame buffer memories.

Design Choices

A key decision about the architectural style of the rotation algorithm is quality. For example, when moving the pixels of the original image grid to fractional locations on the rotated image grid, is a nearest neighbor selection adequate? Should you perform bi-linear interpolation on the image to reduce shear (the tendency to see discontinuities along object edges)? Is bicubic interpolation (determining the new pixel value based on weighting and summing its closest 16 neighbors) the preferred method? Your choice of quality will impact resources in both the FPGA and the frame buffer.

Our example is based upon the Hotelling transform to determine the original image versus the rotated image pixel addresses. You have two choices as to where the rotation engine occurs with respect to frame buffering:

1. Place the rotation engine after the frame buffer. This has the effect of sequential raster scan address writes into the frame buffer and allows for raster scan format of the output data by reading from the frame buffer in non-sequential address form. The Hotelling transform with basis vectors cos(t) and sin(t) for rotation angle (t), {Sx,Sy} representing source x and y coordinates, and {Dx,Dy} representing destination x and y coordinates in the 2-D image are:

$$Sx = Dx * \cos(t) + Dy * \sin(t)$$

$$Sy = Dy * \cos(t) - Dx * \sin(t)$$

2. Place the rotation engine before the frame buffer. In effect, this method predetermines and weights the values stored through non-sequential addressing into the frame buffer. The output data is read in raster scan format from the frame buffer. The Hotelling transforms with similar representation as above are:

$$Dx = Sx * \cos(t) - Sy * \sin(t)$$

$$Dy = Sy * \cos(t) + Sx * \sin(t)$$

In their paper, "Real Time Image Rotation and Resizing, Algorithms and Implementations" (*www.xilinx.com/products/logicore/dsp/rotation_resize.pdf*), my Xilinx colleagues Robert Turney and Chris Dick showed that this approach is more economical in terms of memory bandwidth. Because the data is stored to the frame buffer in non-sequential order, you must take care to ensure that all valid pixel locations are written to.

Also, if the rotation angle is changed, you must clear artifacts in the corners from the previous frame from the frame buffer. A nearest neighbor rotation of 45 degrees clockwise demonstrates the void artifacts, as shown in Figure 1, that occur due to multiple input pixels being written to the same frame buffer address.

Figure 1 – Void artifacts when rotation engine occurs before the frame buffer

To avoid a complex control path and concentrate mostly on the data path, our example goes with the first choice previously described (place the rotation engine after the frame buffer). The net effect will be an increase in memory bandwidth of 4 or 16 times for bi-linear and bi-cubic interpolation, respectively. The choice of how to deal with the increase in bandwidth requirements is design- and memory-dependent.

You can increase the number of read accesses from the memory by a factor of four to minimize the total amount of memory for bi-linear interpolation. This will decrease the overall incoming pixel rate by a factor of four unless the memory access speed is sufficient to handle the offset. Alternatively, you can store the four pixels necessary for bi-linear interpolation at the

same address location, thus increasing the total amount of memory by a factor of four. This methodology can be mitigated based on pixel bit width – that is, 8-bit-wide pixels can use this approach to fit into a 32-bit-wide memory footprint.

Design Implementation with System Generator

Our example will implement image rotation with the following assumptions:

- Input image size and pixel widths are known at the time of implementation
- Use the Hotelling transform of the form:

$$Sx = Dx * \cos(t) + Dy * \sin(t)$$

$$Sy = Dy * \cos(t) - Dx * \sin(t)$$

- Bi-linear interpolation
- Increased memory bandwidth is accounted for by reading the data out of the frame buffer four times faster than the incoming pixel rate

Frame Buffer Read Address Generation

Because the data will be output in raster scan format, you can create the destination address with two counters representing the two dimensions. These values must be center-adjusted around zero before being transformed. At this point, any adjustment changes the center of rotation for the output image.

The following two examples demonstrate manipulating the output image by using minimal extra logic:

- Two adders are all that are required to add pan control for the output image.
- Using two multipliers, you can scale the destination addresses to zoom in or out from the center point.

As interpolation occurs at a later stage, zooming and panning at this point will result in an output image with each pixel uniquely interpolated, versus a simple copy or additional interpolation procedure later. Figure 2 demonstrates a 45-degree counter-clockwise rotation with 8x zoom.

Once the destination address is correct for center, pan, and zoom, the transform is applied. The resulting addresses are reverse-corrected for the centering function. The numbers are of the form integer with a decimal portion. The integer portions are the required source address locations to read from the frame buffer. The decimal portions are used to create weighting factors used for the bi-linear interpolation.

Figure 2 – Zoom and pan incorporated into the algorithm

Figure 3 – Original picture for subjective comparison

Figure 4 – Image rotated counter-clockwise 7.5 degrees, followed by rotation clockwise 7.5 degrees.

Weighting the Data

Four pixels are fetched from the frame buffer to create a 2 x 2 matrix containing the source address pixel and its original neighbors to the right, below, and below-right, which we will identify as XY, XpY, XYp, and XpYp, respectively. The source address transform uses the decimal portions of {Sx,Sy} represented as {Rx,Ry} to create the following weighting equations:

- Weighting(XY) = Wxy = (1 – Rx) (1 – Ry)
- Weighting(XpY) = Wxpy = (Rx) (1 – Ry)
- Weighting(XYp) = Wxyp = (1 – Rx) (Ry)
- Weighting(XpYp) = Wxpyp = (Rx) (Ry)

These equations can be shown to be equal to the following equations to reduce the number of multipliers necessary from four to one:

- Wxy = (1 – Rx) – Wxyp
- Wxpy = (Rx) – Wxpyp
- Wxyp = (Ry) – Wxpyp
- Wxpyp = (Rx) (Ry)

The interpolated pixel value is the summation of the 2 x 2 matrix pixels multiplied by their respective weighting functions.

Compare the original image in Figure 3 with an image that was rotated through 7.5 degrees, followed by a -7.5 degree rotation in Figure 4.

Conclusion

In this article, I've shown how to use System Generator to explore and implement image processing algorithms.

The use of a mathematical simulation tool with image handling capabilities allows you to easily investigate various options in an intuitive capacity. Although this example shows an image rotation implementation, these same methodologies can help you develop any image processing algorithm.

If you have any questions or suggestions, call me, Daniel Michek, at (858) 431-5901, or send me an e-mail at *daniel.michek@xilinx.com.*

A Low-Cost PCI Express Solution

Spartan FPGAs are ideal for next-generation PCI applications and systems.

by Abhijit Athavale
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PCI has been the most widely used bus standard in the PC, server, and embedded markets for the past decade. Because PCI is limited by its shared, central arbitration-based architecture and system-synchronous clocking scheme, current and next-generation processors are outstripping its ability to keep up.

PCI's emerging replacement is PCI Express, a new connectivity standard that preserves the flexibility and familiarity of PCI while dramatically increasing bandwidth and performance. The controlling body for the PCI specification, the PCI SIG, has ratified PCI Express as the next-generation PCI. PCI Express-based products are now becoming available; shipments are expected to achieve high volume as early as 2006. Figure 1 shows the adoption forecast for PCI Express.

PCI Express uses serial I/O technology to create point-to-point connections and is reverse-compatible to PCI, preserving many original PCI advantages. It scales from a single lane (1x) to a 32 lane (32x) architecture, offering a bandwidth of 2.5 Gbps per lane. PCI 32/33 has a bandwidth of 1 Gbps, while PCI 64/66 has a bandwidth of 4 Gbps.

The 1x PCI Express implementation matches up very well with PCI 32/33, the most commonly used PCI interface across all markets. A two-lane implementation (5 Gbps) is an incremental improvement over PCI 64/66. At the high end, a 32-lane PCI Express implementation supports a total of 80 Gbps, providing more than enough bandwidth to support the vast majority of next-generation applications.

Implementation Details

PCI Express is a three-layer specification: physical (PHY), logical, and transport, all defining separate functionalities. Also included in the specification are advanced features for hardware error recovery and system power management. (For more information about PCI Express, visit *www.pcisig.com*.)

Since 2000, Xilinx® has offered a line of PCI 32- and 64-bit solutions for Spartan™ series FPGAs. The most logical successor is a PCI Express solution using an external PHY chip paired with a Spartan-3 or Spartan-3E device. The PCI Express specification defines an interface to hook a PHY chip up to a separate device that houses the logical and transport layers (called a PIPE interface – a white paper about this is available from Intel).

In the two-chip solution, the transport layer resides in a dedicated PHY chip, and the logic and transport layers reside in a Spartan FPGA. A broad range of PHY devices are available from manufacturers such as Genesys Logic, Philips Semiconductor, and Texas Instruments. PHY pricing will be less than $10 for high volumes (250,000 units per year). (See the sidebar, "PHY Vendors," for contact information.) Xilinx has collaborated with Phillips Semiconductor and delivered this solution to our customers.

To implement the interface, Xilinx and several of our IP partners (including Eureka, GDA, and Northwest Logic) provide PIPE IP cores for Spartan-3 and Spartan-3E devices. A single-lane PCI Express controller requires approximately 500,000 gates (50% of a Spartan XC3S1000) for the logical and transport layer core, leaving the rest of the FPGA available for the user application (see

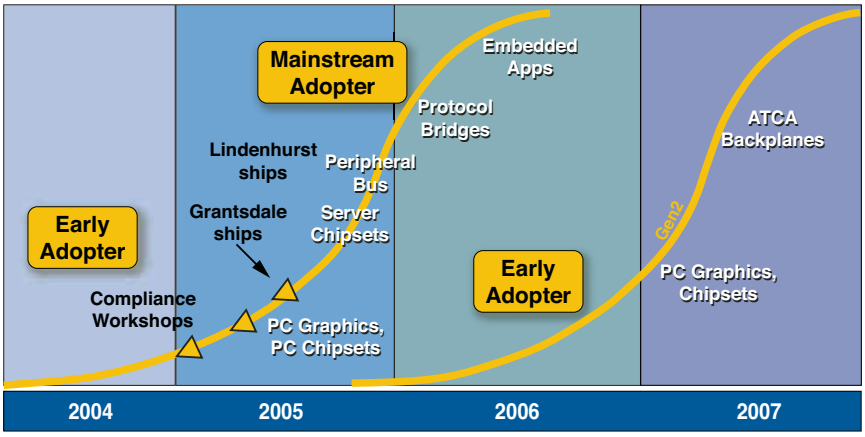

Figure 1 – PCI Express adoption forecast

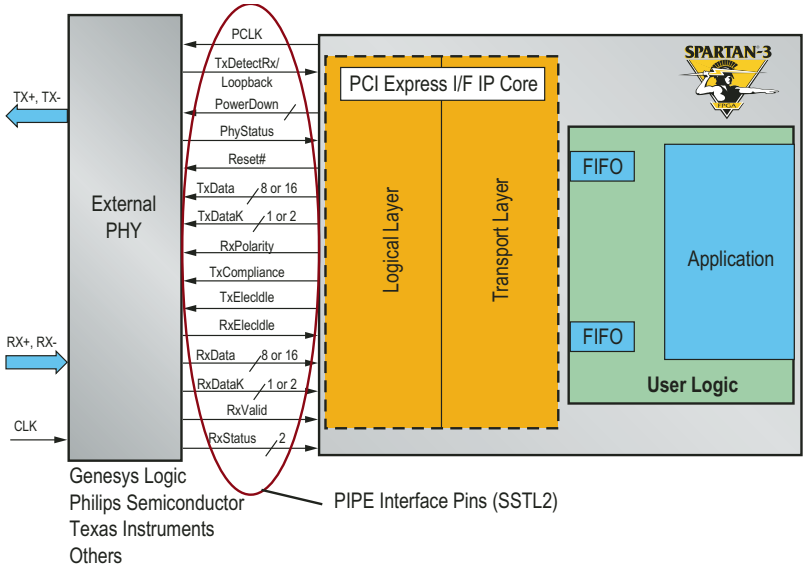

Figure 2 – PIPE interface between a Spartan FPGA and an external PHY

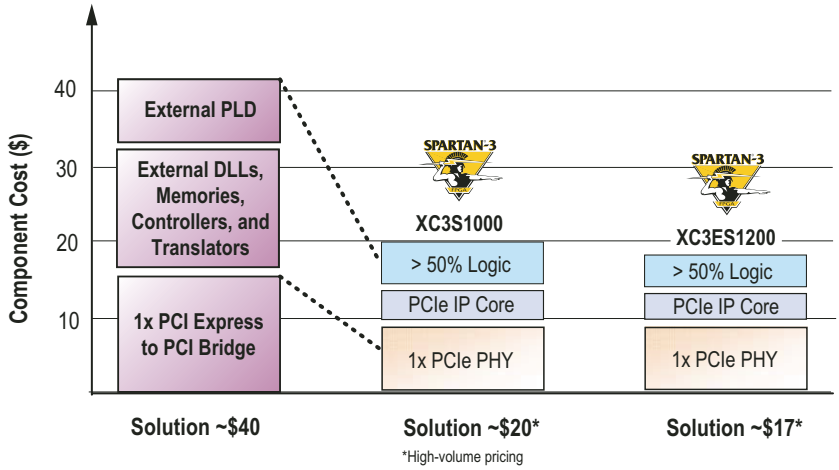

Figure 3 – Single-lane PCI Express implementation options

the "PCI Express Core IP" sidebar for details on Northwest Logic's product and *www.xilinx.com/pciexpress/* for details on PCI Express IP from our other IP partners.) Figure 2 shows the implementation of a PIPE interface using a Spartan FPGA and external PHY.

Figure 3 illustrates a range of options to implement a single-lane PCI Express interface. The cost of a standard-product option is fairly high (>$40), making it tenuous for high-volume/low-cost applications. The Spartan options drop that cost substantially, and add the flexibility of programmable logic to integrate and implement other system capabilities. In 250K quantities (reasonable for typical consumer applications), the Spartan-3E version will cost approximately $17.

Conclusion

In addition to reducing total costs, the Spartan FPGA + PHY option gives you substantial flexibility to build "PCI Express-to-anything" bridges and integrate other circuit elements. As most systems have a range of bandwidth requirements, preserving flexibility is important so that you can add lanes without dramatically changing the layout.

Spartan-3 and Spartan-3E FPGAs are available in a wide range of densities, and preserve migration up and down in overall bandwidth. And because FPGAs are fully reprogrammable post-deployment, they eliminate the risks associated with first-generation ASSPs and ASICs.

If you are currently using PCI for your interconnect standard and are architecting your next-generation designs, you should consider the PCI Express option from Xilinx. We encourage you to find out how Spartan-3 and Spartan-3E FPGAs will help you meet your current and future design requirements. More information about Spartan-3 and Spartan-3E FPGAs, PCI Express IP, and compatible PHY devices is available at *www.xilinx.com/pciexpress/*.

PCI Express IP

PCI Express IP cores are available from multiple vendors including Xilinx and our partners. One such core from Northwest Logic is featured below.

Northwest Logic's PCI Express Core is specifically designed for low-cost Spartan-3 FPGAs. A Spartan-3-based PCI Express design uses the Spartan-3 device with a low-cost physical interface for a PCI Express (PIPE)-compatible PHY chip. The PHY chip implements the low-level PCI Express physical layer, while the device takes care of the upper-level data link and transaction layers.

Another version of the PCI Express Core uses the internal MGTs in Virtex-II Pro and Virtex-4 FX FPGAs to provide a fully integrated PCI Express solution.

Northwest Logic's PCI Express Core is one of the smallest PCI Express cores available, enabling you to target the smallest and consequently lowest cost FPGA. The core is provided with a comprehensive verification suite and expert support to ensure rapidly developed and validated designs.

Also available is a PCI Express Development Board for quickly prototyping a complete PCI Express System. A demo GUI, drivers, and PCI Express FPGA reference design are also included.

For more information (including pricing and core size for a particular FPGA family), visit the Northwest Logic website at *www.nwlogic.com.*

PHY Vendors

Genesys Logic
www.genesysamerica.com

Philips Semiconductor
www.semiconductors.philips.com

Texas Instruments
www.ti.com/pciexpress/

Achieve Breakthrough Performance in Your System

Virtex-4 FPGAs set new records in system performance while consuming minimal power and providing superior signal integrity.

by Adrian Cosoroaba
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Performance in today's systems is defined by more than FPGA clock rates. Every system has different requirements, and the maximum achievable performance is determined by various factors such as logic fabric performance, I/O bandwidth, embedded processing, and DSP performance, among others. These requirements can also be subject to power restrictions, as well as signal integrity and cost budgets.

Xilinx® developed the Virtex™-4 FPGA family after consulting hundreds of customers to address these requirements and make it easier than ever to meet system performance goals. In this article, we'll look at how Virtex-4 FPGAs provide new and unique capabilities to help you meet diverse requirements for system performance.

System Design Challenges

With each new generation of devices, semiconductor vendors are able to offer higher clock rates, due to shrinking process geometries. However, today's system performance challenges go beyond traditional glue logic and maximized clock rates. In a PC, for example, the real system performance bottleneck lies not in clock frequency but in how the other blocks of the system work together at the desired frequency.

Let's consider these challenges in the perspective of applications employing high-performance FPGAs. Seemingly diverse applications like video stream processing, packet data processing, storage systems, wireless base stations, and many others incorporate similar functions, including:

- Incoming and outgoing data streams
- Bridging multiple connectivity standards
- Arithmetic and DSP (signal conditioning and data processing)
- External memory interfacing
- State machines
- Data buffering
- Embedded processing (Figure 1)

To facilitate these applications, Virtex-4 FPGAs include common building blocks as embedded – yet parameterizable – hard IP. The integration of complex functions like DSP slices, embedded CPUs, dedicated I/O circuitry, and on-chip RAM (block RAM, FIFOs) provides you with unprecedented capabilities to build programmable systems within a single FPGA device.

Meeting system requirements takes the right combination of I/O bandwidth, programmable logic, on-chip RAM, DSP, and embedded processing. To provide the ideal combination of functions, Virtex-4 FPGAs come in three flavors (LX, SX, and FX platforms) comprising 17 devices.

Virtex-4 FPGAs offer not only enhanced logic fabric capabilities, but also customized XtremeDSP™ MACs and embedded PowerPC™ processors that give you enough performance headroom to reach your design performance goals.

I/O bandwidth is often the limiting factor in the quest for performance. To remove I/O bottlenecks, Virtex-4 FPGAs have unique built-in 1 Gbps ChipSync™ source-synchronous circuitry and 622 Mbps to 10.3125 Gbps serial transceivers that can help you achieve bandwidth targets.

System Performance Categories

Let's look at various aspects of performance and Virtex-4 FPGAs in the context of seven major performance categories: logic fabric, embedded processing, DSP, on-chip RAM, high-speed serial, I/O memory bandwidth, and I/O LVDS bandwidth. Figure 2 offers a comparison with the nearest 90 nm FPGA vendor in each of these categories.

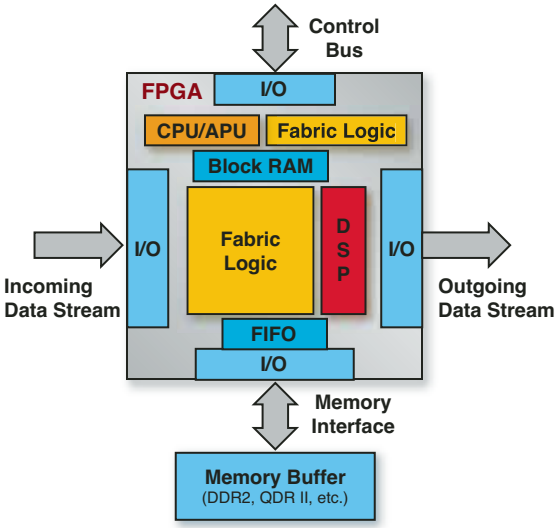

Figure 1 – FPGA-based system

Logic Fabric Performance

Xilinx enhanced the performance of its already fast programmable logic fabric by building Virtex-4 devices with advanced 90 nm technology. A flexible look-up table (LUT) architecture (with the ability to covert any LUT into a 16-bit RAM or 16-bit shift register), a high-speed carry chain, and arithmetic blocks provide further performance gains.

The 500 MHz global clocking structure, the key driver behind logic performance, is fully differential to reduce skew, jitter, and duty-cycle distortion. Virtex-4 FPGAs also provide a hierarchical clocking structure (global and regional clocks) and clock management circuitry. Evaluations of logic fabric performance using a suite of real-world designs demonstrate a performance advantage as much as 70% above our nearest 90 nm competitor. Averaged across this suite of designs, the Virtex-4 performance advantage is 15%. This performance boost means that Virtex-4 devices effectively provide an extra speed-grade advantage.

Embedded Processing

Virtex-4 FX platform FPGAs provide up to two enhanced PowerPC 405 cores, each delivering 702 DMIPS performance

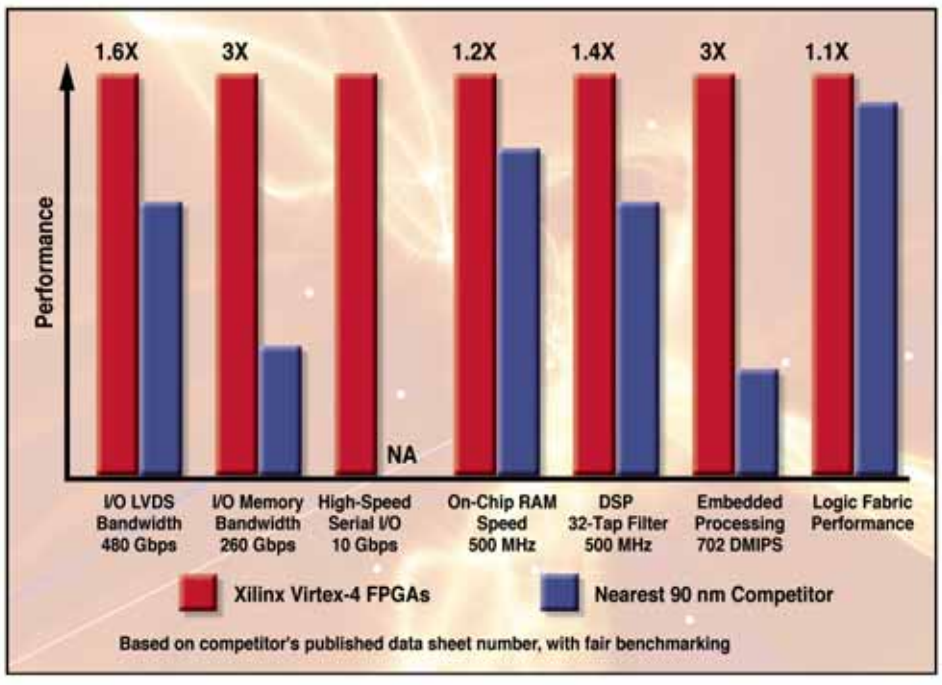

Figure 2 – Performance comparison for Virtex-4 FPGAs

at 450 MHz, while consuming only 0.45 mW/MHz. This is more than three times the performance of the best soft microprocessor cores.

Moreover, the new Auxiliary Processor Unit (APU) controller makes it easy to reach even higher levels of performance by integrating custom co-processors and hardware accelerators. The APU controller provides a low-latency path for connecting co-processor modules implemented in the FPGA to the embedded PowerPC processor. These user-defined, configurable hardware accelerator functions operate as extensions to the PowerPC 405, offloading the CPU from demanding computational tasks. For example, implementing floating-point calculations in hardware improves performance by a factor of 20 over software emulation. A 10/100/1000 Mbps tri-mode Ethernet MAC implemented alongside a PowerPC processor enables Ethernet connectivity.

DSP Performance

The XtremeDSP™ slice is a versatile, user-configurable block providing twice the DSP performance of previous implementations while drawing less than 1/7th the power. Each slice contains a dedicated two's complement, signed 18 x 18 bit multiplier, and a three-input adder/subtracter/accumulator with feedback path. With as many as 512 XtremeDSP slices running at 500 MHz, a single Virtex-4 FPGA delivers 256 GigaMAC/s (18 x 18 GMACs) performance.

You can configure the XtremeDSP slices to implement multipliers, counters, multiply-accumulators, and many more functions, all without consuming logic fabric resources. The ability to implement complex systolic functions without incurring the delay of fabric routing provides significant performance gains. For example, in a 32-tap FIR implementation, the Virtex-4 FPGA outperforms competing devices by 40%.

On-Chip Memory Performance

The Virtex-4 family carries forward the size and basic structure of on-chip memory, 18 Kb dual-port block RAM (proven in previous generations), but adds a data-output pipeline register to increase speed to 500 MHz. The two ports still have individual width control, and in write mode you can choose between automatically reading the previously stored data or the new data. Two neighboring block RAMs, when combined, form a 32K x 1 RAM without loss of speed, or a 512-deep 64-wide RAM with automatic Hamming error correction – without using any extra logic.

Each block RAM also contains its own FIFO controller, a unique Virtex-4 FPGA feature that provides 500 MHz functionality without additional logic resources. Compared to competing devices, the block RAMs provide at least 20% better performance.

But getting your FPGA internal blocks to run fast is only half the battle. Maximum system performance requires efficient interaction between the FPGA and other components in your system. Virtex-4 FPGAs offer the flexibility to achieve the highest possible bandwidth for chip-to-chip, board-to-board, and box-to-box connectivity.

High-Speed Serial I/O

As designs move to faster interface speeds, serial interconnect saves power and board space while reducing design complexity and cost. Virtex-4 RocketIO™ MGTs offer performance from 622 Mbps to 10.3125 Gbps, one of the broadest ranges offered by any device. The transceivers are fully programmable and can implement a myriad of speeds and serial standards. Link-layer IP is available for such standards as PCI Express, Serial-ATA, Fibre Channel, Gigabit Ethernet, and Aurora.

Memory I/O Bandwidth

The great majority of systems today need a data buffer external to the FPGA for temporary storage. This buffer's bandwidth can be the critical factor in determining overall performance.

Memory interfaces like DDR2 SDRAM, QDR II SRAM, or RLDRAM II are source-synchronous, with per-pin data rates of more than 533 Mbps. Memory bandwidth is determined not only by the per-pin data rate but also by the width of the bus. The ChipSync circuitry built into every I/O simplifies the physical layer interface and provides the capability to implement buses three times wider than other programmable solutions, for bandwidths as high as 260 Gbps.

To enable reliable data capture, ChipSync circuitry also includes built-in delay elements, adjustable in 75 ps increments, to ensure the proper alignment between clock and data signals. The unique capability to calibrate timing at run time, rather than at design time, substantially improves design margins. Xilinx also provides hardware-verified reference designs, development systems, and software tools to further speed up the implementation of memory interfaces.

LVDS I/O Bandwidth

ChipSync technology simplifies the design of differential parallel bus interfaces, with embedded SERDES blocks that serialize and de-serialize parallel interfaces to match the data rate to the speed of the internal FPGA circuits. Additionally, this technology provides per-bit and per-channel de-skew for increased design margins, simplifying the design of interfaces such as SPI-4.2, XSBI, and SFI-4, as well as RapidIO.

Virtex-4 FPGAs incorporate ChipSync technology into every I/O, providing the most flexible I/O solution available. This enables wider 1 Gbps LVDS buses for up to 480 Gbps bandwidth, 60% higher than the competition.

Other Performance Challenges

Achieving the desired system performance with your FPGA is often impeded by signal integrity, cost, and power budget restrictions.

The innovative Application Specific Modular Block (ASMBL) architecture enables I/O, clock, power, and ground pins to be located anywhere on the silicon chip, not just along the periphery. This architecture alleviates the problems associated with I/O and array dependency, power and ground distribution, and hard-IP scaling.

Furthermore, the Virtex-4 FPGA packaging technology, SparseChevron, enables distribution of power and ground pins evenly across the package. The benefit to you is improved signal integrity. As

demonstrated by Dr. Howard Johnson, Virtex-4 FPGA devices have seven times less simultaneously switching output (SSO) noise and crosstalk when compared to competing devices.

The ASMBL architecture, with its column-based implementation of programmable logic, DSP slices, block RAM, I/O columns, MGTs, clocking, and PowerPC embedded cores, provides another significant benefit in that it allows a more flexible allocation of resources. This enables Xilinx to offer three Virtex-4 FPGA platforms: the LX platform, optimized for logic resources; the SX platform, optimized for DSP; and the FX platform, optimized for embedded processing and high-speed serial applications.

Device power budgets impose an additional impediment to meeting performance goals. Because power consumption increases with clock rate, you may exceed your power budget at frequencies below your performance target, even if your chosen device has more performance on tap. Selecting a device with low power consumption will help you achieve performance goals while staying within your power budget, and can deliver the additional benefits of lower system cost and higher reliability through reduced power supply and cooling requirements.

Virtex-4 FPGAs incorporate unique triple-oxide 90 nm technology that significantly reduces static power. Additionally, by implementing commonly used functions such as embedded IP, Virtex-4 FPGAs further reduce dynamic power when compared to previous generations or competing devices. Measurements and analysis of Xilinx against competing tools and silicon show that Virtex-4 FPGAs consume 1 to 5W less than the competition's 90 nm FPGAs.

Conclusion

Virtex-4 FPGAs incorporate innovative built-in silicon features, extensive embedded IP, triple-oxide 90 nm technology, and unique packaging to provide designers with capabilities that enable breakthrough performance at the lowest cost.

For more information about getting started with your Virtex-4 FPGA design, visit *www.xilinx.com/virtex4*.

Using System Generator for DSP to Create the J.83 Cable Modulator

System Generator enables the rapid development of multi-channel cable head-end modulators to provide a true low-cost solution.

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The increased capability and capacity of video, audio, data, and interactive services through cable distribution has spurred much interest. Applications such as video-on-demand and cable telephony are natural extensions of these services.

The ITU-T (International Telecommunications Union – Telecommunication Standardization Sector) has established the J.83 specification to standardize the physical layer transmission of audio, video, and data services over cable networks. These cable transmission networks as they apply to Europe, North America, and Japan are detailed in Annex A, B, and C of this standard, respectively.

Xilinx addresses this interest with the J.83 Cable Modulator IP, a flexible, scalable, and cost-effective solution. In this article, we'll discuss the use of Xilinx J.83 cores in the downstream modulator at the head-end (Figure 1), while focusing on the physical layer implementation.

The Xilinx J.83 IP solution provides flexibility to parameterize the modulator; scalability to allow you to select any number of channels on a single FPGA; and ease of use in the System Generator for DSP visual programming environment as the design and delivery mechanism.

This programming interface allows you to work at a suitable level of abstraction from the target hardware platform and use the same model.

System Generator for DSP

The Xilinx System Generator tool suite was employed to implement a majority of the J.83 modulator design. System Generator is a visual dataflow design environment based on The MathWorks Simulink® visual modeling tool set. This programming interface allows you to work at a suitable level of abstraction from the target hardware platform and use the same model – not only for simulation and verification but also for FPGA implementation.

System Generator blocks are bit- and cycle-true behavioral models of FPGA intellectual property components, or library elements. A library-based approach results in design cycle compression in addition to generating area-efficient high-performance circuits. Together with model features such as data-type propagation and the extensive virtual instruments that are part of the Simulink libraries, the environment facilitates rapid design space exploration, together with powerful mechanisms for model debugging.

MATLAB® scripts from The MathWorks programmatically generate custom VHDL and project files based on user-defined parameters.

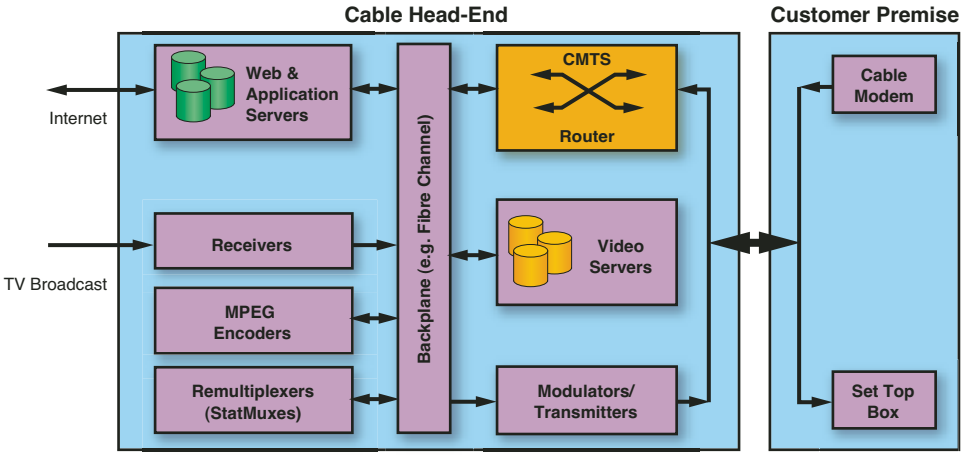


Figure 1 – Cable network (J.83 modulator fits in the cable head-end modulator/transmitter block)

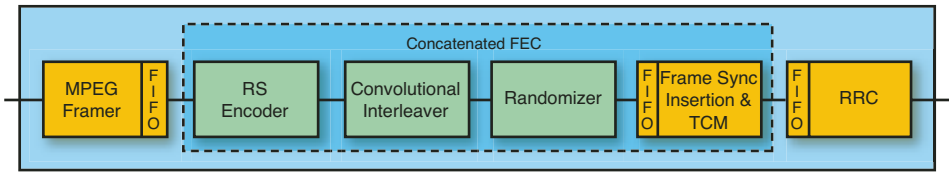


Figure 2 – J.83 Annex B functional block diagram

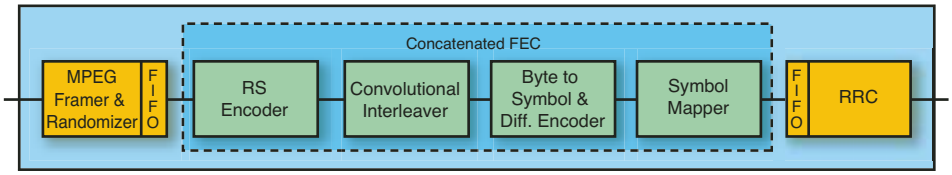


Figure 3 – J.83 Annex A/C functional block diagram

J.83 in System Generator for DSP

The J.83 specification defines the forward error correction (FEC) and baseband modulation with pulse-shaping characteristics. The J.83 Annex B FEC section (Figure 2) uses a concatenated coding technique with four processing layers, comprising an RS encoder, convolutional interleaver, randomizer followed by a frame sync insertion block, and trellis-coded modulation (TCM). The J.83 Annex A and Annex C (Figure 3) have identical FEC processing stages, comprising an RS encoder, convolutional interleaver, and a byte-to-symbol differential encoder, followed by a symbol mapper.

The System Generator Xilinx library, or block set, is abundantly populated with IP that enables rapid design and simulation of such a system. The tokens required to construct the J.83 FEC section – as well as the filter blocks required to construct pulse-shaping filters – are available within the library browser. The underlying circuit of each of these tokens is optimized in area and speed to suit the Xilinx family of devices.

Each of these elements is conveniently customizable to be compatible with the precise specification of the J.83 standard. It is then a simple matter of using these customized library elements to build out the circuit required.

For example, you can obtain the (204,188) RS encoder required for J.83 Annex A/C by using the Xilinx Reed Solomon encoder block, with the Code Specification parameter set to DVB. Similarly, the Xilinx interleaver deinterleaver block is directly used in the design, with the mode set to Interleaver and the Number of Branches and Length of Branches set to 12 and 17, respectively. This results in an exact match to the requirements of the interleaver in the J.83 A/C specification. Using the visual graphic means of design entry in System Generator, these blocks are easily connected to each other and to the control circuitry that is part of the design.

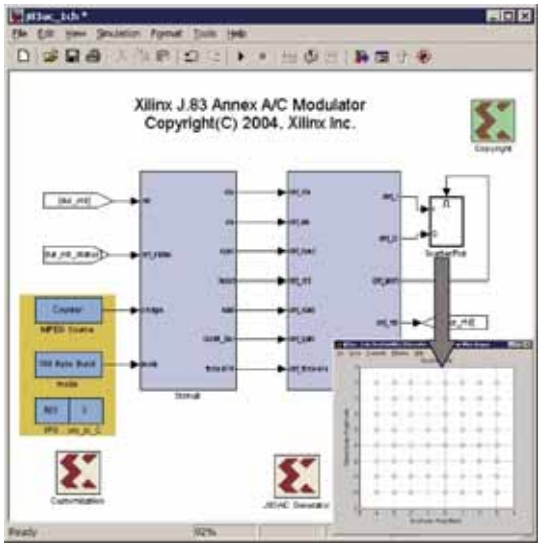


Figure 4 – J.83 Annex A/C modulator with scatter plot

IP Simulation in Simulink

It takes a lot of time to simulate and test the functionality of a complex system. You can use the same J.83 circuit built in System Generator for simulation and verification, as well as the FPGA implementation. Within the same environment, using Simulink for simulation, the design is stimulated with MPEG transport packets and the appropriate QAM, reset, synchronization, and other control inputs.

As shown in Figure 4, this stimulus is shown in the block labeled "Stimuli." The source, inter-packet gap, and burst nature of the MPEG transport packet may be chosen at random at the top level, allowing a test of the full suite of possibilities. Figure 4 also shows a discrete time scatter plot of the output of the baseband section of the modulator.

Simulation of this complex system in an HDL simulator for a meaningful number of clock cycles (such that several frames of data may be processed) imposes a huge penalty in the time taken to complete a simulation. This makes it an impractical choice, but sometimes it is the only option when the design source is in an HDL format.

This simulation time is drastically reduced when simulating the model in Simulink. What might take days to simulate in a gate-level simulator could be accomplished in a matter of hours. This savings in time is highly valuable – not only do you benefit from superior simulation speed in Simulink but you also reap the benefits of a shortened design cycle, allowing for overall rapid IP delivery.

Single and Multi-Channel Designs

The modulator is constructed out of two primary footprints or granularity: a single-channel implementation and a four-channel implementation. A block diagram of the four-channel granularity Annex B and A/C are shown in Figure 5 and Figure 6, respectively.

Each instance of the single-channel footprint provides for exactly one independent channel; the four-channel footprint, however, is optimized to efficiently support four channels at a time, using resource-sharing techniques. You select the granularity, and with that selection, make a trade-off between resource utilization and individual channel control.

The trade-off is essentially in the area (resource) utilization; the optimized four-channel group solution results in a very efficient and compact design requiring fewer FPGA resources. However, it imposes the restriction that the four channels must share the same controls. The single-channel solution imposes no such restriction; the trade-off here is the linearly increasing FPGA resources used, which is directly proportional to the number of channels required.

Multi-channel modulators are automatically constructed through the use of multiple copies (also referred to as groups) of the single- or four-channel implementation. For example, a four-channel modulator may be constructed with four copies of single-channel granularity or a single copy of the optimized 4-channel granularity design. Similarly, a 12-channel modulator may comprise 12 copies of the single-channel granularity design or 3 copies of the optimized 4-channel design.

The ease of use is evident in that the

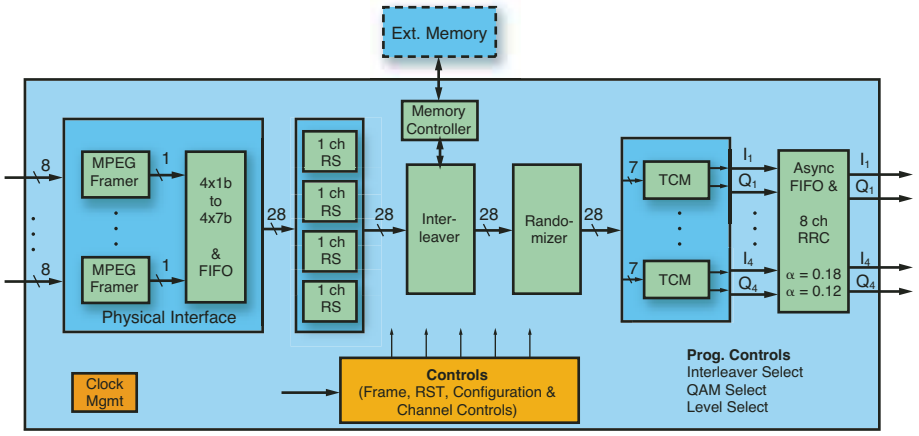


Figure 5 – J.83 Annex B four-channel granularity design

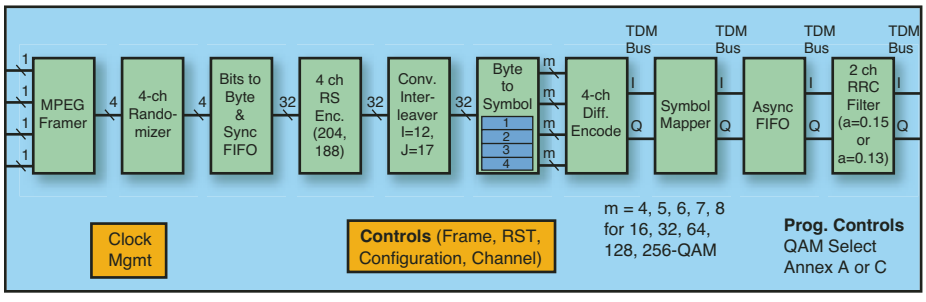


Figure 6 – J.83 Annex A/C four-channel granularity design

only requirement is for you to specify the parameters; the multiple instantiations of the basic footprints and the required connections between them are automatically generated, leaving you with a core design tailored to those exact specifications.

Usage

The Xilinx J.83 modulator implementation is available as a module that plugs into Xilinx System Generator for DSP, or as a netlist that may be directly referenced by another design. The design of the J.83 core in System Generator allows for generation with a simple push button solution.

Through a GUI constructed in the familiar Simulink environment, the core provides you with a convenient means of supplying design specifics such as the granularity desired, the number of channels required, and clock rates, as shown in Figure 7.

Figure 7 – J.83 Annex B generator GUI screenshot

During parameterization and generation, the core is automatically configured to the specifications and deposited into the target directory. Along with the netlist, the core also includes behavioral and timing simulation script files (.do) for Mentor Graphics® ModelSim™ and an ISE Project Navigator project file (.npl). From this point on, you can bring the core into the ISE Project Navigator environment for synthesis, place and route, and bitstream generation.

Resource Sharing

The Xilinx FPGA implementation of the J.83 modulator specification capitalizes on a particular architectural feature to construct efficient multi-channel implementations: the shift register logic 16 (SRL16) primitive, found in Virtex-II™, Virtex-II Pro™, and Spartan-3™ devices. You can think of SRL16 as a series concatenation of 16 flip-flops with a programmable tap point. This unique aspect of Xilinx FPGAs is extremely powerful for building very efficient time-division multiplexed (TDM) hardware that you can use, for example, to process multiple channels of data.

Because they run the design at a faster rate, TDM processing structures save resources. This has been notably exploited during the design of an optimized multi-channel group of modulators. For example, in the design of the optimized four-channel granularity of a group, all channels share a common control structure in the MPEG framer, RS encoder, interleaver, randomizer, and TCM. As the interleaver controls are shared, the data path into and out of the interleaver effectively becomes wider.

Resource Utilization

Using the resource sharing techniques we've described thus far, you can realize significant savings in the implementation of modulators constructed out of optimized four-channel granularity designs compared to the equivalent constructed out of single-channel granularity designs.

Table 1 and Table 2 show a comparison of the resources used in the design of various sizes of J.83 modulators using single- and four-channel granularity footprints. They also show the resources used to implement 4, 8, and 12 channels of J.83 Annex B and J.83 Annex A/C solutions on a Spartan-3 device.

Although Table 1 details the resources on an implementation that does not contain the optional root-raised cosine filter, the details in Table 2 are specific to an implementation that contains the option. Using the 12-channel case as an example, the scales are favorably tipped towards a four-channel granularity implementation of the J.83 Annex B and J.83 Annex A/C, as the savings achieved are significant.

Number of Channels	J.83 Annex B		J.83 Annex A/C	
	Slices/BRAM/External Memory		Slices/BRAM	
	One Channel Granularity	Four Channel Granularity	One Channel Granularity	Four Channel Granularity
4	3372/8/1	1866/2/1	1574/4	1049/3
8	6764/16/2	3644/4/1	3130/8	2088/6
12	10049/24/2	5405/6/1	4683/12	3304/9

Table 1 – Resource utilization comparison between one- and four-channel granularity J.83 Annex A/B/C designs without RRC (Spartan-3 FPGAs)

Number of Channels	J.83 Annex B		J.83 Annex A/C	
	Slices/BRAM/External Memory		Slices/BRAM	
	One Channel Granularity	Four Channel Granularity	One Channel Granularity	Four Channel Granularity
4	8014/20/1	3748/7/1	4829/8	2444/4
8	16024/40/2	7402/14/1	9661/16	4877/8
12	23924/60/2	11057/21/1	14449/24	7483/12

Table 2 – Resource utilization comparison between one- and four-channel granularity J.83 annex A/B/C designs with RRC (Spartan-3 FPGAs)

Design Example Usage

The J.83 modulator design provides control configuration that you can control using a PowerPC™ or the MicroBlaze™ processor in Virtex-II Pro FPGAs. The processor can not only control the (J.83 Annex B) configurations such as QAM, interleaver control word, and interleaver level, but also the reset sequence of the design. It may be shared to control other user logic such as the MAC layer implementation for cable communication at the head end and baseband-to-IF digital upconversion. The functional block diagram in Figure 8 depicts how you can leverage the capabilities of the Virtex-II Pro architecture for the J.83 design.

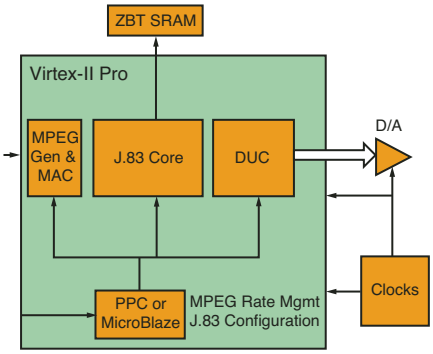


Figure 8 – J.83 single chip system design

Conclusion

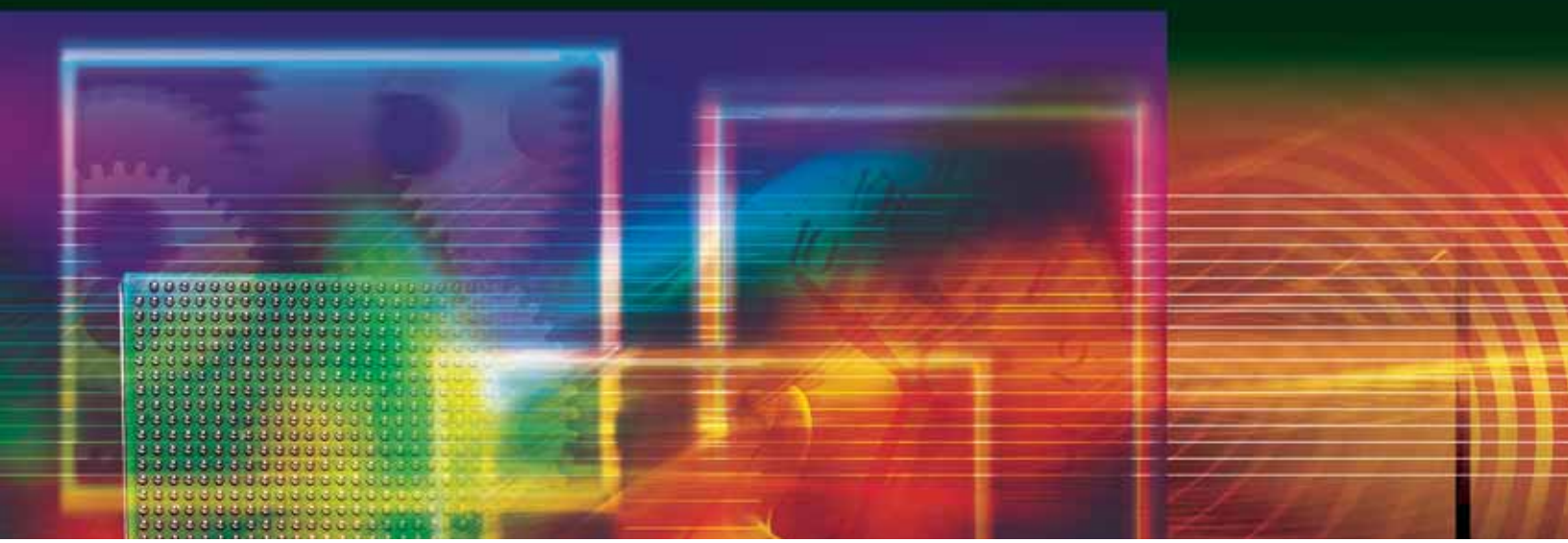
Xilinx System Generator enables the rapid development and simulation of high-performance systems on Xilinx FPGAs. SRL16s allow you to design a 16-channel granularity modulator without using 16 times the resources of a 1-channel granularity modulator or 4 times the resources of a 4-channel granularity modulator.

You can build various standard-compliant modulators for video broadcast for transmission over terrestrial links (DVB-T) via satellite (DVB-S2) or to handheld devices (DVB-H) quickly and efficiently using System Generator for DSP and various library blocks available from Xilinx. SRL16s in Xilinx FPGAs allow efficient time-multiplexed dataflow structures, offering significant resource savings.

For more information about the Xilinx J.83 Modulator IP, visit *www.xilinx.com/ipcenter/j83_mod/*.

Implementing the H.264/AVC Video Coding Standard on FPGAs

Xilinx Virtex FPGAs provide excellent co-, pre-, and post-processing hardware acceleration solutions.



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H.264/AVC is the latest international video coding standard in a series of such standards: H.261, MPEG-1, MPEG-2, H.263, and MPEG-4 visual, or part 2. It was approved by the ITU-T (International Telecommunications Union Telecommunication Standardization Sector) as recommendation H.264 and by ISO/IEC as International Standard 14 496-10 (MPEG-4 part 10) Advanced Video Coding (AVC) in May 2003.

Despite H.264/AVC's promises of improved coding efficiency over existing video coding standards, it still presents tremendous engineering challenges to system architects, DSP engineers, and hardware designers. The H.264/AVC standard brought in the most significant changes and algorithmic discontinuities in the evolution of video coding standards since the introduction of H.261 in 1990.

The algorithmic computational complexity, data locality, and algorithm and data parallelism required to implement the H.264/AVC coding standard often directly influences the overall architectural decision at the system level. In turn, this determines the ultimate cost of developing any commercially viable H.264/AVC system solution in the broadcasting, video editing, teleconferencing, and consumer electronics fields.

Complexity Analysis

To achieve a real-time H.264/AVC standard definition (SD) or high definition (HD) resolution encoding solution, system architects often employ multiple FPGAs and programmable DSPs. To illustrate the enormous computational complexity required, let's explore the typical run-time cycle requirements of the H.264/AVC encoder based on the software model provided by the Joint Video Team (JVT), comprising experts from ITU-T's Video Coding Experts Group (VCEG) and ISO/IEC's Moving Picture Experts Group (MPEG).

Using Intel™ VTune™ software running on an Intel Pentium™ III 1.0 GHz general-purpose CPU with 512 MB of memory, achieving H.264/AVC SD with a main profile encoding solution would require approximately 1,600 BOPS (billions of operations per second).

Table 1 illustrates a typical profile of the H.264/AVC encoder complexity based on the Pentium III general-purpose processor architecture. Notice that in Table 1, motion estimation, macroblock/block processing (including mode decision), and motion compensation modules are the primary candidates for hardware acceleration.

Functional Blocks	% of Run-Time Total Cycles
mv_search.c	67.31 %
block.c	8.19 %
refbuf.c	6.95 %
macroblock.c	3.48 %
rdopt.c	3.37 %
biariencode.c	3.21 %
cabac.c	2.98 %
memcpy.asm*	2.91 %
abs.c*	0.57 %
image.c	0.54 %
rdopt_coding_state.c	0.46 %
loopFilter.c	0.03 %

Table 1 – H.264/AVC encoder complexity profile by files

However, computation complexity alone does not determine if a functional module should be mapped to hardware or remain in software. To evaluate the viability of software and hardware partitioning of the H.264/AVC coding standard implementation on a platform that consists of a mixture of FPGAs, programmable DSPs, or general-purpose host processors, we need to look at a number of architectural issues that influence the overall design decision.

- Data locality. In a synchronous design, the ability to access memory in a particular order and granularity while minimizing the number of clock cycles due to latency, bus contention, alignment, DMA transfer rate, and the types of memory used (such as ZBT memory, SDRAM, and SRAM) is very important. The data locality issue is primarily dictated by the physical interfaces between the data unit and the arithmetic unit (or the processing engine).
- Data parallelism. Most signal processing algorithms operate on data that is highly parallelizable (such as FIR filtering). Single instruction multiple data (SIMD) and vector processors are particularly efficient for data that can be parallelized or made into a vector format (or long data width). FPGA fabric exploits this by providing a large amount of block RAM to support numerous very high aggregate bandwidth requirements. In the new Xilinx Virtex-4™ SX device family, the amount of block RAM matches closely with the number of Xtreme DSP™ slices (SX25 – 128 block RAM, 128 DSP slices; SX35 – 192 block RAM, 192 DSP slices; SX55 – 320 block RAM, 512 DSP slices).
- Signal processing algorithm parallelism. In a typical programmable DSP or a general-purpose processor, signal processing algorithm parallelism is often referred to as instruction level parallelism (ILP). A very long instruction word (VLIW) processor is an example of such a machine that exploits ILP by grouping multiple instructions (ADD, MULT, and BRA) to be executed in a single cycle. A heavily pipelined execution unit in the processor is also an excellent example of hardware that exploits the parallelism. Modern programmable DSPs have adopted this architecture (including the Texas Instruments™ TMS320C64x).

  However, not all algorithms can exploit such parallelism. Recursive algorithms like IIR filtering, variable-length coding (VLC) in MPEG1/2/4, context-adaptive variable length coding (CAVLC), and context-adaptive binary arithmetic coding (CABAC) in H.264/AVC are particularly sub-optimal and inefficient when mapped to these programmable DSPs. This is because data recursion prevents ILP from being used effectively. Instead, dedicated hardware engines can be built efficiently in the FPGA fabric.
- Computational complexity. Programmable DSP is bounded in computational complexity, as measured by the clock rate of the processor. Signal processing algorithms implemented in the FPGA fabric are typically computationally intensive. Some examples of these are the sum of absolute difference (SAD) engine in motion estimation and video scaling.

  By mapping these modules onto the FPGA fabric, the host processor or the programmable DSP has the extra cycles for other algorithms. Furthermore, FPGAs can have multiple clock domains in the fabric, so selective hardware blocks can thus have separate clock speeds based on their computational requirements.
- Theoretic optimality in quality. Any theoretic optimal solution based on the rate-distortion curve can be achieved if and only if the complexity is unbounded. In a programmable DSP or general-purpose processor, the computational complexity is always bounded by the clock cycles available. FPGAs, on the other hand, offer much more flexibility by exploiting data and algorithm parallelism by means of multiple instantiations of the hardware engines, or increased use of block RAM and register banks in the fabric.

  A programmable DSP or general-purpose processor is often limited by the number of instruction issues per cycle, the level of pipeline in the execution unit, or the maximum data width to fully feed the execution units. Video quality is often compromised as a result of the limited cycles available per task in a programmable DSP, whereas hardware resources are fully allocated in FPGA fabric (three-step vs. full-search motion estimation).

Implementing Functional Modules onto FPGAs

Figure 1 shows the overall H.264/AVC macroblock level encoder with major functional blocks and data flows defined. One of the primary successes of the H.264/AVC standard is its ability to predict the values of the content of a picture to be encoded by exploiting the pixel redundancy in different ways and directions not exploited previously in other standards. Unfortunately, when comparing to previous standards, this increases the complexity and memory access bandwidth approximately four-fold.

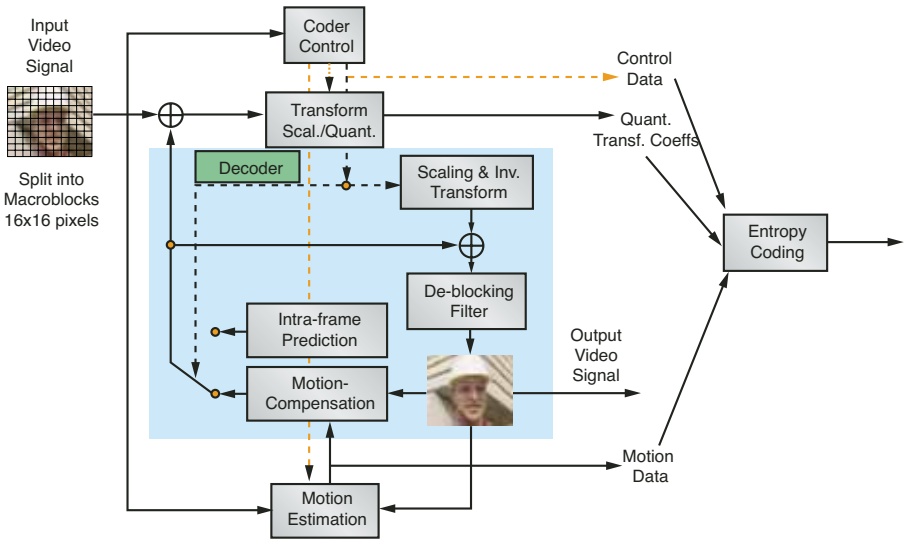


Figure 1 – H.264/AVC macroblock encoder with functional blocks and data flows

Improved Prediction Methods

Let's highlight some of the main features of the H.264/AVC video coding standard design that enable its enhanced coding efficiency, evaluating these functional modules based on the design criteria discussed in the previous section.

- Quarter-pixel-accurate motion compensation. Prior standards use half-pixel motion vector accuracy. The new design improves on this by providing quarter-pixel motion vector accuracy. The prediction values at half-pixel positions are calculated by applying a one-dimensional six-tap FIR filter [1, -5, 20, 20, -5, 1]/32 horizontally and vertically.

  Prediction values at quarter-pixel positions are generated by averaging samples at the full- and half-pixel positions. These sub-sampling interpolation operations can be efficiently implemented in hardware inside the FPGA fabric.

- Variable block-sized motion compensation with small block size. The standard provides more flexibility for the tiling structure in a macroblock size of 16 x 16 pixels. It allows the use of 16 x 16, 16 x 8, 8 x 16, 8 x 8, 8 x 4, 4 x 8, and 4 x 4 sub-macroblock sizes.

  Because of the increasing combinations of tiling geometry with a given 16 x 16 macroblock, to find a rate distortion optimal tiling solution is extremely computationally intensive. This additional feature places an enormous burden on the computational engines used in motion estimation, refinement, and mode decision process.

- In-the-loop adaptive deblocking filtering. The deblocking filter has been successfully applied in H.263+ and MPEG-4 part 2 implementations as a post-processing filter. In H.264/AVC, the deblocking filter is moved inside the motion-compensated loop to filter block edges resulting from the prediction and residual difference coding stages of the decoding process. The filtering is applied on both 4 x 4 block and 16 x 16 macroblock boundaries, in which two pixels on either side of the boundary may be updated using a three-tap filter. The filter coefficients or "strength" are governed by a content-adaptive non-linear filtering scheme.

- Directional spatial prediction for intra coding. In cases where motion estimation cannot be exploited, intra-directional spatial prediction is used to eliminate spatial redundancies. This technique attempts to predict the current block by extrapolating the neighboring pixels from adjacent blocks in a defined set of directions. The difference between the predicted block and the actual block is then coded.

  This approach is particularly useful in flat backgrounds where spatial redundancies exist. There are a total of nine prediction directions for Intra_4x4 prediction, and four prediction directions for Intra_16x16 prediction. Note that the data causality imposes quick memory access to the neighboring 13 pixel values to the above and left of the current block in the case of Intra_4x4. For the Intra_16x16, 16 neighboring pixels on each side are used to predict a 16 x 16 block.

- Multiple reference picture motion compensation. The H.264/AVC standard offers the option for multiple reference frames in the inter-frame coding. Unless the number of the referenced pictures is one, the index at which the reference picture is located inside the multi-picture buffer has to be signaled. The multi-picture buffer size determines the memory usage in the encoder and decoder. These reference frame buffers must be addressed correspondingly during the motion estimation and compensation stages in the encoder.

- Weighted prediction. The JVT recognizes that in encoding certain video scenes that involve fades, having a weighted motion-compensated prediction dramatically improves the coding efficiency.

Improved Coding Efficiency

In addition to improved prediction methods, other parts of the standard design were also enhanced for improved coding efficiency. Two additional features are most likely to impact the overall system architecture based on our design criteria for software and hardware partitioning:

- Small block size, hierarchical, exact-match inverse, and short word-length transform. The H.264/AVC, like other standards, also applies transform coding to the motion-compensated prediction

residual. But, unlike previous standards that use an 8 x 8 discrete cosine transform (DCT), this transform is applied to 4 x 4 blocks, and is exactly invertible in a 16-bit integer format. The small block helps reduce blocking and ringing artifacts, while the precise integer specification eliminates any mismatch

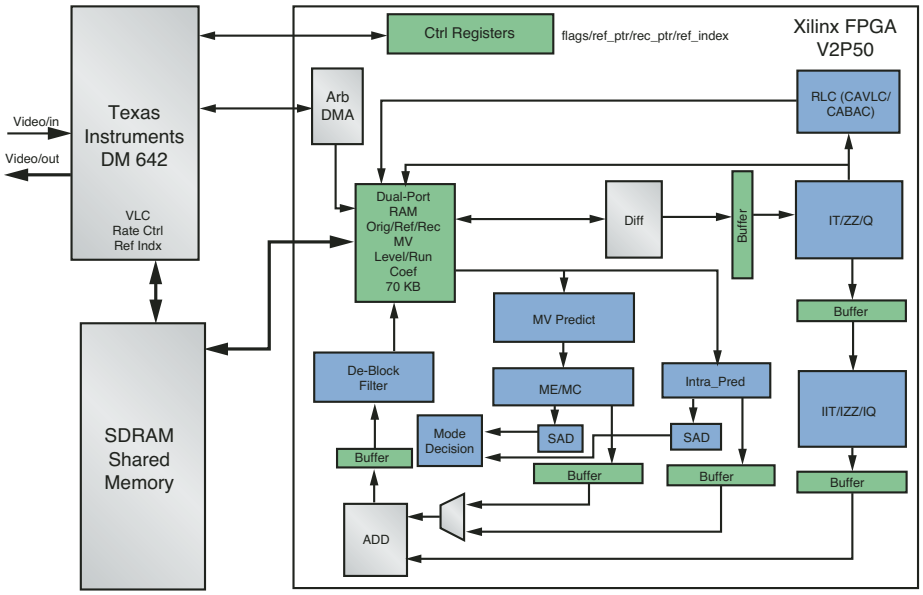


Figure 2 – Typical H.264/AVC hardware/software functional block partition
Diagram courtesy of W&W Communications

issues between the encoder and decoder in the inverse transform.

Furthermore, an additional transform based on the Hadamard matrix is also used to exploit the redundancy of 16 DC coefficients of the already transformed blocks. Compared to a DCT, all applied integer transforms have only integer numbers ranging from -2 to 2 in the transform matrix. This allows you to compute the transform and the inverse transform in 16-bit arithmetic using only low-complexity shifters and adders.

- Arithmetic and context-adaptive entropy coding. Two methods of entropy coding exist: a low-complexity technique based on the use of context-adaptively switched sets of variable length codes (CAVLC) and the computationally more demanding algorithm of context-based adaptive binary arithmetic coding (CABAC). CAVLC is the baseline entropy coding method of H.264/AVC. Its basic coding tool consists of a single VLC of structured Exp-Golomb codes, which by means of individually customized mappings are applied to all syntax elements except those related to the quantized transform coefficients. For the CABAC, a more sophisticated coding scheme is applied. The transform coefficients are first mapped into a 1-D array based on a predefined scan pattern. After quantization, a block contains only a few significant non-zero coefficients.

  Based on this statistical behavior, five data elements are used to convey information of the quantized transform coefficients for a luminance 4 x 4 block. The efficiency of entropy coding can be improved further if using CABAC.

  There are two parts in CABAC. The arithmetic coding core engine and its associated probability estimation are specified as multiplication-free low-complexity methods using only shifts and table look-ups. The use of adaptive codes allows it to adapt to non-stationary symbol statistics. By using context modeling based on switching between conditional probability models that are estimated from previous coded syntax elements, CABAC can achieve a reduction in bit rate between 5-15% compared to CAVLC.

Figure 2 depicts a typical system-level functional block partition of the H.264/AVC SD video codec. The solution is implemented based on the Spectrum Digital EVM DM642 evaluation module for the Texas Instruments TMS320DM642 DSP, together with the Xilinx XEVM642-2VP20 Virtex-II Pro™ or XEVM642-4VSX25 Virtex-4™ daughtercard.

Conclusion

When used in an optimized fashion, the coding tools of the H.264/AVC standard increase coding efficiency by about 50% compared to previous video coding standards (like MPEG-4 part 2 and MPEG-2) for a wide range of bit rates and resolutions. Currently, it is the most likely successor to the widely used MPEG-2. However, the algorithm is quite complex, at a resolution greater than source input format (SIF).

The DVD-Forum, with its HD-DVD initiatives, has selected H.264/AVC together with WMV-9 and MPEG-2 as the standard video coding formats. The European DVB consortium has also selected H.264/AVC as the next format after MPEG-2. These announcements, plus endorsements from Hollywood studios, content distributors, and broadcast infrastructures, have further validated the importance of the H.264/AVC video coding standard for the next few years.

For more comprehensive studies and technical details of the H.264/AVC video coding standard, please see the References.

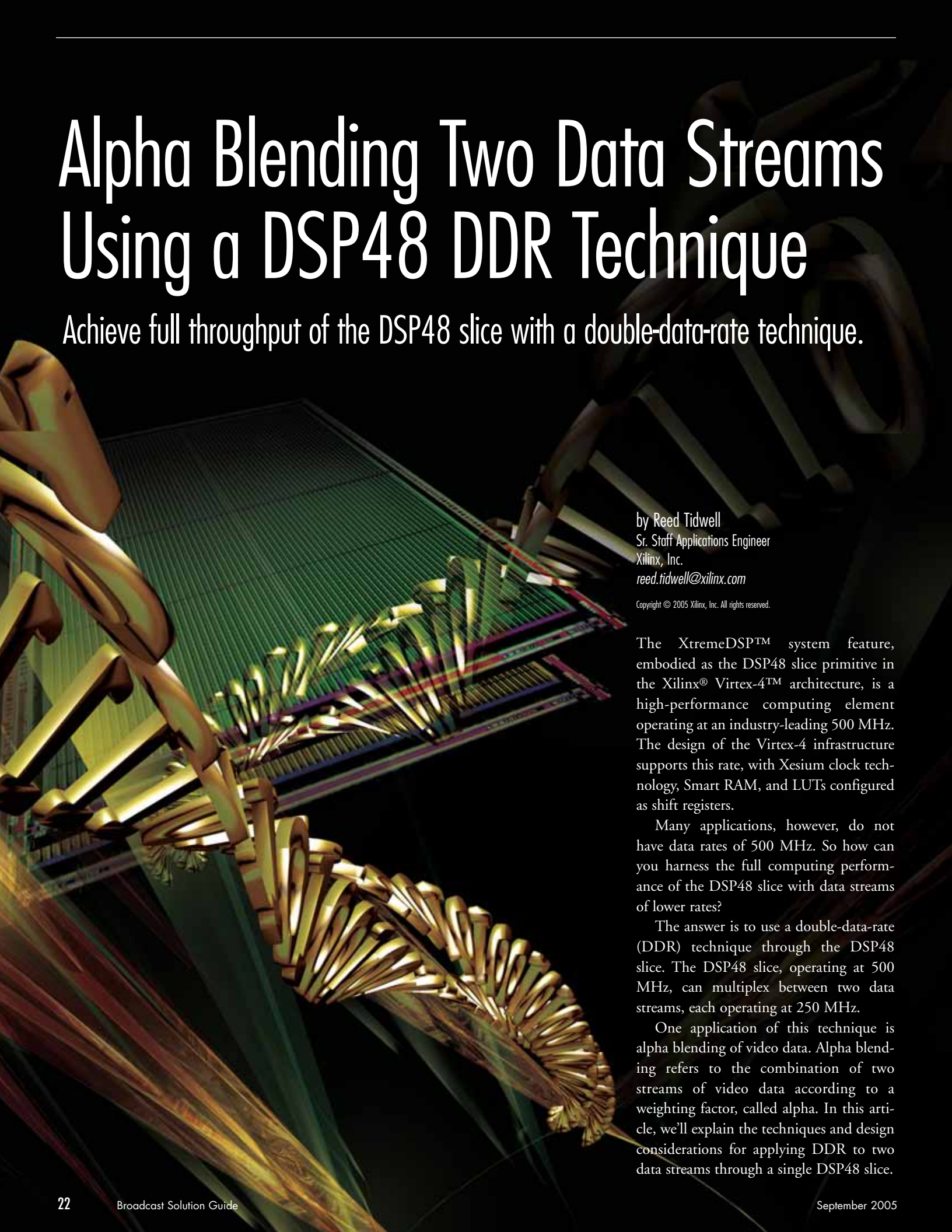
References

"Draft ITU-TU Recommendation and Final Draft International Standard of Joint Video Specification (ITU-T Rec. H.264/ISO/IEC 14 496-10 AVC)," in Joint Video Team (JVT) of ISO/IEC MPEG and ITU-T VCEG, JVT-G050, 2003.

A. Luthra, G.J. Sullivan, and T. Wiegand. July 2003. "Special Issue on The H.264/AVC Video Coding Standard." *IEEE Trans. Circuits System Video Technology* 13(7): 557-725.

Alpha Blending Two Data Streams Using a DSP48 DDR Technique

Achieve full throughput of the DSP48 slice with a double-data-rate technique.



by Reed Tidwell
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The XtremeDSP™ system feature, embodied as the DSP48 slice primitive in the Xilinx® Virtex-4™ architecture, is a high-performance computing element operating at an industry-leading 500 MHz. The design of the Virtex-4 infrastructure supports this rate, with Xesium clock technology, Smart RAM, and LUTs configured as shift registers.

Many applications, however, do not have data rates of 500 MHz. So how can you harness the full computing performance of the DSP48 slice with data streams of lower rates?

The answer is to use a double-data-rate (DDR) technique through the DSP48 slice. The DSP48 slice, operating at 500 MHz, can multiplex between two data streams, each operating at 250 MHz.

One application of this technique is alpha blending of video data. Alpha blending refers to the combination of two streams of video data according to a weighting factor, called alpha. In this article, we'll explain the techniques and design considerations for applying DDR to two data streams through a single DSP48 slice.

All Virtex-4 devices have DSP48 slices, although the SX family contains the largest number (an industry-high 512) and the highest concentration of DSP48 slices to logic elements, making it ideal for math-intensive applications …

Virtex-4 DSP48

The DSP system elements of Virtex-4 FPGAs are dedicated, diffused silicon with dedicated, high-speed routing. Each is configurable as an 18 x 18-bit multiplier; a multiplier followed by a 48-bit accumulator (MACC); or a multiplier followed by an adder/subtracter. Built-in pipeline stages provide enhanced performance for 500 MHz throughput – 35% higher than for competing technologies.

All Virtex-4 devices have DSP48 slices, although the SX family contains the largest number (an industry-high 512) and the highest concentration of DSP48 slices to logic elements, making it ideal for math-intensive applications such as image processing.

A triple-oxide 90 nm process makes the DSP48 slice very power-efficient. Architectural features, including built-in pipeline registers, accumulator, and cascade logic nearly eliminate the use of general-purpose routing and logic resources for DSP functions, and further reduce power. This slashes DSP power consumption to a fraction when compared to Virtex-II Pro™ devices.

DDR with Two Data Streams

DDR, in this context, refers to multiplexing two input data streams into one stream at twice the rate, interleaving (in time) the data from each stream (Figure 1). Figure 1 also shows the reverse operation, creating two parallel resultant streams after processing.

You can drive the DSP48 slice inputs at the fast 500 MHz clock rate from CLB flip-flops; CLB LUTs configured as shift registers (SRL16); or directly from block RAM. Block RAM, configured as a FIFO using the built-in FIFO support, also supports the 500 MHz clock rate.

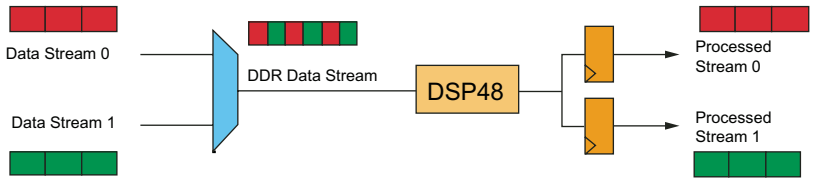

Figure 1 – DSP48 DDR

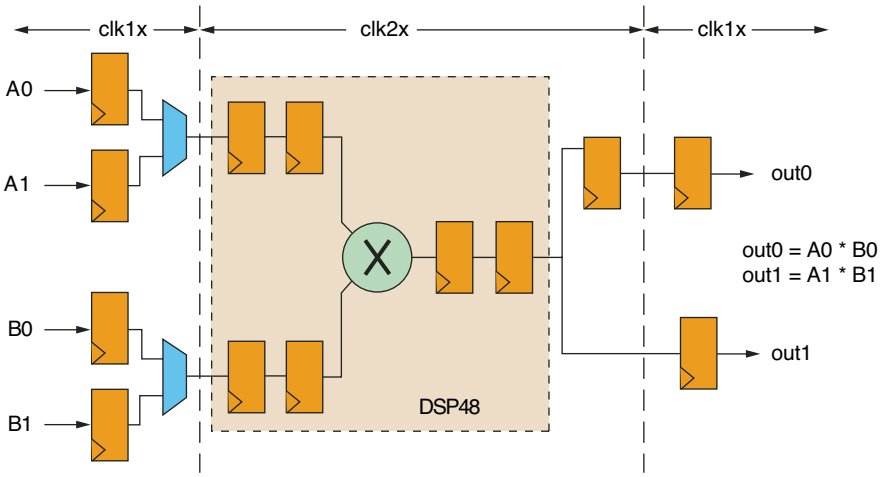

Figure 2 – Two-stream multiply through DSP48 slice

Design Considerations

Dealing with data at 500 MHz requires great care; you should observe strict pipelining with registers on the outputs of each math or logic stage. The DSP48 slice provides optional pipeline registers on the input ports, on the multiplier output, and on the output port from the adder/subtracter/accumulator. Block RAM also has an optional output register for efficient pipelining when interfaced to the DSP48 slice.

Where you are using CLBs, place only minimal levels of logic between registers to provide maximum speed. For DDR operation, only a 2:1 mux (a single LUT level) is required between pipeline stages. Whether you are interfacing to the DSP48 slice with memory or CLBs, placing connected 500 MHz elements in close proximity minimizes connection lengths in the general routing matrix.

DDR requires the DSP48 slice to operate at double the frequency of the input data streams. You can use a DCM to provide a phase-aligned double-frequency clock using the CLK 2X output.

Another aspect of inserting DDR data through a section of pipeline is ensuring that data passes cleanly between clock domains. This may require adding extra registers clocked with the double-frequency clock at the output of the double-pumped section, to synchronize the data with the original clock. The rule of thumb is that in order to insert a double-pumped section cleanly into a single-pumped pipeline, there must be an even number of register delays in the double-pumped section.

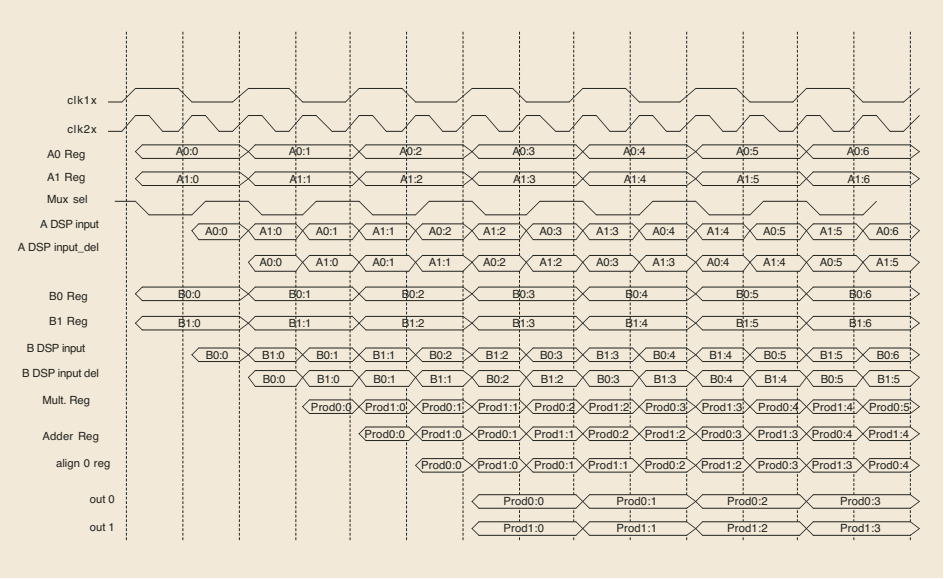

Figure 3 – Timing of two-stream multiply

Implementation

Several configuration options exist for implementing DDR functionality. Figure 2 shows a straightforward implementation.

In Figure 2, stream 0 consists of A0 and B0 inputs. We multiply them together and output as out0. Likewise, stream 1 consists of inputs A1 and B1 multiplied together and output as out1. There are two clock domains: the clk1x domain, at the nominal data stream frequency, and the clk2x domain, at twice the nominal frequency.

Figure 2 shows two registers after the multiplier. The second is the accumulation register, even though we do not use accumulation in this configuration. The register, however, is still required to achieve the full, pipelined performance. We use two sets of registers on the inputs of the DSP to make the total delay through the DSP48 slice an even number (four) for easier alignment of the output data with clk1x. These registers are "free" because they are built into the DSP48 slice, and using them reduces the need for alignment registers external to the DSP48 slice. The extra pipeline register on out0 compensates for taking stream 0 into the DSP one clk2x cycle before stream 1. As seen from the timing diagram in Figure 3, this is required to realign the stream 0 data back into the clk1x domain.

Note that the input mux select, mux_sel, is essentially the inverse of clk1x. It is important, however, to generate this signal from a register based on clk2x (rather than deriving it from clk1x) to avoid hold-time violations on the receiving registers.

At the transitions between clock domains, the data have only one clk2x period to set up. This is the reason to have no logical operations between registers in the two domains. The placement of the first registers in the clk1x domain is more critical than other registers in the same domain.

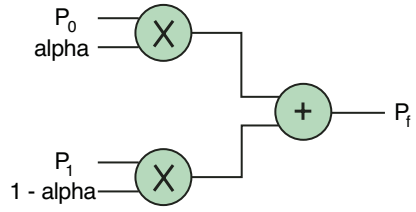

Figure 4 – Alpha blend formula in graphical terms

Alpha Blending

Alpha blending of video streams is a method of blending two images into a single combined image, such as fading between two images, overlaying anti-aliased or semi-transparent graphics over an image, or making a transition band between two images on a split-screen or wipe. Alpha is a weighting factor defining the percentage of each image in the combined output picture. For two input pixels

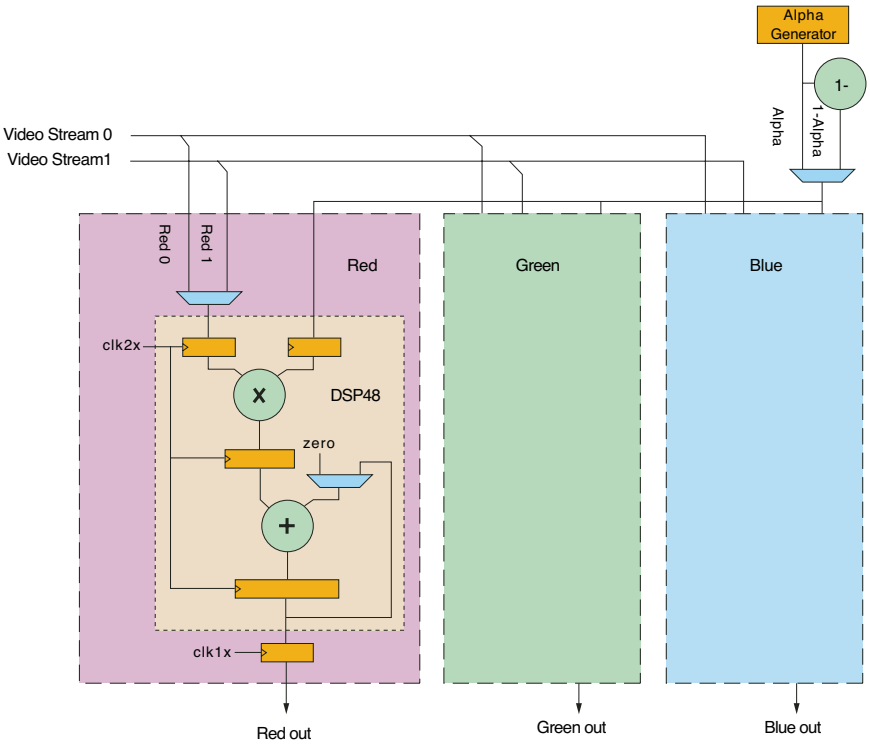

Figure 5 – Alpha blend on three-component video

You can efficiently use the high-performance of Virtex-4 devices with DSP48 slices by processing multiple data streams in a time-multiplexed fashion.

(P0, P1, and a blend factor, α, where 0 <=α < =1.0), the output pixel Pf will be:

$P_f = \alpha P_0 + (1-\alpha)P_1$ (see Figure 4)

This operation is performed separately for each component: red, green, and blue.

A pixel rate of 250 MHz or less is sufficient for all standard and high-definition video rates, and common Video Electronics Standards Association (VESA) standards as high as 1600 x 1200 at 85 Hz. Therefore, one DSP48 slice can perform the multiply and add on one component, and a set of three slices can alpha blend the three components from each of two video streams, as shown in Figure 5. The operations must be performed identically and in parallel on each of the three components.

There are several ways to implement alpha blending depending on the nature of the video streams and how alpha is generated. Figure 6 shows a basic implementation with two video streams alternating as one multiplier input. The other multiplier input alternates between alpha and 1- alpha.

The operating mode of the adder alternates between add zero (pass through) mode and add output (accumulate) mode. The DSP48 slice output register contains the result of the Video0 * alpha multiply during one clock cycle, and the final result (Video1 * (1 – alpha) + Video0 * alpha) on the alternate clock. Figure 7 shows the timing for this configuration.

The align registers on the inputs of the DSP are used to make the total delay through the DSP48 slice an even number (four), as explained in the previous example. The final output register for blend loads new data to every other DSP clock to register the blend results at the original pixel rate.

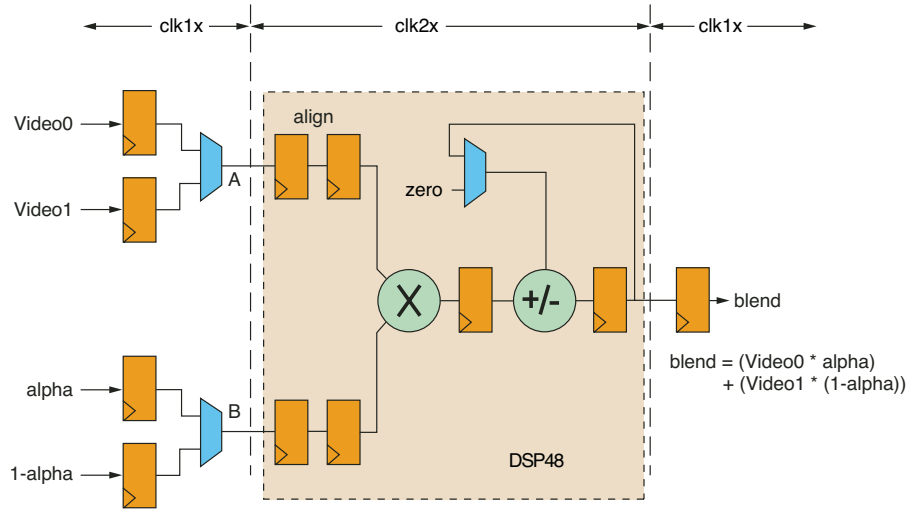

Figure 6 – Alpha blend implementation (one component)

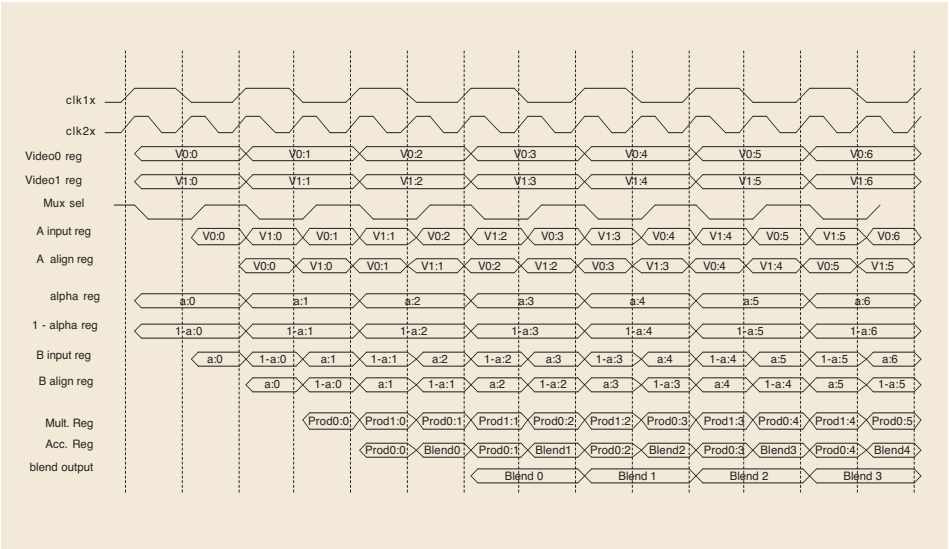

Figure 7 – Alpha blend timing

Conclusion

You can efficiently use the high-performance of Virtex-4 devices with DSP48 slices by processing multiple data streams in a time-multiplexed fashion. With careful design, a single DSP48 can perform multiply operations on two independent data streams, operating at 250 MHz each.

Alpha blending of video streams, as outlined in this article, is one example of processing two data streams through a single DSP48 slice. This capability complements the DSP features of Virtex-4 FPGAs – including built-in pipelining and cascading, integrated 48-bit accumulator, and an abundance of DSP48 slices in the SX family – to make Virtex-4 devices the ideal DSP platform.

For details about the DSP48 slice, refer to the "Virtex-4 FPGA Handbook," Chapter 10, or the "XtremeDSP Design Considerations User Guide" at *www.xilinx.com/bvdocs/userguides/ug073.pdf.*

Designing with the Virtex-4 Embedded Tri-Mode Ethernet MAC

Integrate the versatile Virtex-4 10/100/1000 Ethernet MAC into your next programmable SoC design.

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Ethernet is the predominant wired connectivity standard. The range of standard products for Ethernet is large, and it just got bigger with the introduction of the Xilinx® Virtex-4™ FX device family. Combining embedded Ethernet connectivity with the unique flexibility of the Virtex-4 feature set, Xilinx has created a compelling single-chip platform for solutions not possible with existing off-the-shelf products.

The Virtex-4 FX device family contains paired embedded Ethernet media access controllers (MAC) that are independently configurable to meet all common Ethernet system connectivity needs. Each Virtex-4 FX device contains either two or four MAC, implemented using Xilinx IP immersion technology, as shown in Figure 1.

Using standard Xilinx design products, you now have the unprecedented capability to create a huge range of customized packet processing and network end-point products for 10/100/1000 Mbps Ethernet.

An external physical layer device (PHY) is required for the MAC to connect to a network. The Virtex-4 FX device directly supports all standard serial and parallel PHY interfaces for both copper and optical Ethernet connections. In addition, Virtex-4 embedded RocketIO multi-gigabit transceivers can be used to drive Ethernet directly across PCB traces, such as serial backplanes, for in-system connectivity. PHY connections can be routed to any user pin or RocketIO block in the device.

In this article, we'll review the feature set of the embedded Ethernet MAC blocks in Virtex-4 FX devices, and offer some pointers on how you can start right away using them with standard Xilinx design tools, LogiCORE™ IP, and development boards.

Feature Set

The Virtex-4 Ethernet MAC addresses all common configuration requirements for embedded Ethernet connectivity, and is fully compliant to the IEEE802.3-2002

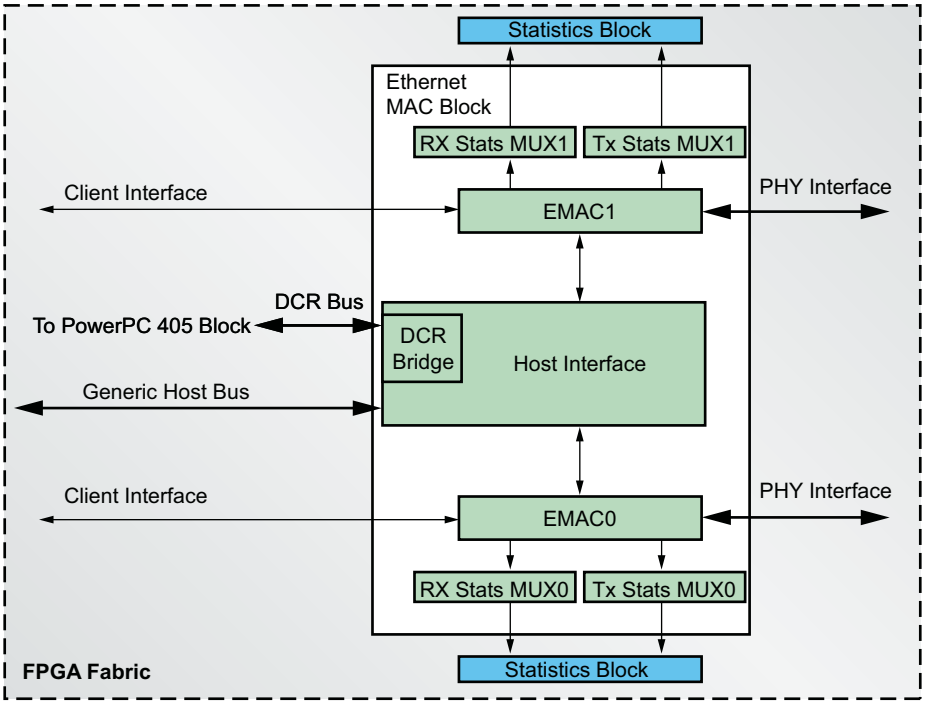

Figure 1 – Embedded Virtex-4 Ethernet MAC Block, with interfaces to FPGA resources

specification. It will allow you to build Ethernet systems that support VLAN, jumbo frames, and end-to-end flow control.

Built-in hardware address filtering reduces the burden on software of processing unneeded frames. You can independently configure each MAC for multiple rates and topologies:

- 10 Mbps or 100 Mbps full- and half-duplex
- 10/100 Mbps full- and half-duplex
- 1000 Mbps full-duplex
- 10/100/1000 Mbps full-duplex

When used in multi-rate modes, auto-negotiation support is provided.

Connecting the MAC to external PHY and optical modules is supported through the PHY interface to the FPGA fabric. This provides flexible use models for the MAC, allowing, for example, attachment to a shared processor bus or to custom packet processing hardware.

Controlling the MAC in your system is performed through the host interface, which provides flexible software access to the internal registers. Each MAC pair shares a common host interface, which can be directly accessed by the embedded PowerPC™ 405 device control register (DCR) bus, or from the FPGA fabric.

Let's describe each of these interfaces in more detail.

PHY Interfaces

Your application will require connection to a particular medium – copper, fiber optics, or one of your own invention. The PHY interface provides many options to meet your requirements.

All common interfaces to external media are directly supported in the PHY interface. As the PHY interface is routed to the outside world through FPGA fabric, creating "bump-in-the-wire" solutions in FPGA fabric is straightforward.

PHY interfaces fall into two categories: one using SelectIO™ resources and another using RocketIO serial transceivers.

The first category is typically used to connect to a discrete external PHY:

- Media independent interface (MII) for 10/100 Mbps
- Gigabit MII (GMII), and reduced GMII (RGMII) for 10/100/1000 Mbps

The second category will also connect directly to a discrete external PHY, and is commonly used to connect to small form-factor pluggable (SFP) modules for both optical and copper connectivity:

- Serial GMII (SGMII) for 10/100/1000 Mbps
- 1000BaseX for 1000 Mbps

These interface options have 9-bit signaling that connect to the RocketIO. Embedded state machines in the MAC provide University of New Hampshire-certified operation for link initialization using these options.

A MII management (MIIM) interface is also included, which allows your software to access external PHY registers through this standard IEEE interface. The registers are accessed via the address map in the host interface.

Host Interface

For your software to control the MAC, a host interface provides access to the internal registers. A dedicated DCR bus connects the embedded PowerPC directly to the host interface, requiring no additional FPGA resources. Alternatively, the host interface can also be accessed directly from the fabric, providing a flexible solution for porting legacy driver software. Each pair of MAC shares a single host interface.

The registers accessed through the host interface are used by driver software to initialize and control the MAC during operation. All register values may be preset at power-on from the FPGA fabric. This allows the MAC to be used by applications that do not include a processor and software. The registers provide access to the following settings:

- Independent receiver settings for reset and enable, pause frame address, jumbo and VLAN frame enables, half/full duplex, and passing frame check sequence (FCS) to the client
- Independent transmitter settings for reset and enable, inter-frame gap (IFG) adjustment, jumbo and VLAN frame enables, half/full duplex, and FCS from client

- Independent flow control enables for receiver and transmitter
- RGMII/SGMII status, and speed for fixed and negotiated settings
- Management interface enable and clock rate
- Receive-side address filter access – unicast and multi-cast address entries

The address filter provides a single unicast and as many as four multi-cast Ethernet addresses that are used to match against the destination address of incoming frames. You can set the filter to optionally discard incoming frames that do not match the stored addresses or to simply flag when a match occurs, allowing you to make routing decisions for received frames at hardware speed rather than in software.

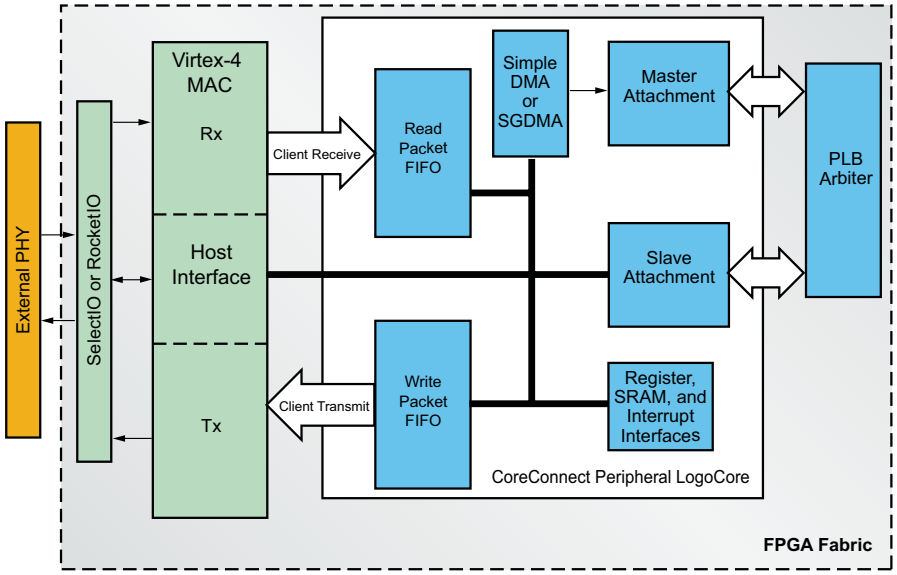

Figure 2 – Embedded MAC connected to embedded PowerPC as a PLB peripheral, with the addition of Xilinx CoreConnect LogiCORE IP

Client Interface

Ethernet frames are passed between the MAC and your design across the client interface, which is divided into receive and transmit sides.

Receiver Side Client Interface

On the receive interface, frame errors and unmatched frames are signaled to the user logic. When flow control is enabled, any valid pause frames received will be flagged as invalid.

Transmitter Side Client Interface

The transmit interface will indicate collisions on half-duplex connections, and will corrupt a truncated frame in the case of FIFO starvation in the middle of a frame. When flow control is enabled, the transmitter interface will automatically assert back pressure on the client when a pause request frame is received from the remote host.

Flow Control and Statistics Vectors

A separate flow control interface allows the client to make pause requests to the far end, allowing the pause interval to be set for each individual request. Separate interfaces provide separate statistics vectors for the receiver and transmitter portions of the MAC. The IEEE-defined statistics are updated on a per-frame basis, and can be accumulated using circuitry in the FPGA fabric.

Over-Speed Operation

This feature allows you to clock the MAC at higher rates than allowed by the standard. The double-width interface on the client side means that your design can process frames at the same system frequency as normal operation, but at twice the data width, providing up to 2 Gbps in each direction.

Virtex-4 Ethernet MAC Use Models

The features described previously provide the Virtex-4 Ethernet MAC with multiple use models. Some examples of these are given here, but this should not be considered a complete list.

- Attach the MAC to CoreConnect PLB or OPB peripheral interface in FPGA fabric to embedded PowerPC or MicroBlaze™ processors, as in Figure 2.
- Create a custom interface to packet processing hardware implemented in FPGA fabric, such as protocol offload, DMA engines, embedded FIFO, and embedded block RAM. Figure 3 shows an example scheme for a Transmission Control Protocol (TCP) offload engine (TOE), and/or Remote Direct Memory Access (RDMA), as covered by the iWARP protocols from the RDMA Consortium.
- Directly connect multiple MAC blocks to Virtex-4 embedded FIFO and external QDR and DDR memory for classification, policing, and switching applications, see Figure 3.
- Provide independent packet monitoring and statistics collection, using custom hardware in FPGA fabric that connects directly to the statistics interface of the MAC blocks.

Any of these use models may be connected to external PHY in multiple system topologies:

- Optical gigabit Ethernet connectivity – connect directly to external optical modules through the Virtex-4 RocketIO transceiver for 1000BaseX operation (Figure 4)
- 10/100 Ethernet connected to external copper PHY through RMII interface implemented between the MII PHY interface and SelectIO pins
- 10/100/1000 tri-mode Ethernet to external PHY or SFP module through SGMII connection to RocketIO transceiver, utilizing a RocketIO block

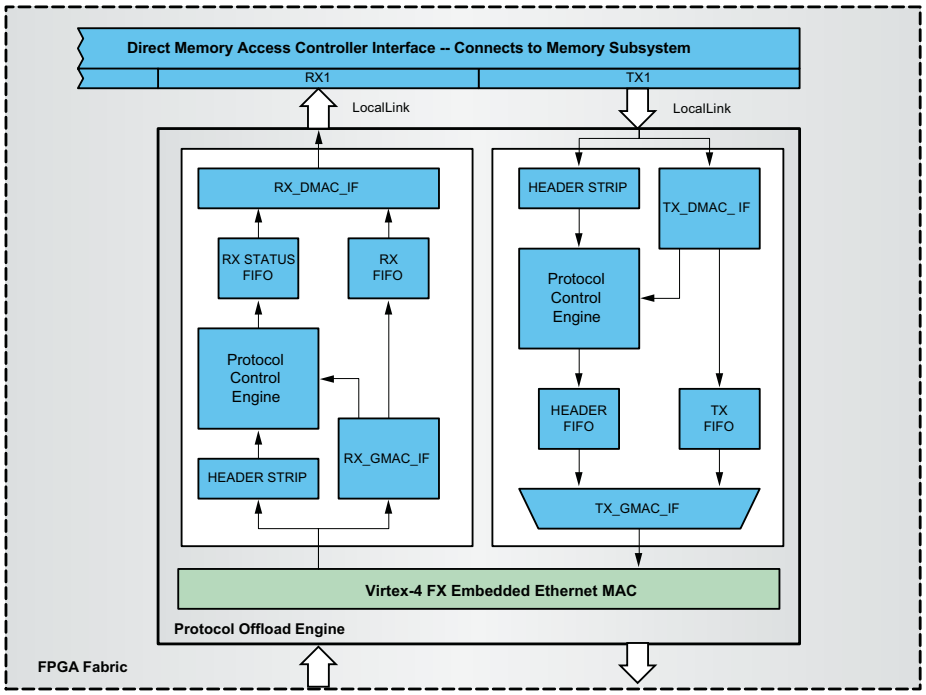

Figure 3 – Packet-processing end-point in Virtex-4 FPGAs using embedded MAC with additional logic for checksum offload, TCP segmentation offload (TSO), network address translation, and other standard or custom applications

Tools, IP, and Development Boards

Xilinx provides support for the MAC with tools, LogiCORE IP, reference designs, and Virtex-4 development boards.

Virtex-4 Embedded EMAC Wrappers

Available from the Xilinx CORE Generator™ tool, you can automatically generate HDL wrappers for the MAC instantiations in your design and completely configure the MAC through the GUI. A low-level software driver for the embedded PowerPC to access the MAC across the dedicated DCR interface will also be automatically generated.

Embedded Developers Kit (EDK)

The EDK tool enables you to build a complete processor subsystem around the MAC. The tool includes standard Xilinx LogiCORE IP to connect the MAC as a CoreConnect peripheral, and will automatically generate a software driver.

Xilinx Ethernet LogiCORE IP and Reference Designs

Much of the legacy Virtex-II Pro™ Ethernet collateral will be reusable with the Virtex-4 MAC.

Reference designs are available that demonstrate useful techniques for optimizing your Ethernet system designs. The LocalLink LLTEMAC checksum offload peripheral, available with the Gigabit System Reference Design (XAPP536) demonstrates how to accelerate the TCP performance of your network endpoint.

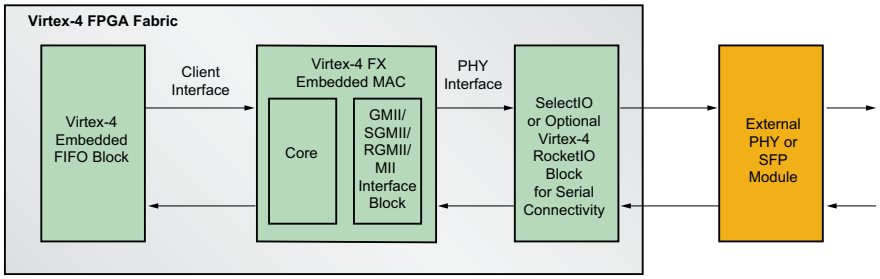

Figure 4 – Multiple Gigabit Ethernet MAC in a switch/router configuration; Virtex-4 embedded FIFO blocks provide intermediate packet storage in the fabric.

Development Boards

Xilinx provides a family of development boards for immediate prototyping of your system design. These include:

- The ML403, a low-cost development platform featuring the Virtex-4 FX12 device, includes a tri-speed Ethernet PHY for Ethernet copper connectivity
- The ML405 development board provides a superset of the ML403, with additional serial connectivity options enabled by the Virtex-4 FX20 RocketIO transceivers

All Xilinx and partner-developed boards are available from the "Xilinx on Board" section of the Xilinx website.

Conclusion

The embedded tri-mode Ethernet MAC in Virtex-4 FX devices provides unparalleled flexibility for today's Ethernet systems designers; spanning:

- Hub, switch, and router systems topologies
- Tightly coupled network processing functionality utilizing embedded processors and custom logic
- Embedded processing shared bus subsystems
- Direct low latency connectivity to packet storage
- Cost effective interoperability with future, current, and legacy physical layer standards

In short, the Virtex-4 FX family enables you to customize your solution for the Ethernet topology and feature set that your application requires. To find out more, please follow the Virtex-4 links on the Xilinx website, *www.xilinx.com/virtex4/*.

The Virtex-4 Power Play

The latest Xilinx FPGA offers revolutionary power innovations.

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Device power consumption is a primary issue in the semiconductor industry – as process technologies get smaller and faster, they normally consume more power, putting power concerns and performance at odds. The new Virtex-4™ FPGA family from Xilinx® employs innovative architectural features and clever IC design techniques that dramatically reduce power consumption, without compromising performance. This bucks expected trends normally associated with the reduced feature sizes of 90 nm process technology.

In this article, we'll explore how Xilinx IC designers achieved remarkable power efficiency in the high-performance Virtex-4 FPGA.

Components of Power Consumption

There are two main components to power consumption: static and dynamic. Static or quiescent power is mainly dominated by transistor leakage current. When this current is listed in data sheets, it is listed as I_{CCINTQ} and is the current drawn through the V_{CCINT} supply powering the FPGA core.

Dynamic or active power has components from both the switching power of the core of the FPGA and the I/O being switched. The dynamic power consumption is determined by the node capacitance, supply voltage, and switching frequency and governed by the basic formula $P=CV^2f$.

Both static and dynamic power have been significantly reduced in Virtex-4 devices, even when compared to Virtex-II Pro™ devices.

Dramatic Power Reduction

The Virtex-4 product family has reduced power consumption in several key areas. The power-per-CLB has been cut in half, with static power reduced by 40% and dynamic power reduced by 50% when compared to the 130 nm Virtex-II Pro FPGA and other 90 nm FPGAs. Furthermore, certain hard-logic silicon functions in the Virtex-4 FPGA reduce power consumption by 80-95%, a whopping factor when compared to the same functions implemented in configurable logic blocks and programmable interconnect routing.

Additionally, comprehensive power planning tools are available to help you get an idea, up front, of power consumption for your Xilinx FPGA under its operating conditions.

Reduced Power Consumption Benefits

Reduced power consumption benefits cut across a few areas of product design in reduced thermal concerns as well as eased power supply design (see Figure 1).

- Reduced thermal concerns – When you reduce power consumption in a device or system, you use smaller heat sinks, or no heat sinks at all in some cases. You also have simpler thermal system design from the point of view of reducing airflows and fan size needs.
- Easier power supply design – You can also use smaller supply circuitry and reduce the number of components in the power supply. Using less PCB space allows you to reduce the cost of the power system. Plus, by not having your device consume as much power, you can achieve higher reliability by lowering the temperature of the FPGA die.

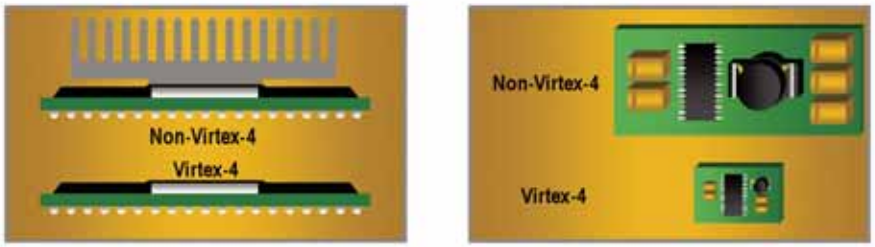


Figure 1 – Virtex-4 devices reduce thermal concerns and simplify power supply design.

Static Power Trends in 90 nm Technology

The reduction in transistor size in 90 nm technology has several effects on power consumption. The biggest potential problem is in the area of static power.

Scaling Trends for Static Power

As we mentioned earlier, static power is dominated by transistor leakage current. Unfortunately, channel leakage increases as transistor size decreases. This is especially true for low V_T transistors where V_T refers to voltage threshold between the gate and drain.

Low V_T transistors are the fastest transistors – the ones with the shortest turn-on and propagation delay – that IC designers use inside the FPGA when the highest speed performance is needed. Regular V_T transistors are also used when less performance is acceptable, but this only helps so much with leakage.

Figure 2 shows that leakage goes up dramatically when moving from 130 nm to 90 nm technology. The Virtex-II Pro device uses 130 nm process technology, whereas the new Virtex-4 device uses 90 nm process technology.

Triple-Oxide – The Savior of Static Power

Triple-oxide simply means that we use a third thickness of oxide in making some of the transistors in the FPGA (two oxide thicknesses are used in devices like the Virtex-II Pro FPGA). Most transistors in the past had a thin oxide layer. Within those transistors could be low V_T, regular V_T, NMOS, or PMOS transistors. Thick-oxide transistors are mostly used for I/O drivers and a few other functions.

Oxide deposition thickness is a very stable and controllable process in the semiconductor industry because it depends on temperature, concentration, and exposure time. Figures 3a and 3b show the Virtex-4 transistor with the middle oxide thickness used in the triple-oxide process. You may notice that the oxide thickness is still very, very thin, but this thicker oxide transistor has much lower leakage than the standard thin-oxide low V_T and regular V_T transistors used in Virtex-II Pro FPGAs and in various parts of Virtex-4 FPGAs.

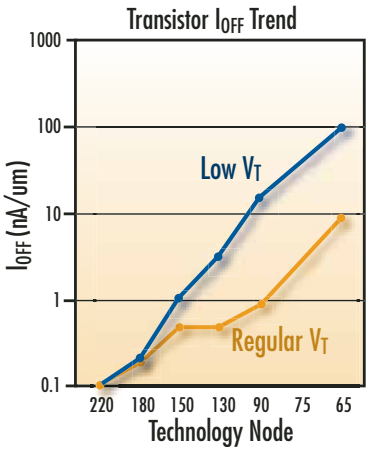


Figure 2 – Transistor leakage trends due to process scaling

Why Doesn't Everyone Use Triple-Oxide?

If triple-oxide is such a great process, why don't other companies like Intel™ or IBM™ use it in their own ASICs?

They probably would if it benefited them. The reason they don't is that all of their transistors need to run at speed; hence, they must use the low V_T leakier transistors for everything. FPGAs can have many different transistor types, which can be selected for function, power, or performance.

FPGAs can use different transistor types for different functions, and Xilinx designers have accomplished this balance.

Optimizing Performance and Leakage

Our IC designers have many things that they can do to adjust the mix to optimize for certain factors. The Virtex-4 FPGA is the first Platform FPGA designed for high speed and low power.

Low V_T transistors are used only where necessary for maximum speed, while the middle thickness of oxide from the triple-oxide process may be used for less aggressive performance with very low leakage. You may use different sizes and types of transistors for performance and function. Combinations are also possible, such as small and medium-sized low V_T fast transistors and small and medium-sized middle oxide thickness transistors. It is not a one-size-fits-all procedure.

Xilinx IC designers were given a directive to reduce power, among other things, in the Virtex-4 platform while maintaining the highest system performance. These transistors are used across the various FPGA functions of LUTs, I/O, interconnect, and configuration memory cells. Even within a given FPGA function, all transistors don't need to be the same, and that is up to the Xilinx IC designers (see Figure 4).

The surprising result of this balancing is that the overall static current in Virtex-4 devices with 90 nm process is reduced by 40% when compared to Virtex-II Pro devices with 130 nm process. Table 1 shows a chart of the weighted average changes to the transistors in the Virtex-4 die compared to Virtex-II Pro die, which allows you to arrive at the reduced transistor leakage in the Virtex-4 FPGA.

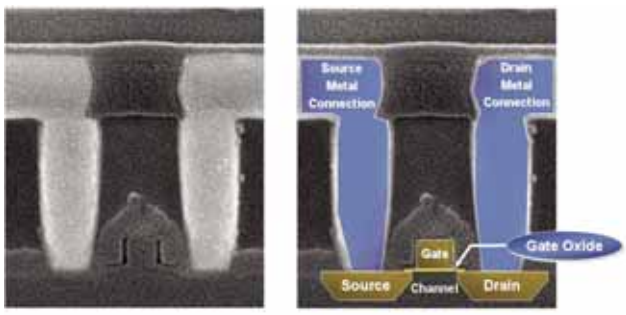


Figure 3a, 3b – Middle oxide thickness Virtex-4 transistor used in triple-oxide process and with highlighted portions of the transistors

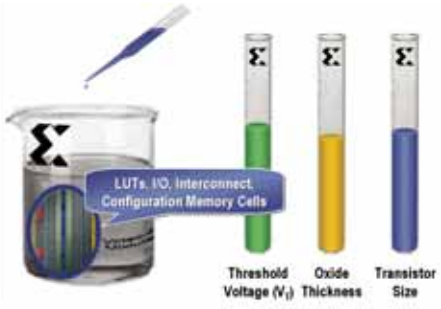


Figure 4 – Optimal transistor mix for minimizing leakage and maximizing performance

Dynamic Power Reduction

Static power reduction, while dramatic, is not the only power winner that you can take advantage of. Dynamic power is also reduced by 50% when compared to Virtex-II Pro FPGAs.

The dynamic power in the FPGA is governed by the following equation:

$$P_{Dynamic} = FPGA_{Core}(CV^2f) + FPGA_{I/O}(CV^2f)$$

The Virtex-4 family of FPGAs has the following:

- Reduced FPGA core dynamic power
  - Internal operating voltage is the dominant factor
  - Secondary scaling by frequency (f) and node capacitance (C)
- Constant FPGA I/O dynamic power
  - Unchanged voltage swing ($V_{I/O}$), toggle rate (f), and pin/pad capacitance (C) for a given I/O standard

So you can see that we may be able to have an effect on dynamic power inside the device, but that dynamic power consumed by I/O switching remains unchanged.

When we go from the 130 nm process of the Virtex-II Pro FPGA to the 90 nm process of the Virtex-4 FPGA, the internal supply voltage changes from 1.5V to 1.2V. This reduces the dynamic power consumption for every internal transistor by 36% ($1-\left[\frac{1.2}{1.5}\right]^2$) of that in the Virtex-II Pro FPGA.

Additionally, the FPGA internal composite capacitance is reduced in the Virtex-4 FPGA. This internal capacitance comprises transistor parasitic capacitances and trace-to-metal and trace-to-trace capacitances for the interconnecting metal traces. Figure 5 shows the capacitance involved relative to their structures.

As mentioned earlier, dynamic power is related to the bulk capacitance and internal voltage levels being switched, $P=CV^2f$. All things being equal, having a lower internal capacitance for the interconnects would be a benefit for dynamic power and reduced resistor-capacitor delay, but other factors contribute to interconnect capacitance, such as distance above the metal plane, interconnect width, and interconnect length.

Additionally, other parasitic capacitances such as gate-to-drain and gate-to-source are also part of the equation. Total capacitance for a path is based on a complex combination of parasitic capacitance

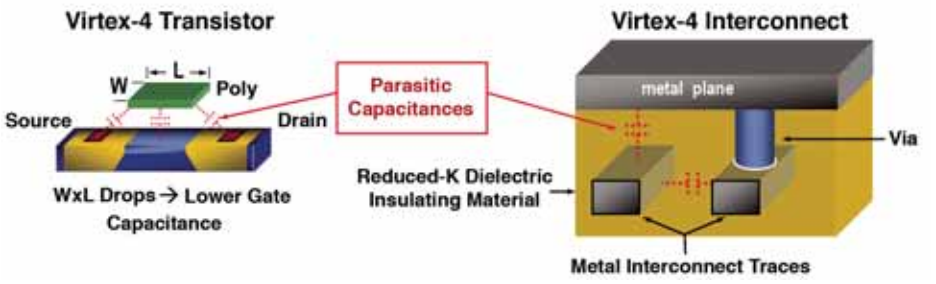


Figure 5 – Internal FPGA capacitance comprises parasitic transistor and interconnect capacitances

Does low-K reduce power? Low-K refers to the dielectric insulating material between the metal traces in the FPGA. Lower K dielectric insulating layers do reduce internal capacitances per unit trace length, but "low-K" is a relative term. Xilinx has reduced-K-insulating materials, and in the past has used low-K itself; we may do so again in the future.

Parameters	Virtex-II Pro	Virtex-4	Change
Channel Width Ratio	1.00	0.64	-36%
Channel Length Ratio		0.71	-29%
Leakage Current per Unit Width Ratio		1.14	+14%
Leakage Current per Transistor		0.74	-26%
V_{CCINT} Ratio		0.80	-20%
Static Power per Transistor Ration ($I_{LEAKAGE}$ * V_{CCINT})		0.59	-41%

Table 1 – Overall weighted average transistor leakage and parameter comparisons for 90 nm Virtex-4 transistors relative to 130 nm Virtex-II Pro transistors

in the transistors; the architecture of the interconnect paths and actual path lengths; and the number of hops through interconnect switches. Xilinx has reduced the overall capacitance for those components in the Virtex-4 FPGA.

The overall effect is mostly due to reduced gate capacitance and lowers capacitance by 20% for Virtex-4 FPGAs when compared to Virtex-II Pro FPGAs. Table 2 shows a dynamic power reduction of 50% for the Virtex-4 FPGA when compared to the Virtex-II Pro FPGA. We have a 23% reduction in dynamic power when running at a 50% higher frequency.

Because the Virtex-4 FPGA is a much higher performance device than the Virtex-II Pro FPGA, you may need to operate it at higher clock speeds to meet newer demanding performance targets that could never be achieved in previous systems.

Parameters	Virtex-II Pro	Virtex-4	Change
V_{CCINT}	1.5	1.2	-20%
C_{TOTAL} (rel.)	1.0	0.8	-20%
f_{MAX} (rel.)	1.0	1.5	+50%
Power at Same Frequency	2.25	1.15	-49%
Power at f_{MAX}	2.25	1.73	-23%

Table 2 – Chart showing changes in internal FPGA in Virtex-4 devices compared to Virtex-II Pro devices and the effect on dynamic power

Parameters	Virtex-II Pro	Virtex-4	Logic Slice Reduction	Logic Slice Power Reduction
QDR II SRAM Interface	550 slices	125 slices	77%	89%
SPI-4.2 Core	5000 slices	3900 slices	22%	61%

$$\text{Logic slice power reduction} = 100^{*}\left(1 - 0.5\,\frac{\text{Virtex-4 slice count}}{\text{Virtex-II Pro slice count}}\right)\%$$

Note: The factor of 0.5 above comes from the fact that Virtex-4 power per slice is 1/2 of the Virtex-II Pro power per slice because of the 50% dynamic power reduction in Virtex-4 devices compared to Virtex-II Pro devices.

Table 3 – QDR II SDRAM and SPI-4.2 core benefit in reduced power consumption from significant logic cell reduction due to new Virtex-4 ChipSync block

Embedded Blocks

Another major area of improvement in power consumption is in the area of embedded functions. This has always been a strength in Xilinx FPGAs, but it is more so in the Virtex-4 FPGA, even when compared to the feature-rich Virtex-II Pro FPGA.

In Virtex-4 FPGAs you can take further advantage of both static and dynamic power reduction by using the embedded functions, which are built as hard-logic functions.

When embedded functions are implemented as hard-logic functions instead of in configurable logic blocks and programmable interconnects, there is a lot less static and dynamic power consumed. This is because far fewer transistors are used for hard, fixed logic than for programmable logic. Additionally, there are no transistors needed to make connections for interconnects in the embedded functions, because there are no programmable interconnects.

Xilinx has carefully studied some of the functions that engineers like you have struggled with and that we have also found tedious to implement within the FPGA programmable logic. The new embedded functions lower power by 80-95% compared to their configurable logic blocks and routed counterparts in programmable silicon.

Comprehensive Power Planning Tools

Another useful thing in planning power is that Xilinx data sheets show you both typical and maximum power consumption numbers. Maximum numbers are for worst-case process, temperature, and voltage, but many designers are very happy to work with typical numbers, depending on their application and the number of parts being used in one system.

One additional very useful thing that you can take advantage of in planning for power consumption in Xilinx FPGAs are power planning tools. Xilinx web power tools are available for estimating power early in the design cycle. Also, as part of the Xilinx design flow, XPower looks in more detail at a mapped or routed design. Both can be found, along with power application notes, by searching the Xilinx website for the phrase "Xilinx Power Tools."

Conclusion

Xilinx has made profound improvements in both static and dynamic power in the Virtex-4 90 nm family of FPGAs when compared to Virtex-II Pro FPGAs – and (we believe) in comparison to our competitors. We have done this through a multi-pronged, purposeful approach in the areas of reduced leakage current, reduced dynamic power consumption, and embedded functions, without compromising performance. These, along with comprehensive power planning tools, make the Virtex-4 device an excellent choice for a high-performance FPGA system.

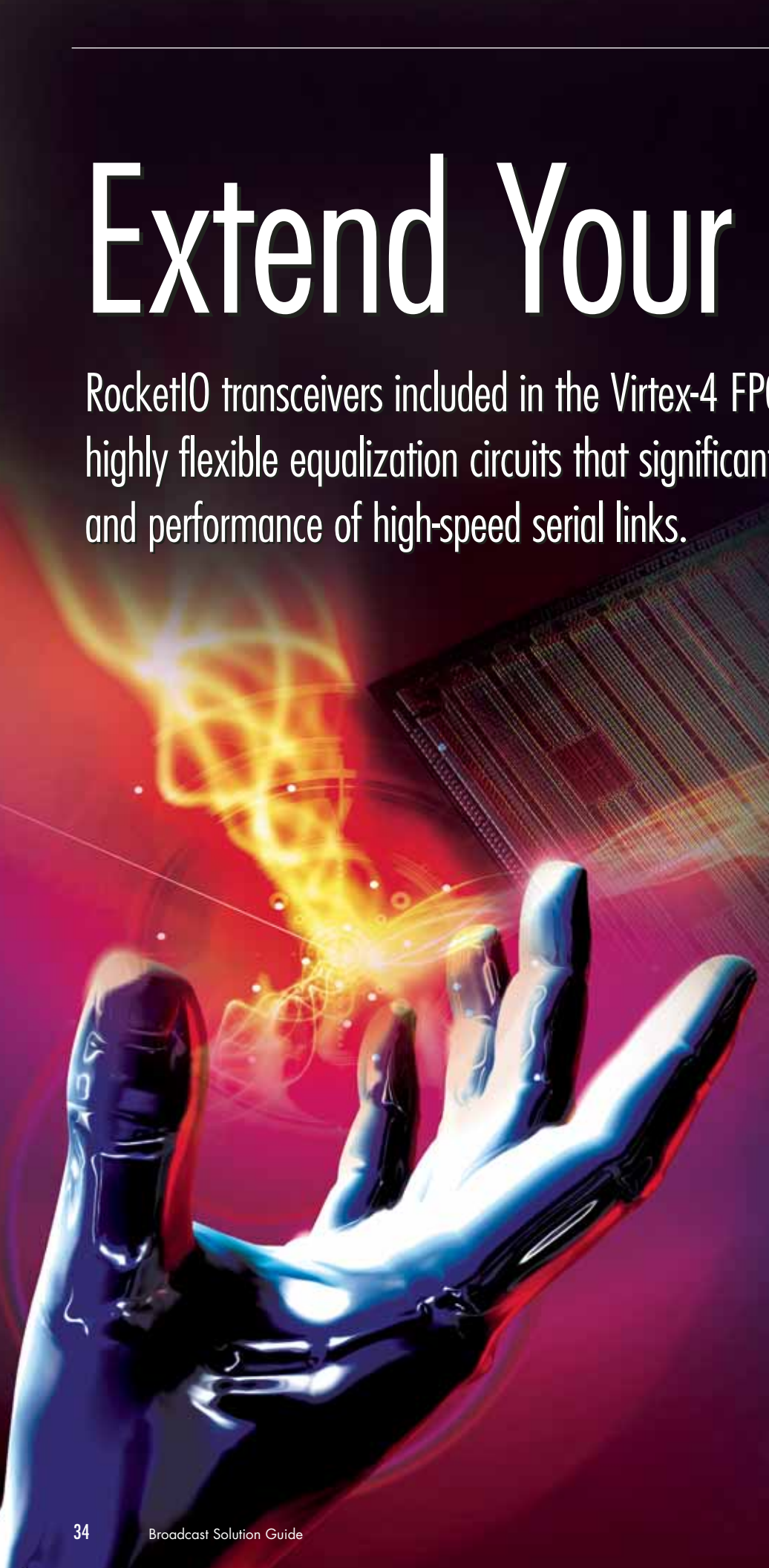
For more information about power consumption in Virtex-4 and other Xilinx FPGAs, visit *www.xilinx.com/products/design_resources/design_tool/grouping/power_tools.htm.*

Virtex-4 Embedded Functions and Reduction of Dynamic Power

- PowerPC – 50% power reduction compared to Virtex-II Pro PowerPC
- – 10:1 power reduction over FPGA fabric-built version
- DSP – XtremeDSP™ slice greatly reduces logic cells, which previously needed many filtering functions
- – 20:1 power reduction over Virtex-II Pro separated multiply/accumulate functions
- SSIO – New ChipSync™ block reduces logic cell count for SSIO (source synchronous I/O) designs
- – Significant logic cell savings for various memory and networking interface designs leads to reduction in overall power up to 9:1 for selected designs (see Table 3)
- Embedded Ethernet MAC(s) – No need to use logic and interconnect for MAC function, which saves >3,000 logic cells for the Xilinx implementation
- FIFO – SmartRAM™ memory includes built-in FIFO controllers, which can save hundreds of logic cells per FIFO and greatly simplify design as well

Extend Your Reach

RocketIO transceivers included in the Virtex-4 FPGA family incorporate highly flexible equalization circuits that significantly extend the range and performance of high-speed serial links.



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Every multigigabit backplane, trace, and cable distorts the signals passing through it. This degradation may be slight or devastating, depending on the conductor geometry, materials, length, and type of connectors used.

Because they spend their lives working with sine waves, communications engineers like to characterize this distortion in the frequency domain. Figure 1 shows the channel gain, also called the frequency response, of a perfectly terminated typical 50 ohm stripline (or 100 ohm differential stripline). This stripline acts like a low-pass filter, attenuating high-frequency sine waves more than lower frequency waves.

Figure 2 illustrates the degradation inherent to a digital signal passing through 20 inches (.5 meters) of FR-4 stripline. The dielectric and skin-effect losses in the trace reduce the amplitude of the incident pulse and disperse its rising and falling edges. We like to call the received pulse, much smaller than normal, a "runt pulse." In a binary communication system, any runt pulse that fails to cross the receiver threshold by a sufficient margin causes a bit error.

For the purposes of this discussion, three things degrade the amplitude of the runt pulse in a high-speed serial link: losses in the traces or cables, reflections due to connectors and other signal transitions, and the limited bandwidth of the driver and receiver.

A classic test of dispersion appears in Figure 3. This particular waveform – adjusted so that the long flat portions of the test signal represent the worst-case, longest runs of ones or zeros available in your data code – displays the runt-pulse amplitude. In the absence of reflections, crosstalk, or other noise, this single waveform (as measured at the receiver) represents a worst-case test of channel dispersion. Longer traces introduce progressively more dispersion, eventually causing receiver failure at (in this example) a length of 1.5 meters.

One measure of signal quality at the receiver is voltage margin. This number equals the minimum distance (in volts) between the signal amplitude and the receiver threshold at the instant sampling occurs. In a system with zero reflections, crosstalk, or other noise you could theoretically operate with a very small voltage margin and still expect the system to operate perfectly.

In a practical system, however, you must maintain a healthy noise margin sufficient to soak up the maximum amplitude of all reflections, crosstalk, and other noise in the system, while still keeping the received signal sufficiently above the threshold to account for the limited bandwidth and noise inherent to the receiver.

Following the example in Figure 4, a runt-pulse amplitude equal to 85% of the nominal low-frequency signal amplitude exceeds the receiver threshold by only 35%, instead of the nominal 50%. A smaller runt pulse with amplitude 75% of the normal size would reduce the voltage margin by half – a huge hit to your noise budget, but still workable. For generic binary communication using no equalization, we would like to see the runt pulse arrive with amplitude never smaller than 70% of the low-frequency pulse amplitude.

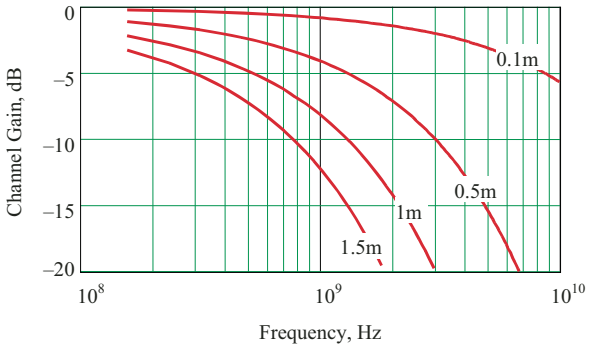


Figure 1 – The effective channel gain associated with a long PCB trace depends on the trace width, dielectric materials, length, and type of connectors used.

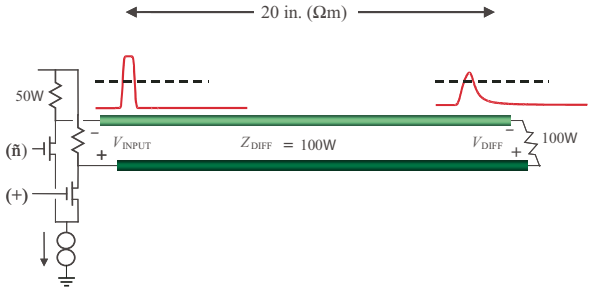


Figure 2 – Long traces reduce the amplitude of the input pulse and disperse its rising and falling edges.

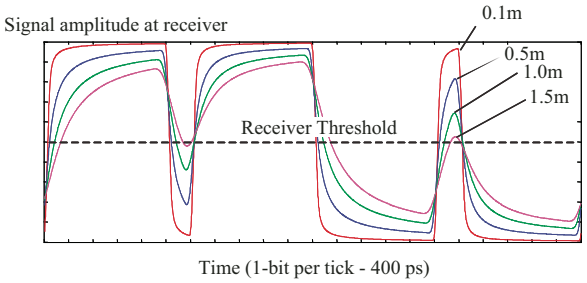


Figure 3 – This test waveform displays the worst-case runt-pulse amplitude.

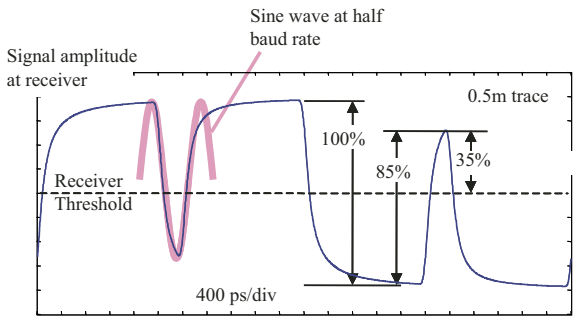


Figure 4 – A runt-pulse amplitude equal to 85% of the nominal low-frequency signal amplitude reduces the voltage margin above the threshold to only 35%, instead of the nominal 50%.

Runt-Pulse Degradation

On the left side of Figure 4 is a sine wave with a period of two baud. To the extent that the runt-pulse pattern (101) looks somewhat like this sine wave, you should be able to infer the runt-pulse amplitude from a frequency-domain plot of channel attenuation. Let's try it.

In Figure 4, the data waveform has a baud rate of 2.5 Gbps. One half this frequency (the equivalent sine wave frequency) equals 1.25 GHz. According to Figure 5, the half-meter curve gives you 4.5 dB of attenuation at 1.25 GHz. The same curve also shows 1.5 dB of attenuation at 1/10th this frequency, corresponding roughly to the lowest frequency of interest in an 8B10B coded data transmission system. The difference between these two numbers (-3 dB) approximates the ratio of runt-pulse amplitude to low-frequency signal amplitude at the receiver. With only -3dB degradation, the system satisfies our 70% frequency-domain criterion for solid link performance – precisely explaining why time-domain waveforms look so good at a half-meter.

Looking closely at Figure 4, the actual runt-pulse amplitude in the time domain is 85%, not quite as bad as the -3dB predicted by our quick frequency-domain approximation. This discrepancy arises partly from the harmonic construction of a square wave, where the fundamental amplitude exceeds the amplitude of the square wave signal from which it is extracted, and partly from the natural fuzziness inherent to any quick rule-of-thumb translation between the time and frequency domains. The simple frequency-domain criteria conservatively estimates these factors.

If your data code permits longer runs of zeros or ones than 8B10B coding, then you must use a correspondingly lower frequency as your "lowest frequency of interest." In the time domain, you will see the

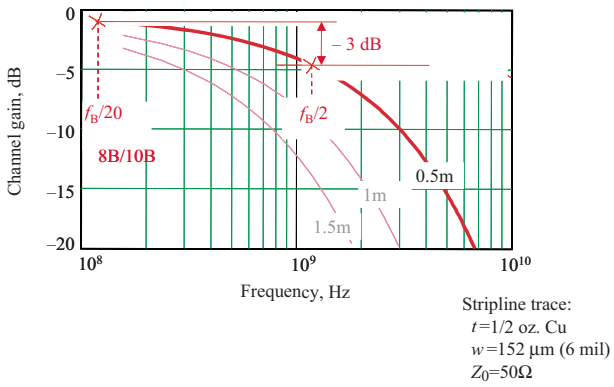


Figure 5 – The difference between high-frequency and low-frequency channel gain in this 2.5 Gbps system equals 3 dB.

received signal creep closer to the floor (or ceiling) of its maximum range before the runt pulse occurs, making it even more difficult for the worst-case runt pulse to cross the threshold.

As a rule of thumb, we look at the difference between the channel attenuation at the highest frequency of operation (the 101010 pattern) and the lowest frequency of operation (determined by your data coding run length) to quickly estimate the degree of runt-pulse amplitude degradation at the receiver. This simple frequency-domain method only crudely estimates link performance. It cannot substitute for rigorous time-domain simulation, but it can greatly improve your understanding of link behavior.

A channel with less than 1 dB of runt-pulse degradation works great with just about any ordinary CMOS logic family, assuming that you solve the clock skew problem either with low-skew clock distribution or by using a clock recovery unit at the receiver. A channel with as much as 3 dB degradation requires nothing more sophisticated than a good differential architecture with tightly placed well-controlled receiver thresholds. A channel with 6 dB of degradation requires equalization.

Transmit Pre-Emphasis

The Xilinx® Virtex™-4 RocketIO™ transceiver incorporates three forms of equalization that extend your reach on deeply degraded channels. The first is transmit pre-emphasis.

Figure 6 illustrates a simple binary waveform x[n] and the related first-difference waveform x[n]-x[n-1]. If you are familiar with calculus, you can think of the first-difference waveform as a kind of derivative operation. On every edge, the difference waveform creates a big kick. The transmit pre-emphasis circuit adds together a certain proportion of the main signal and the first difference waveform to superimpose the big kick at the beginning of every transition. As viewed by the receiver, each kick boosts the amplitude of the runt pulses without enlarging low-frequency portions of your signal, which are already too big.

The first-difference idea helps you see how pre-emphasis works, but that is not how it is built. The actual circuit sums not two but three delayed terms, called the pre-cursor, cursor, and post-cursor. This architecture gives you the capacity to realize both first and second differences by adjusting the coefficients associated with these three terms. Programmable 5-bit multiplying DACs control the three coefficients. The first and third amplitudes are always inverted with respect to the main center term, a trick that is accomplished by using the NOT-Q outputs of the first and third flip-flops. As an example, Figure 7 plots the frequency response corresponding to the particular coefficient set [-0.056, 0.716, -0.228].

Over the critical range from DC to 1.25 GHz, the pre-emphasis response rises smoothly – just the opposite of the plummeting curves drawn in Figure 5. The response peaks at 1.25 GHz. If you clock this pre-emphasis circuit at a higher data rate, the peak shifts correspondingly higher, always appearing just where you want it at a frequency equal to half the data rate.

Figure 8 overlays the pre-emphasis response with the channel response at 1 meter, showing a composite result (the equalized channel) that appears much flatter than either curve alone. In very simplistic terms, a flatter composite channel response should make a better-looking signal in the time domain.

The time-domain benefits of pre-emphasis appear in Figure 9. At shorter distances the signal appears over-equalized. The overshoot at each transition works fine in a binary system, assuming that the receiver has ample headroom to avoid saturation with the maximum-sized signal. At 1 meter, the signal looks quite nice, with very little runt-pulse degradation visible and (if you look closely) very little jitter. The 1.5 meter waveform now just meets the 70% criteria for runt-pulse success.

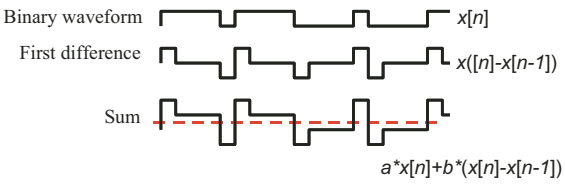


Figure 6 – The transmit pre-emphasis circuit creates a big kick at the beginning of every transition.

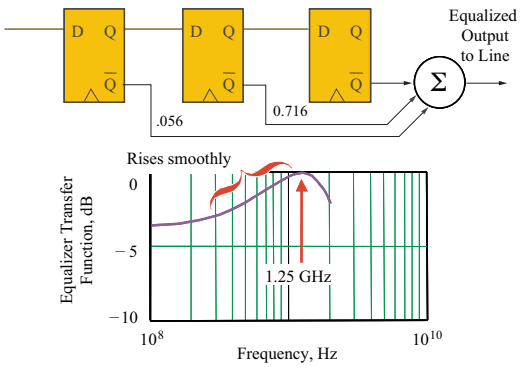


Figure 7 – Over the critical range from DC to 1.25 GHz, the pre-emphasis response rises smoothly.

Compared to a simple differential architecture, the pre-emphasis circuit has at least doubled the length of channel over which you may safely operate.

Linear Receive Equalizer

In addition to the pre-emphasis circuit, the RocketIO transceiver also incorporates a sophisticated 6-zero, 9-pole receive-based linear equalizer. This circuit precedes the data slicer. It comprises three cascaded stages of active analog equalization that may be individually enabled, turning on zero, one, two, or all three stages in succession.

Figure 10 presents the set of four possible frequency-response curves attainable with this receiver-equalization architecture. Each section of the equalizer is tuned to approximate the channel response of a typical PCB channel with an attenuation of about 3 dB at 2.5 GHz. With all stages on, you get a little more than 9 dB of boost at 2.5 GHz. Because the response keeps rising all the way to 5 GHz, this equalizer is useful for data rates up to and beyond 10 Gbps.

When setting up the equalizer, first select the number of sections of the RX linear equalizer that best match your overall channel response. Then fine-tune the overall pulse response using the 5-bit programmable coefficients in the transmit pre-emphasis circuit to obtain the lowest ISI, the lowest jitter, or a combination of both. After building the circuit, a clock phase adjustment internal to the receiver helps you map out bit error rate (BER) bathtub curves, so you can corroborate the correctness of your equalizer settings.

The flexibility provided by these two forms of equalization lets you interoperate with an amazing array of serial-link standards, meeting exact transmitted signal specifications and at the same time adding receiver-based equalization to keep your system working at the peak of performance.

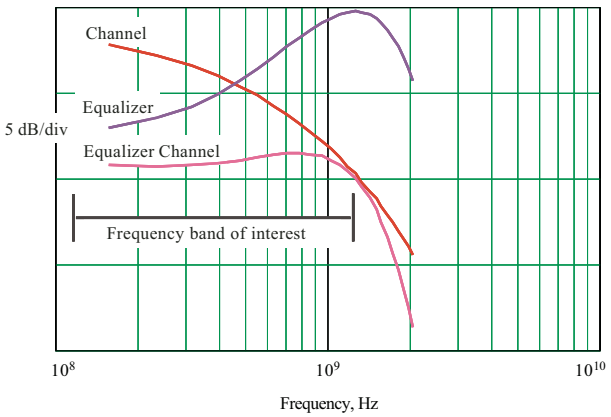


Figure 8 – Composing the pre-emphasis circuit with the channel produces an overall response much flatter than either curve alone.

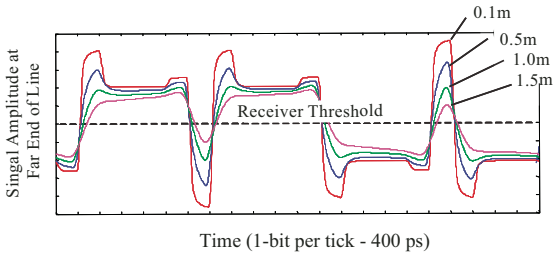


Figure 9 – A pre-emphasis circuit at least doubles the length of channel over which you may safely operate.

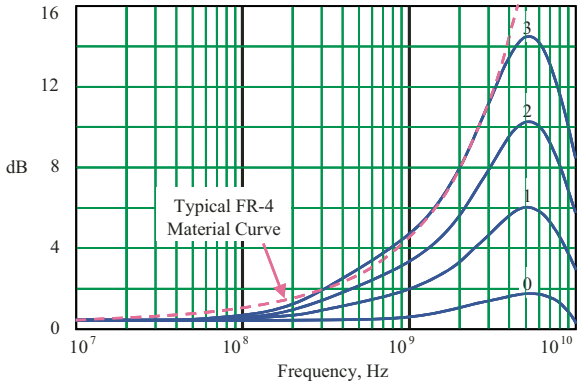


Figure 10 – The linear equalizer in the receiver may be set to one of four distinct response curves preprogrammed to match the response of various lengths of FR-4 PCB trace.

Decision-Feedback Equalizer

As a last defense against the slings and arrows of uncertain channel performance, the RocketIO transceiver includes a manually adjustable six-tap decision-feedback equalizer (DFE). This device is integrated into the slicer circuit at the receiver. The DFE is particularly useful with poor-quality legacy channels not initially designed to handle high serial data rates. It has the remarkable property of accentuating the incoming signal without exacerbating crosstalk.

Those of you familiar with signal processing will recognize that a DFE inserts poles into the equalization network, while a TX pre-emphasis circuit creates zeros. (A very accessible book about digital equalization, including DFE circuits, is John A.C. Bingham's "The Theory and Practice of Modem Design.")

Working together, the DFE, TX-pre-emphasis, and RX linear equalizer provide an incredibly rich array of possible adjustments.

Conclusion

For any channel with as much as 6 dB of runt-pulse degradation, a simple pre-emphasis adjustment easily doubles the length at which your link operates.

If you anticipate more than 6 dB of runt-pulse degradation, we strongly suggest that you simulate your system in detail before making the final equalizer adjustments. Contact your local Xilinx customer support office or visit the Xilinx website to obtain the necessary RocketIO models and associated design kits for modeling your channel. The modeling effort is well worth it, as equalization can substantially extend the reach of your circuits.

Howard Johnson, PhD, is the author of High-Speed Digital Design *and* High-Speed Signal Propagation. *He frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. For more information, visit* www.sigcon.com, *or e-mail* howie03@sigcon.com.

Figures 1, 3, 4, and 9 are adapted with permission from Johnson and Graham, *High-Speed Signal Propagation: Advanced Black Magic*, Prentice-Hall, 2003.

The High-Definition Video Challenge

Hardware developed by Modulus using the Xilinx Virtex-4 FPGA is ideally suited to demanding video processing.

Neil Brydon
Director of Product Marketing
Modulus Video
NBrydon@modulusvideo.com

High-definition television (HDTV) is driving a major transition for television broadcasters worldwide. There is an increasing amount of HD content, HD-capable receivers are achieving mass-market price points, and consumers are buying HDTVs at accelerating rates.

Interest in HDTV is already high in North America and Japan, and is rapidly gaining momentum in new markets such as Europe, Latin America, and Asia. This year, many of the major content distributors - terrestrial TV, cable, satellite, and now telecommunications companies - are all competing with new HD channels to address the demand.

HD uses six times the bandwidth of traditional standard-definition TV, and the challenge is to economically distribute thousands of new HDTV channels over existing satellite, cable, and IPTV networks.

A Standards-Based Response ... with a Catch

The solution is to deploy MPEG-4 AVC advanced video coding technology to deliver HDTV at around half the bandwidth of the legacy MPEG-2 technologies. This change is facilitated by the fact that AVC is compatible with existing MPEG-2 transports, allowing new HDTV-compressed services to be distributed over existing infrastructure. It has also endured the initial marketing hype and uncertainties; services are now being tested in field trials and customers are poised to receive services in their homes. As a result, the AVC standard has widespread industry support.

The HD AVC compression algorithms discard an impressive 99 of every 100 bits received, but these powerful algorithms present a substantial technical challenge. Enormous processing capability is required to support the powerful AVC compression tools. When fully supported, standard-definition AVC compression requires around 10 times more processing power than MPEG-2. A real-time platform designed to compress HD AVC, with all of the features and tools, can demand more than 500 billion operations per second. Currently, no ready-made silicon encoding solutions exist.

Today's CPUs are massively powerful, but their architecture is not universally suited to all video processing tasks. Many video-centric processing tasks are not efficiently handled by CPUs. For example, block-based and pixel-level processing tasks, such as exhaustive search motion-estimation (ME), use many compute cycles but are also very data-flow intensive, thus requiring complex register pipelines with fast memory access. A more effective approach is to combine the massive processing resource from CPUs with hardware acceleration,in a scalable and fault-tolerant server platform.

A Powerful Solution

With these challenges in mind, Modulus Video developed a platform that combines the processing capability of a server-based solution with custom acceleration hardware developed using FPGA technology from Xilinx.

The FPGA Advantage

Modulus considered using DSPs rather than FPGAs, but early benchmarking tests indicated that the Xilinx® Virtex™-4 FPGA option offered approximately 10 times more performance. For example, the motion estimation task suits a hardware-centric approach that can handle repeated sum of absolute difference (SAD) calculations. The data comparisons are very repetitive and many of the calculations are re-used. Although CPU-based implementations tend to struggle to feed the arithmetic logic units (ALU) from cache, the FPGA approach taken by Modulus can be customized to retain all of the values in a custom register pipeline.

The result is the award-winning Modulus ME6000 real-time high-definition AVC video encoder, which delivers broadcast image quality at half the bandwidth of MPEG-2. It provides comprehensive support for main profile encoding at level 4, to meet the stringent quality requirements of today's satellite, telco, and IPTV broadcasters. It also includes support for advanced features such as CABAC entropy coding, macro block adaptive field frame coding, and de-blocking filters.

Modulus Video MPEG-4 AVC encoders featuring Virtex-4 FPGA technology deliver the maximum video quality at the lowest bit rates, offering some of the most comprehensive MPEG-4 AVC SD and HDTV video processing found in the industry.

As impressive as the first implementations deployed have been, in fact they only start to extract the potential that the new AVC tools offer. The Modulus combination of CPUs plus the powerful FPGA technology offered by Xilinx provides an extremely flexible platform foundation capable of supporting ongoing development to further enhance the algorithms.

For more information, visit the Modulus Video website at *www.modulusvideo.com*, e-mail *info@modulusvideo.com*, or call (408) 245-2150.

Virtex-4™ SX ML402 XtremeDSP Evaluation Platform

Breakthrough DSP Performance at the Lowest Cost

Shrinking budgets and design cycles make evaluating, designing, and testing complex DSP systems more challenging than ever before.

With the Virtex-4 ML402 XtremeDSP Evaluation Platform, Xilinx delivers everything you need to meet these demands and finish faster. Powered by the 4VSX35 device and supported by industry-standard peripherals, connectors, and interfaces, the Virtex-4 ML402 DSP Evaluation Platform provides a rich feature set that spans a wide range of applications. Designed for use with the Xilinx System Generator for DSP software and Xilinx DSP IP algorithms, the ML402 DSP Evaluation Platform provides a great entry-level environment for developing signal-processing designs based on the Viretx-4 FPGA.

Virtex-4 SX FPGAs feature up to 512 XtremeDSP slices, each capable of running at 500 MHz. This performance makes them the ideal co-processors for your DSP processors and the best way to increase your system performance by several orders of magnitude.

The Complete DSP Evaluation Platform

The Xilinx ML402 is an entry-level XtremeDSP Evaluation Platform that brings together everything you need to create high-performance signal-processing designs based on industry-leading Virtex-4 FPGAs at a very low cost point.

- **Access to New Virtex-4 XtremeDSP Slices**
  - **High-Performance —** The Virtex-4 XC4VSX35-10C speed-grade FPGA on the ML402 platform includes 192 XtremeDSP slices, each capable of operating at 400 MHz and providing you with up to 77 GMACS performance.
  - **Low Power:** At only 2.3 mW/100 MHz per MAC, the new XtremeDSP slices enable unrivalled DSP power consumption for FPGAs.
- **Ease of Use —** By combining the Xilinx System Generator for DSP software tool and the ML402 evaluation platform, you get an easy-to-use and well-integrated design flow — from algorithm concept to hardware verification. The System Generator tool interfaces with MATLAB®/Simulink® and enables you to perform hardware co-simulation on the ML402 platform via JTAG.
- **Comprehensive Services and Support —** Reduce your time to knowledge with the Xilinx DSP Design Flow and DSP Implementation Techniques courses. You can also leverage the experience of senior DSP support engineers on the Xilinx Hotline.

Finish Faster with Xilinx DSP Design Solutions

Virtex-4 SX ML402 Evaluation Platform Features

- Xilinx Devices
  - XC4VSX35-FF668-10C
  - XC95144XL
  - XCCACE (System ACE™ CF)
  - XCF32P (Platform Flash)
- Clocks
  - 100-MHz Oscillator
  - Extra Clock Socket
- Memory
  - 64-MB DDR SDRAM
  - 1-MB ZBT SRAM
  - 32-MB Compact Flash
  - 8-MB Flash
  - 4-kb IIC EEPROM
  - 32-Mb Platform Flash
- Display
  - 16x2 Character LCD
- Connectors and Interfaces
  - Four SMA Connectors (Differential Clocks)
  - Two PS/2 Connectors (Keyboard/Mouse)
  - LVDS Personality Module
  - Four Audio (Line In, Line Out, Microphone, Head Phone)
  - RS-232 Serial Port
  - Three USB (Host and Two Peripherals)
  - Parallel Cable-IV Header
  - DB15 VGA Display
  - RJ-45 Ethernet Port

Applications

This multi-purpose board can be used for many signal processing applications including:

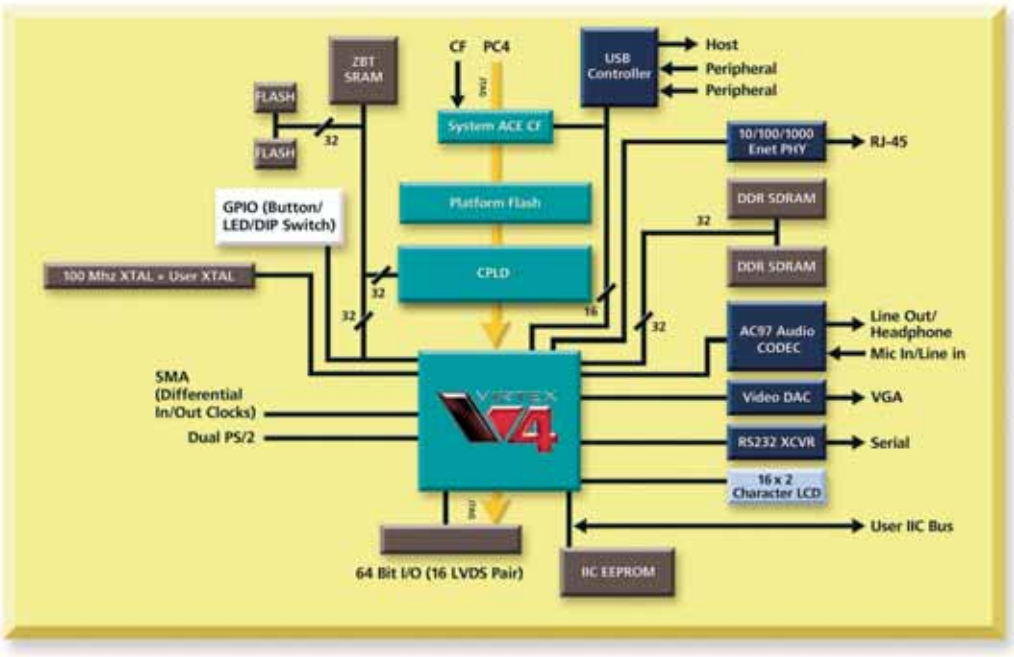
- Video and imaging algorithms
- Narrow-band systems (QAM demodulation, carrier timing recovery, channel coding)
- Spread-spectrum systems (chip-rate processing, RACH, path profiling, TCC)
- Multi-carrier systems (OFDM, MIMO, TCC)
- And many more.

How to Order

You can purchase your XtremeDSP Platform at **www.xilinx.com/store**.

Take the Next Step

Learn more by viewing the Xilinx DSP Demos on Demand at **www.xilinx.com/dod**. You can also find more details on the board at **www.xilinx.com/dsp**.



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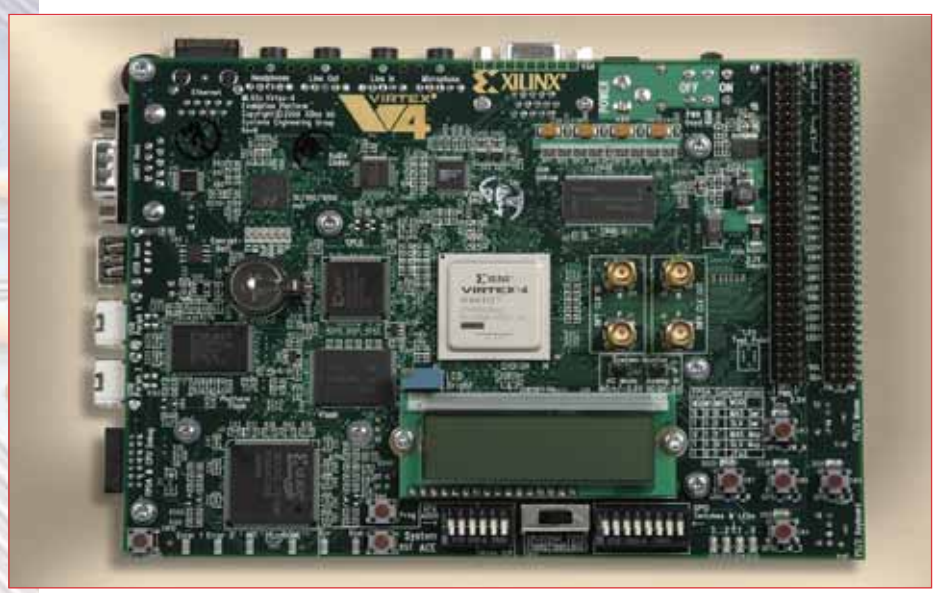
ML403 Virtex-4 FX Evaluation Platform

The Low-Cost, Embedded PowerPC Development Solution



Evaluating, designing and testing complex embedded systems present significant challenge with today's shrinking budget and design cycles.

Xilinx provides the answer with the ML403 Virtex™-4 FX Evaluation Platform. Powered by the XC4VFX12 device and supported by industry-standard peripherals, connectors and interfaces, the ML403 Virtex-4 FX Evaluation Platform offers a rich feature set that spans a wide range of applications. Designed for use with the Xilinx Embedded Development Kit (EDK) and award winning Platform Studio Tool Suite, the ML403 FX Virtex-4 Evaluation Platform provides a comprehensive environment for developing embedded designs based on the Virtex-4 FX FPGA.

Virtex-4 FX FPGAs feature up to two embedded PowerPC™ 405 processor cores with an integrated Auxiliary Processor Unit (APU) controller to deliver breakthrough performance.

The Ideal Platform for Your FPGA Embedded System Development

Explore the Rich Feature Set of the ML403 Virtex-4 FX Evaluation Platform

- Support for multiple clock sources and differential clock inputs
- Memory interfaces for DDR SDRAM, ZBT SRAM, and Flash
- Multiple FPGA programming modes: Platform Flash, System ACE, Linear Flash, and PC4
- Audio and video interfaces
- Multiple user interfaces: dual PS/2, IIC Bus, RS-232, USB, and Tri-Mode Ethernet

Optimize Your Design with Unique Built-In Silicon Features

- Embedded IBM PowerPC 405 RISC processor core
- Auxiliary Processor Unit (APU) controller provides a high-bandwidth interface between the PowerPC 405 core and co-processors to execute custom instructions in the FPGA fabric
- Two fully integrated UNH-certified 10/100/1000 Ethernet MACs enable system communication and management functions
- ChipSync™ source-synchronous technology embedded in every I/O ensures reliable data capture
- Xesium™ differential global clocks minimize skew and jitter for increased design margins

Finish Faster Using Proven Reference Designs

- Reference designs and IP cores for numerous applications accelerate your design cycle
- A comprehensive suite of application notes guides you every step of the way

ML403 Virtex-4 FX Evaluation Platform Contents

- **Xilinx Devices**
  - XC4VFX12-FF668-10C
  - XC95144XL
  - XCCACE (System ACE CF)
  - XCF32P (Platform Flash)
- **Clocks**
  - 100 MHz Oscillator
  - 2 Clock Sockets
- **Memory**
  - 64 MB DDR SDRAM
  - 1 MB ZBT SRAM
  - 512 MB Compact Flash
  - 8 MB Linear Flash
  - 4 kb IIC EEPROM
- **Display**
  - 16 x 2 Character LCD
- **Connectors and Interfaces**
  - 4 SMA Connectors (Differential Clocks)
  - 2 PS/2 Connectors (Keyboard/Mouse)
  - 2 Audio (In/Out, Microphone, Head Phone)
  - RS-232 Serial Port
  - 3 USB Ports (2 Peripherals/1 Host)
  - PC4 JTAG
  - DB15 VGA Display
  - RJ-45 Ethernet Port
  - General-Purpose I/O (Buttons/LEDs)

Additional Tools and Services

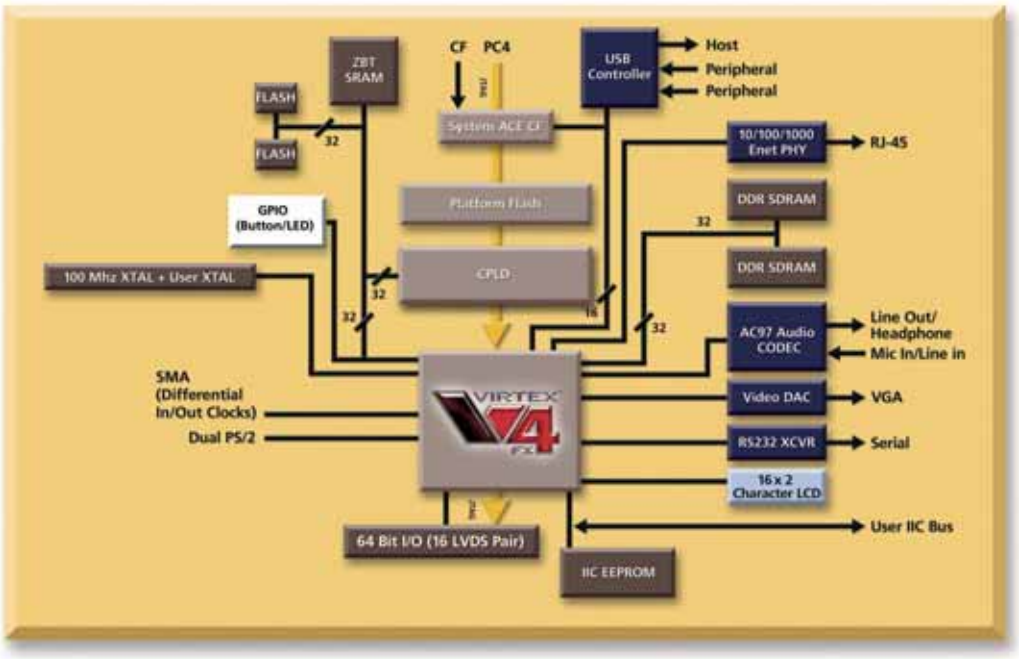
- Xilinx Integrated Software Environment (ISE)
- Xilinx Embedded Development Kit (EDK)
- ChipScope™ Pro – Debug, analyze and verify your design in real time
- IP Center – Comprehensive suite of verified IP cores
- Education Services – Increase your skill set and reduce your time-to- knowledge

Take the Next Step

Order your ML403 Virtex-4 FX Evaluation Platform today and get a head start on your Virtex-4 embedded design. For more information about the Virtex-4 FPGA family, visit ***www.xilinx.com/virtex4***.

Ordering Information

Part Number: HW-V4-ML403



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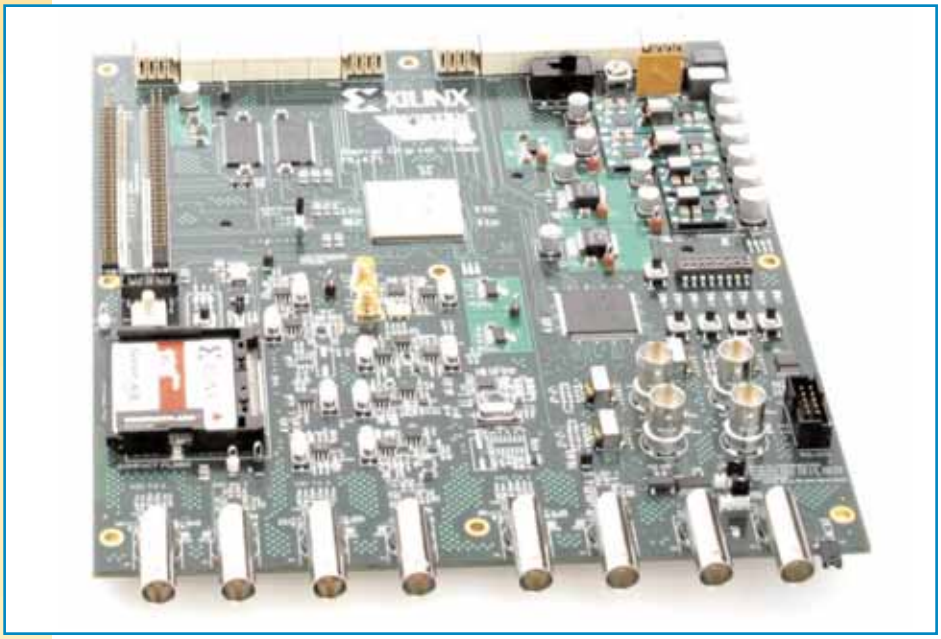
ML471 Virtex-4 FX Serial Digital Video Platform

The Connectivity Development Solution for Professional Video and Audio Applications



As the broadcast, telecom and IT markets converge, the integration of these differentkinds of systems, and connectivity between equipment presents a significant challenge to broadcasters. Your product will therefore have a competitive advantage if it is a flexible solution that can adapt to different connectivity requirements and provide a bridge between traditional and emerging video and audio interface standards.

The Xilinx® ML471 Virtex™-4 FX Serial Digital Video Platform demonstrates the ability of Xilinx Virtex-4 FPGAs to provide a variety of high-speed serial digital video interfaces required by all kinds of professional broadcast equipment, video conferencing systems and even some high-end consumer applications.

With the additional flexibility of expansion ports to incorporate daughter cards and to include the ML471 platform in larger systems like the ML410, this is the ideal vehicle for all your video and audio networking needs.

The Ideal Platform for Your Video System Development

Evaluate a Wide Range of Serial Digital Video Standards

- Two RocketIO serial digital video transmitters and two RocketIO receivers supporting SD-SDI (SMPTE 259M), HD-SDI (SMPTE 292M), and DVB-ASI (CENELEC EN-50083-9). Two inputs/outputs can also be combined to implement a dual-link HD-SDI (SMPTE 372M) input/output
- One SelectIO serial digital video transmitter and one SelectIO receiver supporting SD-SDI and DVB-ASI
- Two AES3 audio inputs and two AES3 audio outputs conforming to SMPTE 276M. Each input and output can handle an AES3 audio pair.
- One video sync input with passive daisy-chain output. HD and SD video sync inputs compatible. Tri-level, bi-level, and black-burst sync compatible.

Finish Faster Using Proven Reference Designs

- A complete set of reference designs to accelerate your design cycle
- A comprehensive suite of application notes guide you every step of the way

ML471 Virtex-4 FX Platform Contents

• Xilinx Devices

- XC4VFX60-10FF672C Virtex-4 FPGA
  Contains two embedded PowerPC cores, twelve bonded RocketIO multi-gigabit transceivers, and four tri-mode Ethernet MACs.
- Xilinx 95144XL CPLD
- XCCACE (System ACE CF)
- Platform Flash Socket

• Clocks

-Wide variety of XO and VCXO devices providing reference clocks

• Memory

- 64 MB DDR333 SDRAM memory array

• Connectors and Interfaces

- Ten 75-ohm BNC connectors
- Two SMA connectors
- General purpose I/O (Switches/LEDs)

• Personality Module and Expansion Connections

- Personality module connectors to the ML410, an embedded processing demonstration board containing a Xilinx Virtex-4 FX60 device and a complete set of PC-style peripherals
- ML40x expansion headers allow a number of Xilinx daughter cards to be added, including a dual tri-mode Ethernet PHY daughter card for video-over-IP applications.

Take the Next Step

Order your ML471 Virtex-4 FX Platform today and get a head start on your Virtex-4 video design. For more information about the Virtex-4 family, visit ***www.xilinx.com/virtex4***

Ordering Information

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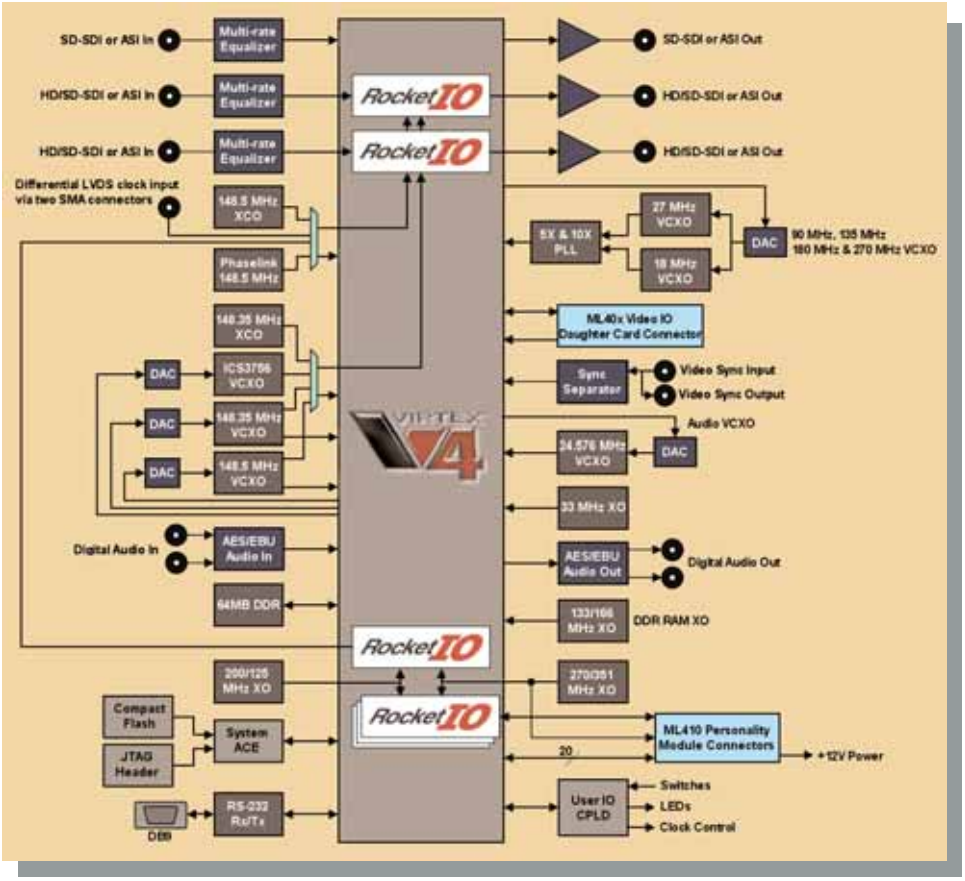

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Platform Studio™

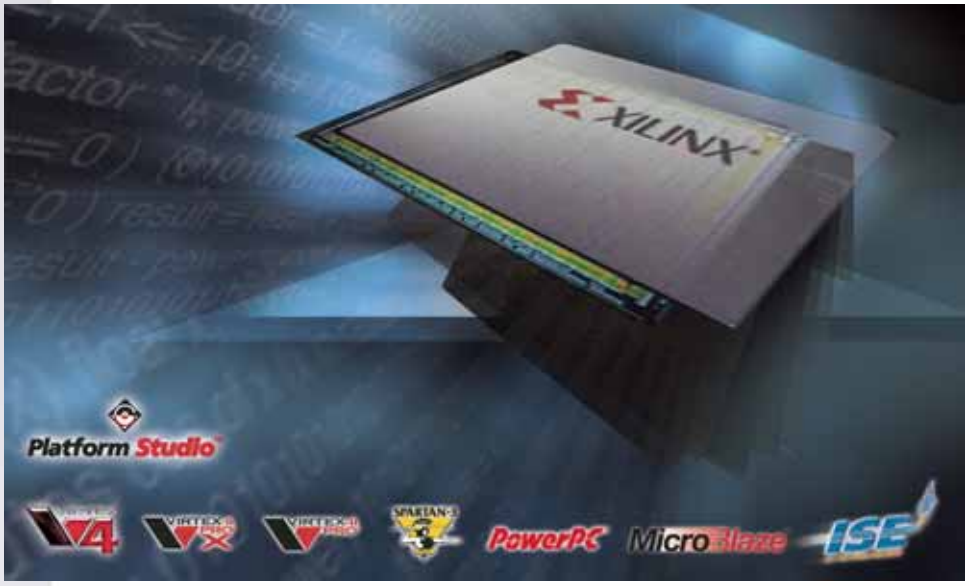
Embedded Development Kit

Programmable Systems Design is Now Easier than Ever

Developing a custom processing system using traditional solutions such as ASSPs or ASICs involves risk, time delays, and challenges in both resources and cost.

Programmable system platforms that include hard and soft processor core options, along with soft peripherals to implement a complete SoC in an FPGA, can resolve these issues. By combining a programmable Platform FPGA with a tightly integrated embedded design environment, system designers can accelerate their products to market.

The Xilinx Embedded Development Kit (EDK). streamlines and eases the platform development process. This kit includes the Platform Studio tool chain and a gallery of unique time saving tools like automatic BSP generation, IP creation, example software application generation, and integrated hardware/software debug capabilities.



Create Better Embedded Systems while Saving Time and Money

When you have the right tools, you can complete your designs faster and more easily with fewer errors. The Xilinx Embedded Development Kit (EDK) is a comprehensive suite of integrated development environment, software tools, system wizards, and IP that facilitates your design and utilizes all of the power offered by a programmable platform.

- **Create Designs Faster –** The Xilinx Platform Studio tool chain allows you to quickly configure a hardware platform and create a custom software design that includes appropriate libraries as well as automated generation of device drivers and a complete BSP (Board Support Package). This productive environment saves time by accelerating design steps that would otherwise be manual and error-prone.
- **Create Lower-Cost Designs –** Create your own custom processing platform while reducing your system cost by consolidating external functions into the FPGA. You can now have the capability to mix and match design architectures such as data and control path elements to provide the optimal solution to meet your product goals. With a flexible programmable platform, you can also optimize hardware/software design trade-offs for the best price-performance results.
- **Create High-Value Designs –** Many of the traditionally error-prone steps of interfacing hardware elements, together with defining the software/firmware for a custom hardware platform, are handled automatically using out-of-the-box verified components and tools. This means you can now spend your valuable development resources on creating high-value and unique product features.
- **Create More Profitable Designs –** Programmable, reprogrammable, and field-upgradable platforms mean that your product gets to market quicker and has a longer life, returning greater profitability. Enjoy your competitive advantage and spend more time on creating the value-added features that differentiate your products in the marketplace.

The Embedded Development Kit Includes the Following Tools and IP:

Xilinx Platform Studio (XPS)

- Graphical and command line tools for developing and debugging the hardware and software platforms for an embedded application.
- Hardware platform that includes graphical and textual definition tools and generation of simulation and implementation netlists for use with the ISE logic design tools.
- Software platform definition that includes graphical and textual tools for matching it to the hardware platform, editing source code, running the compiler tool chains, and library generation.

Software Development Tools

- GNU C/C++ compiler for MicroBlaze™ and PowerPC™
- GNU Debugger for MicroBlaze and PowerPC
- Other GNU utilities
- XMD – Xilinx Microprocessor Debug engine for MicroBlaze and PowerPC. It provides host-based target control using command line tools that enable complex regression testing.
- Data2MEM – A standalone application for loading and updating on-chip memory content directly within the FPGA bitstream.
- Base System Builder – Wizard to streamline configuring hardware elements, processor options, bus system, and IP options, as well as automatically generating memory map and design files.
- Platform Studio SDK (Software Development Kit) – Software focused development and debug environment based on Eclipse IDE.

Board Support Packages (BSPs)

- Stand Alone BSP – For non-RTOS systems (MicroBlaze and PowerPC)
- Wind River VxWorks – For PowerPC-platform FPGAs
- MontaVista Linux – For PowerPC-platform FPGAs
- Support for Xilinx MicroKernel (XMK) Systems

Processor IP

- PowerPC and MicroBlaze infrastructure and peripheral IP cores (CoreConnect™ Processor Local Bus (PLB) and On-Chip Peripheral Bus (OPB) infrastructure cores)
- Evaluation versions of high-value CoreConnect cores (EMAC 10/100, IIC Master Slave, HDLC Single Channel Controller, HDLC Multiple Channel (up to 256) Controller, UART 16450, 16550, and more)

MicroBlaze Soft Processor Core

- Industry's fastest 32-bit soft processor core

Embedded Development Kit Contents:

The EDK works in both PC and workstation environments, and includes:

- Embedded Development Kit CD
- ISE Design environment evaluation CDs
- Alliance Partner CDs (Trial versions of software tools, documentation, data sheets, etc., from third-party vendors supporting the Xilinx embedded processor solutions)

What Can You Do with the Embedded Development Kit?

- Define custom hardware platform for a programmable system using processor cores (PowerPC or MicroBlaze), parameterizable IP, and interconnect bus
- Develop a software platform to match custom hardware
- Employ verification support and interface to Xilinx-supported HDL simulators

Order the Xilinx Embedded Development Kit Today

Part Number	Description	Pricing
DO-EDK	Embedded Development Kit	Contact your local Xilinx representative for pricing and availability

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Embedded Systems Development Course

Learn how to effectively develop, debug, and simulate an embedded system using the newest EDK advancements by attending the Xilinx Embedded Systems Development course. For complete program and registration information, please visit:
www.support.xilinx.com/support/education-home.htm

Xilinx Design Services – XDS

XDS experience in system, logic, and embedded software design complements your own resources to optimize your budget, schedule, and performance requirements. See how we can help at:
http://www.xilinx.com/xds/

For the latest information on the Embedded Development Kit go to:
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XILINX®

The Spartan-3 FPGA Starter Kit – $99

Complete solution includes:

- Xilinx® Spartan™-3 200,000-gate platform FPGA XC3S200-4FT256C
- Xilinx 2 Mb Platform Flash configuration PROM – XCF02S
- 1 MB of fast asynchronous SRAM (512K x 16 or 256K x 32)
- 3-bit, eight-color VGA display port
- Nine-pin RS-232 serial port
- PS/2-style mouse/keyboard port
- Four-character, seven-segment LED display
- Eight slide switches
- Eight individual LED outputs
- Four momentary contact push-button switches
- 50 MHz crystal clock oscillator
- Three 40-pin expansion connection ports
- Universal power supply 100-240V AC, 50/60 Hz
- JTAG cable
- Spartan-3 resource CD
- ISE™ Foundation™ evaluation CD
- EDK evaluation CD

Part numbers

- DO-SPAR3-DK
- DO-SPAR3-DK-J (Japanese version)

The Spartan-3 FPGA Starter Kit gives you instant access to the complete platform capabilities of the Xilinx Spartan-3 family. The kit brings high-volume designs to reality quicker, at a lower cost, and on schedule.

The Spartan-3E FPGA Starter Kit – $149 (available in Q3CY05)

Complete solution includes:

- Xilinx Spartan-3E 500,000-gate platform FPGA XC3S500E-4FG320
- 32 Mb parallel flash
- 8 Mb SPI flash
- 32 MB of DDR SDRAM
- Board interfaces
- Ethernet 10/100 PHY
- USB 2.0 PHY + controller
- 3-bit, eight-color VGA display port
- Nine-pin RS-232 serial port
- PS/2-style mouse/keyboard port
- Three 40-pin expansion connection ports

Additional features

- Two-line LCD
- Four slide switches
- Eight individual LED outputs
- Two momentary contact push-button switches
- 90 MHz crystal clock oscillator
- Universal power supply 100-240V AC, 50/60 Hz
- JTAG cable
- Spartan-3/3E resource CD
- ISE Foundation evaluation CD
- EDK evaluation CD

Part numbers

- DO-SPAR3E-DK
- DO-SPAR3E-DK-J (Japanese version)

The Spartan-3E FPGA Starter Kit includes a full-featured development board based on the Spartan-3E platform FPGA family.

For more information about the Spartan-3 FPGA Starter Kit, visit *www.xilinx.com/s3boards/*. For more information about the Spartan-3E FPGA Starter Kit, visit *www.xilinx.com/s3eboards/*.

VIRTEX V4

Breakthrough Performance At The Lowest Cost.

LX SX FX

XILINX®

Breakthrough Capabilities. Lowest Price

One Family—Multiple Platforms

The Virtex-4™ family of FPGAs includes three platforms, each with an optimized balance of capabilities and cost. It's a breakthrough in technology and value, only from Xilinx.

Unbeatable Performance

500 MHz Clocking

Achieve the highest system speeds with flexible, precise clock control.

622 Mbps—10.3125 Gbps Serial I/O

Solve your toughest serial I/O challenges.

256 GMACS Digital Signal Processing

Create ultra-high-performance DSP systems.

Processor Acceleration

Build hardware accelerators easily for the 450 MHz PowerPC™ processor with the Auxiliary Processor Unit (APU) controller.

Highest Integration

200,000 Logic Cells Plus Embedded Functionality

Increase effective logic capacity and decrease device cost; embedded cores deliver guaranteed performance while preserving logic fabric for custom functions.

Reduced Power Consumption

Save 1 to 5 Watts per FPGA

Achieve performance goals while staying within your power budget.

73% Lower Static Power

Enabled by Triple-Oxide Technology.

86% Lower Dynamic Power

Enabled by abundant, flexible, embedded IP blocks.

Compared to competing FPGAs.

Superior Signal Integrity

7x Less SSO Noise and Crosstalk

Ensure reliable operation for high bandwidth parallel interfaces, such as memory interfaces, with unique packaging technology that minimizes crosstalk and jitter.

Maximum Productivity

Complete Design Tool Suite

Speed design creation with twice the productivity of ASIC design flows. Slash debug cycle time with the advanced verification and real-time debug capabilities of ChipScope™ Pro tools.

Over 200 Pre-Verified IP Cores

Design faster and reduce risk with the latest pre-verified, pre-optimized intellectual property cores.

Education and Customized Support

Accelerate product development with online resources, training courses, and premium support services. The Xilinx Productivity Advantage (XPA) offers bundled packages of software, education, support services, and IP cores.

Expert Design Services

Augment your development team with our worldwide network of Xilinx Design Service (XDS) and partner system design experts.

Points Ever.

Lowest System Cost

Freedom to Choose

Our multiple platforms enable you to select the device that most cost-effectively implements your unique application; you pay only for the capabilities you need.

Virtex-4 LX

Optimized for high-performance logic:

- Highest logic-to-feature ratio
- Highest I/O-to-feature ratio

Virtex-4 SX

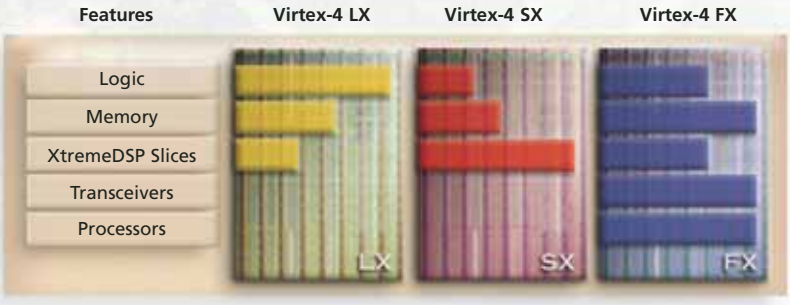
Optimized for high-performance signal processing:

- Highest DSP-to-feature ratio
- Highest memory-to-feature ratio

Virtex-4 FX

Optimized for embedded processing and high-speed serial connectivity:

- Embedded PowerPC and Ethernet MAC
- RocketIO™ multi-gigabit serial transceivers



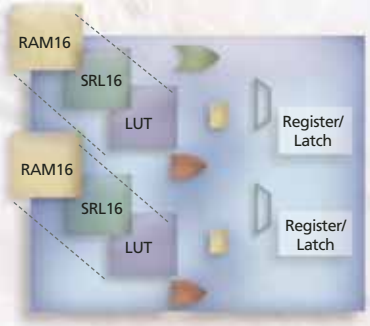
The innovative ASMBL (Advanced Silicon Modular BLock) architecture enables Xilinx to assemble FPGA platforms with varying feature mixes to meet the requirements of different application domains.

Virtex-4 EasyPath™ FPGAs

The lowest system cost just got lower with the industry's easiest, conversion-free path for volume production.

- EasyPath devices are identical in every way to the FPGA—there is no risk of conversion, no hidden costs
- Enjoy unprecedented flexibility and fastest turn-around times at prices below Structured ASICs

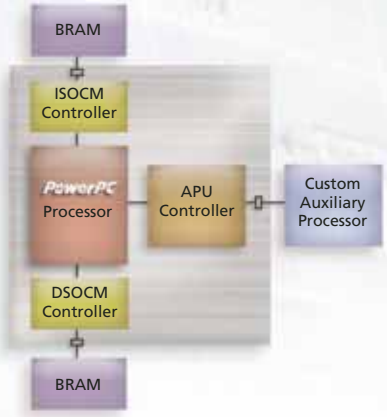
The World's Most Advanced



Most Flexible High-Performance Logic Architecture

Achieve the most compact utilization.

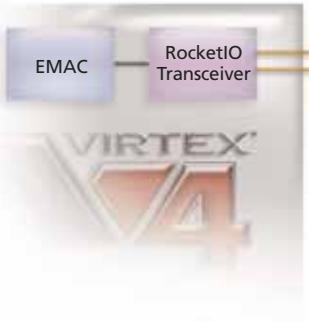
- Up to 200,000 logic cells
- High-speed carry logic
- Configurable as logic, RAM, or shift registers



Enhanced IBM PowerPC™ 32-bit RISC Processor with APU Controller

Build area-efficient, high-performance embedded systems or complex control functions.

- 700+ DMIPS @ 450 MHz; up to 1,400+ DMIPS in a single FPGA with two processors
- Low power consumption: 0.45 mW/MHz
- Auxiliary Processor Unit (APU) controller makes it easy to integrate hardware accelerators



10/100/1000 Mbps Ethernet Media Access Controller

Connect to the Internet via an integrated tri-mode EMAC.

- UNH-verified compliance
- Built-in hard IP frees user logic resources

FPGA Technology

500 MHz Xesium™ Clocking Technology

Obtain the highest performance with up to 80 clocks.

- 32 global and 48 regional clocks
- Up to 20 digital clock managers
- Phase precision <30 ps for better design margin
- Differential global clocking to minimize skew and jitter
- Precision phase-matched clock dividers

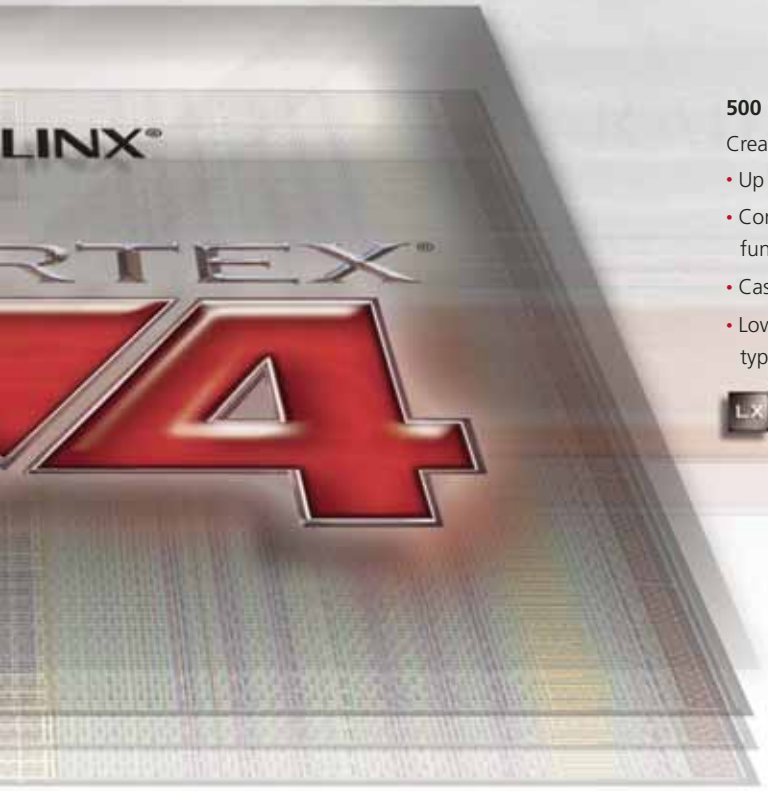
- Small-Local
- Up to 1.36 Mbit
- Medium-Block
- Up to 10 Mbit
- Large-External
- SRAM, DRAM, Flash

500 MHz Smart RAM Hierarchy

Build the right memory for any application with compact utilization and highest performance.

- Configure multi-rate FIFO from block RAM without consuming logic resources
- Block RAM with built-in Error Checking and Correction (ECC) for high-reliability systems
- Integrated source-synchronous support for easy interfaces to external memory

LX SX FX

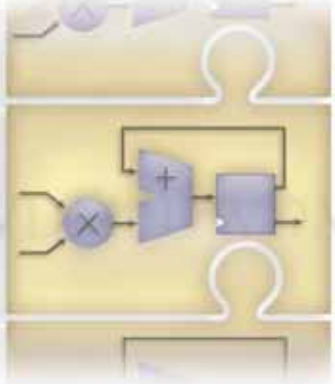


500 MHz XtremeDSP™ Slice

Create ultra-high-performance DSP systems.

- Up to 512 slices for 256 GMACS
- Configurable for over 40 DSP and arithmetic functions
- Cascadable within a column at full system speed
- Low power consumption: 2.3 mW/100 MHz at a typical toggle rate

LX SX FX



Fourth-Generation Design Security

Safeguard your design with SecureChip AES.

- Advance Encryption Standard with 256-bit key

LX SX FX

622 Mbps–10.3125 Gbps RocketIO™ Transceivers

Implement serial protocols to connect or bridge "anything to anything".

- Highest design margin
- Flexible SERDES with the broadest operating range supports multi-rate applications
- Compliance with the widest range of standards and protocols to connect chips, backplanes, and optical devices

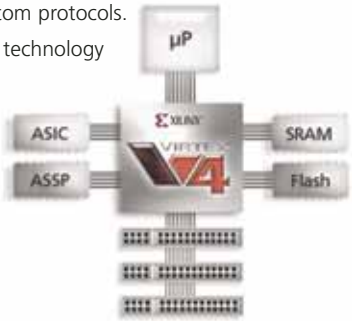
LX SX FX

1+ Gbps SelectIO™ Technology

Implement industry-standard and custom protocols.

- New ChipSync™ source-synchronous technology simplifies board design
- 1+ Gbps differential I/O
- 600 Mbps single-ended I/O
- Digitally controlled impedance with XCITE technology for reduced component count and board size

LX SX FX

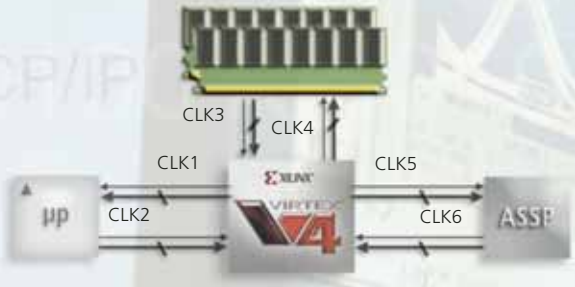


A Solution For Every System Design

Implement Networking and System Interface Standards

SelectIO technology, combined with pre-verified IP cores, makes it easy to support all popular interface standards and offers the flexibility to interface/bridge to virtually any external component.

- Design with PCI, RapidIO, XSBI, SPI4.2, and more
- Configure I/Os: 1.5V to 3.3V; HSTL, LVDS, and more
- Flexibly support multiple electrical standards in the same device with 16 individually configurable I/O banks



Simplify Source-Synchronous Interfacing

ChipSync technology integrated into every SelectIO block makes it easy to create high-performance source-synchronous interfaces.

- Achieve performance targets and simplify PCB layout with flexible per-bit deskew
- Easily synchronize incoming data to FPGA internal clock with optional Serializer/Deserializer and Bitslip technology

Build Highest-Bandwidth Memory Interfaces

ChipSync technology and the Memory Interface Generator tool make it easy to build reliable interfaces to the latest high-performance memories.

Memory	Clock Rate	Data Rate	Bandwidth*
DDR2 SDRAM	267 MHz	534 Mbps	230 Gbps
QDR II SRAM	300 MHz	2 x 600 Mbps	259 Gbps
RLDRAM II	300 MHz	600 Mbps	259 Gbps
FCRAM II	300 MHz	600 Mbps	259 Gbps
DDR SDRAM	200 MHz	400 Mbps	173 Gbps

* Maximum bandwith with 432 I/Os

Accelerate Design with Complete Serial Solutions

Build chip-to-chip, board-to-board, and box-to-box applications quickly and easily.

- Obtain assured compliance with multiple standards
- Reduce system design time with pre-verified IP
- Implement custom solutions
- Reduce pin/trace count to simplify board design and reduce manufacturing cost

Upgrade Legacy Backplanes With 10.3125 Gbps RocketIO

Future-proof your backplanes with data rates adjustable to any speed from 622 Mbps to 10.3125 Gbps.

- Simplify backplane design with advanced channel equalization

Storage		1GFC SATA	2FGC SATA2	SAS 4GFC		SAS2 SATA3	8GFC	
Networking		GbE		XAUI			CEI (OIF) 10GbE Aurora	CEI (OIF)
Telecom	OC-12		OC-48	SFI-4.2 SxI-5			OC-192* Aurora	
Computing		GbE	PCIE	SATA SRIO	SATA2		Aurora	
Video		HD-SDI						
Rate (Gbps)	0.622	1.0	2.0	3.0	5.0	6.0	10.0	

Virtex-4 FX FPGAs support all of these standards

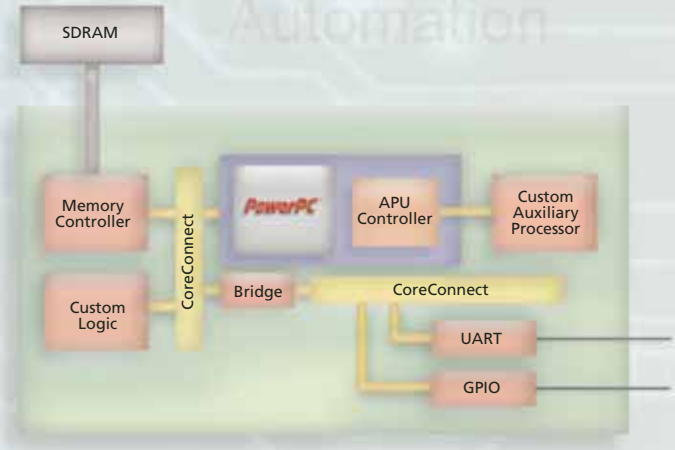
* Payload compatible

Bridge Protocols

Protect your investment by interfacing easily to legacy ASSPs or ASICs.

- Implement all major protocols with pre-verified IP
- Connect external peripheral components to any processor with standards-compliant I/O

Challenge



Accelerate Processing Performance

The PowerPC processor's APU controller makes it easy to create powerful custom co-processors in the Virtex-4 logic fabric.

- Optimize hardware/software partitioning to maximize FPGA utilization and minimize hardware cost
- Offload CPU-intensive operations such as video processing, 3D data processing, and floating-point math

Integrate Complete Processor Subsystems

Build an embedded processor subsystem custom tailored to your requirements.

- Start with the embedded PowerPC core or MicroBlaze™ soft processor core.
- Add an IBM CoreConnect bus for flexible connectivity and guaranteed performance
- Complete your subsystem with pre-verified peripheral IP cores
- Reduce design time with a ready-to-use UltraController PowerPC 405-based microcontroller subsystem package

Create Ultra-High-Performance DSP Systems

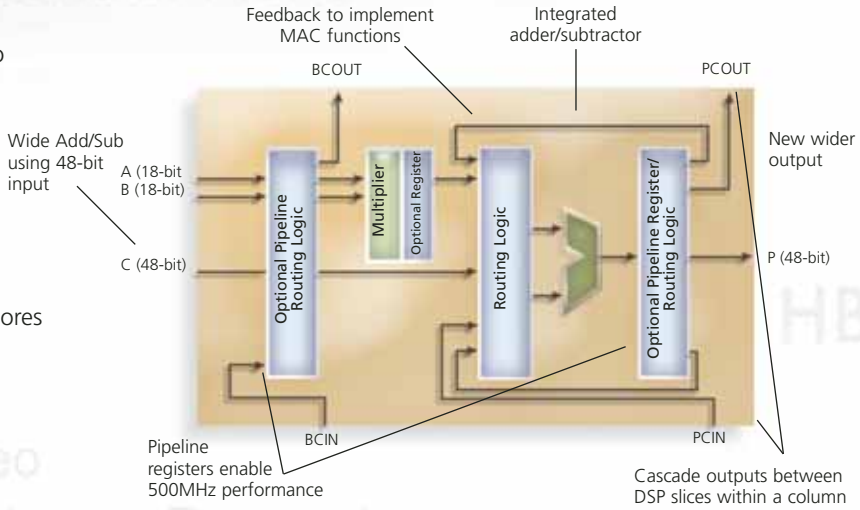
Turbocharge your DSP systems with Virtex-4 FPGAs.

- Achieve 256 GMACS performance with 512 XtremeDSP slices in a medium logic-density FPGA
- Take the performance of your favorite DSP processor to new levels by building custom pre/post/co-processing hardware
- Configure XtremeDSP slices to create more than 40 different functions, such as MACs, multipliers, adders, and Muxes, without consuming logic fabric resources or incurring logic routing delays
- Build high-performance filters by cascading slices with no loss in speed

Solve Multi-Channel DSP Challenges

Build economical multi-channel DSP systems.

- Reduce system cost with Virtex-4 SX devices offering up to 512 XtremeDSP slices in a single package
- Minimize power consumption–the XtremeDSP slice consumes only 2.3 mW/100 MHz, at a typical toggle rate of 38%, that gives you only 6% of the power consumption of previous-generation circuits
- Achieve high compute density using SRL16 shift registers



XtremeDSP slice: increased functionality, flexibility, and performance

Choose the Ideal Virtex-4 Device for Your Application

	Virtex-4 LX (Logic)								Virtex-4 SX (Signal Processing)			Virtex-4 FX (Embedded Processing & Serial Connectivity)					
	XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
EasyPath™ Cost Reduction Solutions[1]	—	XCE4VLX25	XCE4VLX40	XCE4VLX60	XCE4VLX80	XCE4VLX100	XCE4VLX160	XCE4VLX200	XCE4VSX25	XCE4VSX35	XCE4VSX55	—	XCE4VFX20	XCE4VFX40	XCE4VFX60	XCE4VFX100	XCE4VFX140
CLB Array (Row x Column)	64 x 24	96 x 28	128 x 36	128 x 52	160 x 56	192 x 64	192 x 88	192 x 116	64 x 40	96 x 40	128 x 48	64 x 24	64 x 36	96 x 52	128 x 52	160 x 68	192 x 84
Slices	6,144	10,752	18,432	26,624	35,840	49,152	67,584	89,088	10,240	15,360	24,576	5,472	8,544	18,624	25,280	42,176	63,168
Logic Cells	13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448	23,040	34,560	55,296	12,312	19,224	41,904	56,880	94,896	142,128
CLB Flip Flops	12,288	21,504	36,864	53,248	71,680	98,304	135,168	178,176	20,480	30,720	49,152	10,944	17,088	37,248	50,560	84,352	126,336
Max. Distributed RAM Bits	98,304	172,032	294,912	425,984	573,440	786,432	1,081,344	1,425,408	163,840	245,760	393,216	87,552	136,704	297,984	404,480	674,816	1,010,688
Block RAM/FIFO w/ECC (18 kbits each)	48	72	96	160	200	240	288	336	128	192	320	36	68	144	232	376	552
Total Block RAM (kbits)	864	1,296	1,728	2,880	3,600	4,320	5,184	6,048	2,304	3,456	5,760	648	1,224	2,592	4,176	6,768	9,936
Digital Clock Managers (DCM)	4	8	8	8	12	12	12	12	4	8	8	4	4	8	12	12	20
Phase-matched Clock Dividers (PMCD)	0	4	4	4	8	8	8	8	0	4	4	0	0	4	8	8	8
Max Select I/O™	320	448	640	640	768	960	960	960	320	448	640	320	320	448	576	768	896
Total I/O Banks	9	11	13	13	15	17	17	17	9	11	13	9	9	11	13	15	17
Digitally Controlled Impedence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Max Differential I/O Pairs	160	224	320	320	384	480	480	480	160	224	320	160	160	224	288	384	448
I/O Standards	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, LVTTL, LVCMOS33, PCI-X, PCI66, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2I, SSTL2II, SSTL18 I, SSTL18 II																
XtremeDSP™ Slices	32	48	64	64	80	96	96	96	128	192	512	32	32	48	128	160	192
PowerPC™ Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	1	1	2	2	2	2
10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	—	—	—	—	2	2	4	4	4	4
RocketIO™ Serial Transceivers	—	—	—	—	—	—	—	—	—	—	—	0	8	12	16	20	24
Configuration Memory Bits	4,765,568	7,819,904	12,259,712	17,717,632	23,291,008	30,711,680	40,347,008	51,367,808	9,147,648	13,700,288	22,745,216	4,765,568	7,242,624	13,550,720	21,002,880	33,065,408	47,856,896
	XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
SF363	17 x 17 mm	—	240	240	240								240					
FF668	27 x 27 mm	—	448	320	448	448	448					320	448					320
FF1148	35 x 35 mm	—	768			640	640	768	768	768			640					
FF1513	40 x 40 mm	—	960						960	960	960							
FF672	27 x 27 mm	12	352											320 (8)[4]	352 (12)[4]	352 (12)[4]		
FF1152	35 x 35 mm	20	576												448 (12)[4]	576 (16)[4]	576 (20)[4]	
FF1517	40 x 40 mm	24	768														768 (20)[4]	768 (24)[4]
FF1760	42.5 x 42.5 mm	24	896															896 (24)[4]

Notes: 1. EasyPath solutions provide conversion-free path for volume production.
2. SFA Packages (SF): flip-chip fine-pitch BGA (0.80 mm ball spacing).
FFA Packages (FF): flip-chip fine-pitch BGA (1.00 mm ball spacing).
All Virtex-4 LX and Virtex-4 SX devices available in the same package are footprint-compatible.
3. MGT: RocketIO Multi-Gigabit Transceivers.
4. Number of available RocketIO Muti-Gigabit Transceivers.

Pb-free solutions are available. For more information about Pb-free solutions, visit www.xilinx.com/pbfree.

QUALITY IS EVERYONE'S BUSINESS.

Take the Next Step

Visit us online at ***www.xilinx.com/virtex4***

Quality Commitment & Policy

Xilinx is committed to excellence in quality, reliability, and on-time delivery. We strive for continuous improvement in business processes, engineering & development, service & support, and manufacturing. At Xilinx, Quality is Everyone's Business.

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OPTIMIZED FOR LOGIC | OPTIMIZED FOR DSP | OPTIMIZED FOR PROCESSING/CONNECTIVITY

VIRTEX 4

Introducing the world's first multi-platform, domain-optimized FPGA family—delivering breakthrough capabilities and performance at every price point.

THE FREEDOM TO CHOOSE

For the first time ever, you can select from multiple FPGA platforms, optimized for application domains. You choose the exact capabilities you want. You pay only for what you need. Virtex-4 FPGAs are built upon our unique ASMBL™ (Advanced Silicon Modular Block) architecture, enabling Xilinx to *assemble* logic, memory, I/O, DSP, processors and more, giving you complete freedom of choice.

Easiest to Use Software

A SOLUTION FOR EVERY SYSTEM DESIGN CHALLENGE

The three Virtex-4 platforms—LX, SX, and FX—offer you up to 200,000 logic cells, and 500 MHz tuned performance. Our new ChipSync™ technology simplifies source-synchronous interfaces. You can implement serial protocols at any speed from 600 Mbps to 11.1 Gbps with RocketIO™ multi-gigabit transceivers. Hardware acceleration for the embedded PowerPC™ is easy with our auxiliary processing unit. And with XtremeDSP™ delivering 256 GMACS, you can solve those ultra-high performance DSP challenges.

All of your design possibilities just became realities. See for yourself at ***www.xilinx.com/virtex4***.

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The Programmable Logic Company℠

www.xilinx.com

LOWEST SYSTEM COST · HIGHEST SYSTEM PERFORMANCE

The Spartan-3™ Platform FPGA Family

The World's Lowest-Cost FPGAs

Today's electronic systems need to be brought to market more quickly, within budget, and with feature-sets that outperform competing products.

Xilinx Spartan-3 FPGAs deliver the ideal solution, using 90nm process technology and staggered I/O pads to give you up to 5 million system gates and up to 784 I/Os with the lowest cost per gate and lowest cost per I/O of any FPGA. Spartan-3 EasyPath™ FPGAs further extend the benefits of the Spartan-3 FPGA family to volume production with a conversion-free, no-risk methodology that delivers up to 60% cost reduction. To address low-power challenges, Spartan-3L™ reduced-power devices lower quiescent power consumption by up to 98% and include an exclusive Hibernate mode.

With all their cost and feature advantages, you can now use Spartan-3 FPGAs in higher volume than ever before. Plus, we make it easy to start your FPGA design immediately with the US $99 Spartan-3 Starter Kit.

The World's Lowest Cost per Gate and the Lowest Cost per I/O

The Spartan-3 FPGA family, the fifth generation in the groundbreaking Spartan™ series, offers a platform with a wide range of I/O and density options. This enables you to achieve fast time-to-market and low unit cost while avoiding the high risks of ASICs.

- **Advanced, Low-Cost Features**
  - Eight devices ranging from 50K to 5M system gates
  - Up to 1.8 Mbits of block RAM
  - From 63 to 784 I/Os with package and density migration
  - Digital clock management for high-speed design challenges
  - Embedded 18x18 multipliers for high-performance DSP applications
- **Spartan-3L Reduced-Power FPGAs**
  - Three devices with up to 98% lower power consumption
  - Exclusive Hibernate mode fits seamlessly with systems using power-management
- **Industry-Leading Design Tools and IP**
  - ISE design tools and ChipScope™ Pro system debugging environment shorten design and verification time
  - Web Power Tool and XPower offer accurate, detailed power estimation and analysis
  - 32-bit MicroBlaze™ and 8-bit PicoBlaze™ embedded processors with the easy-to-use Embedded Development Kit (EDK)
  - System Generator for DSP and DSP Intellectual Property (IP) cores for pushbutton DSP system development
  - Hundreds of pre-verified, pre-optimized IP cores and reference designs
- **Easy-to-Use, Low-Cost FPGA Development Systems**
  - Complete Spartan-3 Starter Kit, available for only $99 USD

Optimized Cost

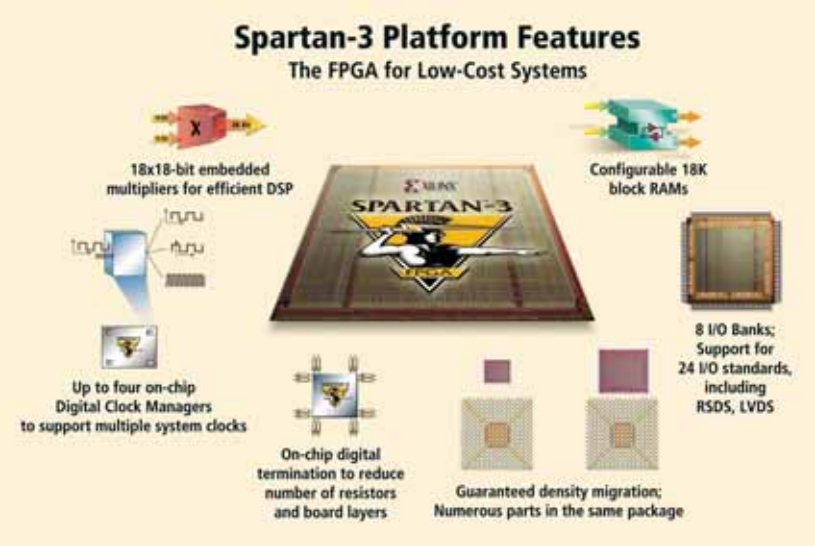
The Spartan-3 family provides the lowest cost per gate and lowest cost per I/O of any FPGA, and Spartan-3 EasyPath FPGAs deliver up to 60% further cost reduction with a conversion-free, no-risk methodology.

Full-Featured

Spartan-3 FPGAs add more value with numerous platform features like embedded 18x18 multipliers, up to 1.8 Mb of block RAM, and embedded 32-bit and 8-bit soft processors. In addition, digitally controlled impedance, digital clock managers, and 24 supported I/O standards solve board design challenges.

Reduced-Power Spartan-3L Devices

Three reduced-power Spartan-3L devices reduce quiescent power consumption by up to 98% to enable lower-cost cooling systems, smaller, less-expensive enclosures, and higher system reliability. Plus, an exclusive Hibernate mode fits seamlessly with systems using power-management.



Spartan-3 FPGA Family								
Spartan-3	**XC3S50**	**XC3S200**	**XC3S400**	**XC3S1000**	**XC3S1500**	**XC3S2000**	**XC3S4000**	**XC3S5000**
Spartan-3L	—	—	—	**XC3S1000L**	**XC3S1500L**	—	**XC3S4000L**	—
Spartan-3 EasyPath	—	—	—	—	**XCE3S1500**	**XCE3S2000**	**XCE3S4000**	**XCE3S5000**
System Gates	50K	200K	400K	1000K	1500K	2000K	4000K	5000K
Logic Cells	1,728	4,320	8,064	17,280	29,952	46,080	62,208	74,880
Block RAM Bits	72K	216K	288K	432K	576K	720K	1,728K	1,872K
Distributed RAM Bits	12K	30K	56K	120K	208K	320K	432K	520K
DCMs	2	4	4	4	4	4	4	4
Multipliers	4	12	16	24	32	40	96	104
I/O Standards	24	24	24	24	24	24	24	24
Max Single Ended I/O**	124	173	264	391	487	565	712	784

Package and I/O Offerings								
	XC3S50	**XC3S200**	**XC3S400**	**XC3S1000**	**XC3S1500**	**XC3S2000**	**XC3S4000**	**XC3S5000**
VQ100 14 x 14 mm	63	63						
TQ144 20 x 20 mm	97	97	97					
PQ208 28 x 28 mm	124	141	141					
FT256 17 x 17 mm		173	173	173*				
FG320 23 x 23 mm			221	221*	221*			
FG456 23 x 23 mm			264	333*	333*			
FG676 27 x 27 mm				391	487*	489		
FG900 31 x 31 mm						565	633*	633
FG1156 35 x 35 mm							712	784

* Also available in Spartan-3L

** See Package and I/O Offerings for Spartan-3L maximum values

Take the Next Step

Visit our website at **www.xilinx.com/spartan3** or call your local sales office or distributor for more information about Spartan-3 FPGAs. To start your FPGA design immediately, check out Spartan-3 development systems at **www.xilinx.com/s3boards**.

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FORTUNE 2004 100 BEST COMPANIES TO WORK FOR

XILINX® The Programmable Logic Company™

Xilinx Spartan™-3E FPGAs

The World's Lowest-Cost FPGAs for Gate-Centric Designs

Designers of gate-centric solutions face a common problem — increasing design functionality while also minimizing device costs. This has often meant sacrificing either features or cost-effectiveness.

The Spartan-3E FPGA family offers the low cost and platform features you're looking for, making it ideal for gate-centric programmable logic designs. Sparatan-3E is the seventh family in the groundbreaking low-cost Spartan Series and the third Xilinx family manufactured with advanced 90nm process technology. Spartan-3E FPGAs deliver up to 1.6 million system gates, up to 376 I/Os, and a versatile platform FPGA architecture with the lowest cost per-logic in the industry. This combination of state-of-the-art low-cost manufacturing and cost-efficient architecture provides unprecedented price points and value.

The features and capabilities of the Spartan-3E family are optimized for high-volume and low-cost applications and the Xilinx supply chain is ready to fulfill your production requirements. We're ready when you are.

Spartan-3E Low-Cost Features

The Spartan-3E family reduces system cost by offering the lowest cost-per-logic of any FPGA family, supporting the lowest-cost configuration solutions including commodity serial (SPI) and parallel flash memories, and efficiently integrating the functions of many chips into a single FPGA.

Advanced, Low-Cost Features

- Five devices with 100K to 1.6M system gates
- From 66 to 376 I/Os with package and density migration
- Up to 648 Kbits of block RAM and up to 231 Kbits of distributed RAM
- Up to 36 embedded 18x18 multipliers for high-performance DSP applications
- Up to eight Digital Clock Managers

Cost-Saving System Interfaces and Solutions

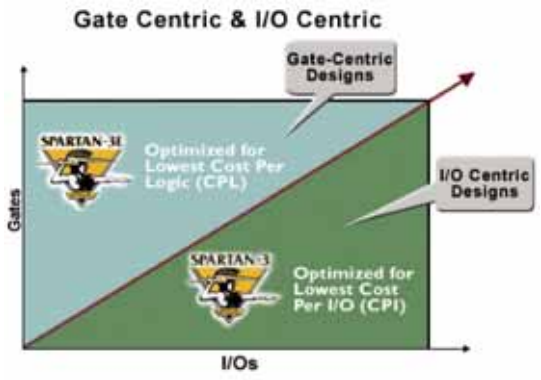
- Support for Xilinx Platform Flash as well as commodity serial (SPI) and byte-wide flash memory for configuration
- Easy-to-implement interfaces to DDR memory
- Support for 18 common I/O standards, including PCI 33/66, PCI-X, mini-LVDS, and RSDS

Industry-Leading Design Tools and IP

- ISE design tools to shorten design and verification time
- Hundreds of pre-verified, pre-optimized Intellectual Property (IP) cores and reference designs
- ChipScope Pro™ system-debugging environment

Easy-to-Use, Low-Cost FPGA Development Systems

- Complete Spartan-3E Starter Kit available for only $149 USD
- Includes XC3S500E FPGA, SPI Flash, 32Mb DDR memory and support for USB2.0
- Get more information about all Spartan-3™ Series development boards at **www.xilinx.com/s3eboards**

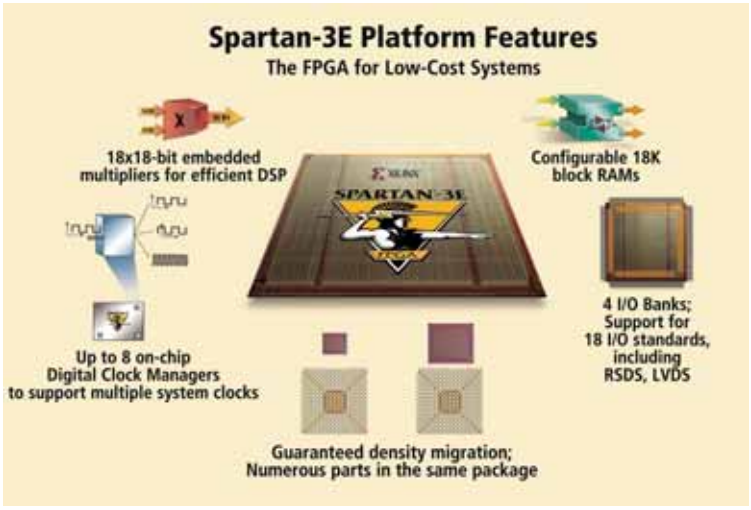


Spartan-3E FPGAs — Cost-Optimized Custom Logic for All Applications

Together, the Spartan-3E and Spartan-3 FPGA families provide the lowest-cost programmable solutions for designs from 50K to 5 million system gates and up to 784 I/Os. Each family is optimized to provide the best ratio of gates to I/O for your application; Spartan-3E is optimized for gate-centric applications and Spartan-3 is optimized for I/O-centric applications.

While Spartan-3 Series FPGA families deliver superior performance in digital consumer applications, the resulting advanced features and capabilities benefit all high-volume/low-cost applications.

	Spartan-3E FPGA Family				
	XC3S100E	XC3S250E	XC3S500E	XC3S1200E	XC3S1600E
System Gates	100K	250K	500K	1,200K	1,600K
Logic Cells	2,160	5,508	10,476	19,512	33,192
Block RAM Bits	72K	216K	360K	504K	648K
Distributed RAM Bits	15K	38K	73K	136K	231K
DCMs	2	4	4	8	8
Multipliers	4	12	20	28	36
I/O Standards	18	18	18	18	18
Max Single Ended I/O	108	172	232	304	376
Max Differential I/O Pairs	40	68	92	124	156
	Package and I/O Offerings				
	XC3S100E	XC3S250E	XC3S500E	XC3S1200E	XC3S1600E
VQ100 14 x14 mm	66	66			
CP132 8 x8 mm		92	92		
TQ144 20 x 20 mm	108	108			
PQ208 28 x 28 mm		158	158		
FT256 17 x 17 mm		172	190	190	
FG320 19 x 19 mm			232	250	250
FG400 21 x 21 mm				304	304
FG484 23 x 23 mm					376



Spartan-3E Low-Cost Features

Through the use of 90nm process technology, 300mm wafers, and application-driven architecture choices, the Spartan-3E family offers the lowest cost-per-logic in the industry and extends the use of FPGAs into volumes and applications previously reserved for mask-programmed ASICs. The typical volume to cross over from FPGAs to ASICs for production is now more than 250K units.

In addition to low unit costs, the Spartan-3E family includes many features to reduce overall system cost. For example, Spartan-3E devices add support for a commodity serial (SPI) and parallel flash memory to reduce configuration memory costs. Other Spartan-3E features reduce system cost by integrating the functions of many discrete chips into a single FPGA:

- PCI 33/66 compliance and PCI-X compatibility, support for mini-LVDS and RSDS I/O standards — eliminates discrete interface solutions
- Embedded Digital Clock Management — eliminates discrete DLLs/PLLs, phase shifters
- Embedded hardware multipliers — implements low-cost DSP

Take the Next Step

Visit our website www.xilinx.com/spartan3e or call your local sales office or distributor for more information about Spartan-3E FPGAs. To start your design immediately, download your free ISE WebPACK™ design tools at **www.xilinx.com/ise**. To begin evaluating Spartan FPGAs, order your hardware development board at **www.xilinx.com/s3eboards**

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CoolRunner™-II

Xilinx CoolRunner-II: RealDigital CPLDs

High performance and ultra-low power consumption with no compromises.

The CoolRunner™-II CPLD family utilizes our second-generation RealDigital technology to give you high performance, advanced features, and low power consumption, all at a very low price. Featuring a 100% digital core, up to 323 MHz performance, and low stand-by current, CoolRunner-II CPLDs offer a wide range of densities, plus abundant I/O, the flexibility to move from one density to another in the same package, and the lowest cost per I/O pin in the industry.

Xilinx RealDigital CPLDs eliminate the high-current sense amplifier technology traditionally used in CPLD products. The result is a scalable technology that is ideal for many high volume applications, such as PDAs, cell phones, routers, and high-speed Internet modems.

A Complete Programmable Solution

- **Up to 323 MHz performance** — High performance for leading-edge applications. Up to 500 MHz toggle rate with clock doubler.
- **Ultra-Low standby current** — The industry's lowest power consumption.
- **1.8 Volt device operation** — I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels to simplify multi-voltage system design.
- **A wide range of densities** — From 32 to 512 macrocells, to suit a broad range of applications.
- **Advanced system features** — Multiple I/O standards, clock management, and increased design security simplify your design.
- **Complete software support** — All Xilinx ISE software packages provide complete support for CoolRunner-II devices.
- **Advanced packaging** — Choose from Chip Scale (CSP), QFG, TQFP, PQFP, VQFP, PLCC, and fine line BGA packages for PC board space savings, cost optimization, and high performance. The world's smallest CPLD package, the 5 by 5 mm QFG32, is also available. All packages available in a Pb-Free option.
- **Easy In-System Programming (ISP)** — Support for IEEE 1532 In-System Programming and IEEE 1149.1 JTAG Boundary Scan testing.
- **Superior pin-locking** — Implement design updates without changing pinouts, minimize PC board layout changes and enable field upgradeability.

Advanced System Features

Advanced I/O Support

- **LVTTL and LVCMOS** for standard chip-to-chip interfacing.
- **SSTL and HSTL** for standard chip-to-memory interfacing.
- **DataGATE** disables unused pins to reduce power.
- **Bus Hold** keeps outputs in their last stable state, for further power reduction.
- **Input hysteresis (500mv)** conditions noisy and slow transitioning signals.

Superior Clock Management

- **DualEDGE Registers:** Enhances performance by doubling input clock switching frequency.
- **Clock Divider:** Improves power savings by dividing externally supplied global clocks by standard values.
- **CoolCLOCK:** Combines a clock divider and doubler to divide an incoming clock by two (reducing clocking power), and then doubling the clock at the macrocell.

Unparalleled Design Security

- **Four levels of design security** prevent accidental overwriting and pattern theft.

Free Reference Designs

- MP3 Player
- UARTs and bus controllers
- PicoBlaze microcontroller
- And many more

Software Tools

CoolRunner-II CPLDs are supported in all versions of the Xilinx Integrated Software Environment (ISE) which include ISE WebPACK™, and ISE Foundation™.

- **ISE WebPACK** is a free, downloadable desktop solution that offers HDL and ABEL synthesis and simulation, schematic entry, JTAG and third-party EDA support, and device support for all CPLD families (as well as Virtex™-4, Virtex-II Pro, Virtex-II, Virtex-E, Spartan™-3E, Spartan-3, Spartan-IIE, and Spartan-II)
- **ISE Foundation** is the full featured software environment that supports all of our current CPLD and FPGA families.

DOWNLOAD NOW

For additional information, please visit our website at:
www.xilinx.com/cr2

CoolRunner-II Family at a Glance

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
I/O Standards	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1	LVTTL,LVCMOS 15,18,25,33 SSTL2-1, SSTL3-1 HSTL-1
Max I/O	33	64	100	184	240	270
T_{PD}(ns)	3.8	4.6	5.7	5.7	7.1	7.1
I/O Banks	2	2	2	2	4	4
DualEDGE Registers	Yes	Yes	Yes	Yes	Yes	Yes
Input Hysteresis	Yes	Yes	Yes	Yes	Yes	Yes
DataGATE & Clock divide	—	—	Yes	Yes	Yes	Yes
Packages	QFG32 VQ44 PC44 CP56	 VQ44 PC44 QFG48 CP56 VQ100	 VQ100 CP132 TQ144	 VQ100 CP132 TQ144 PQ208 FT256	 TQ144 PQ208 FT256 FG324	 PQ208 FT256 FG324

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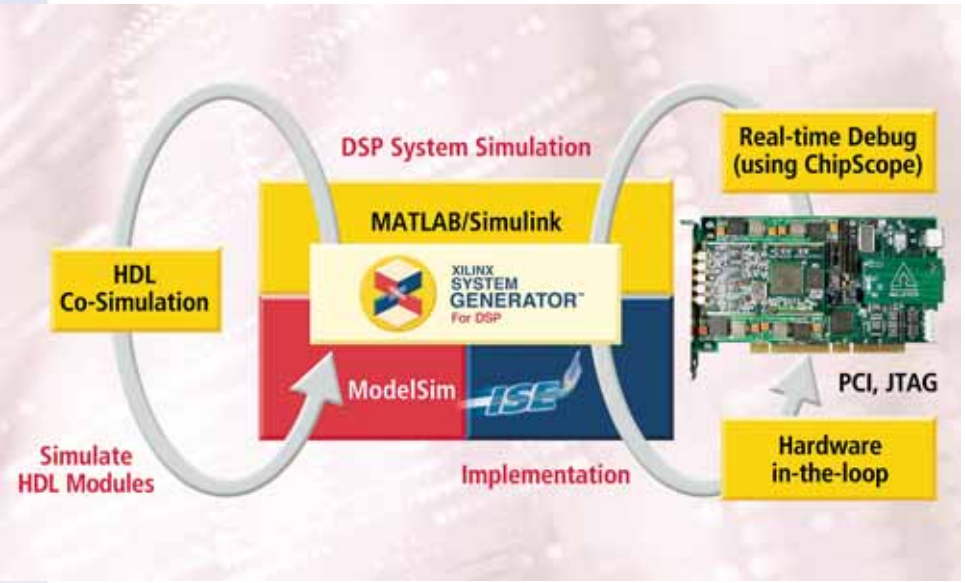
Push-button Performance using System Generator for DSP

Push-button bitstream generation from Simulink to FPGA

Xilinx FPGAs have become the preferred choice for many high-performance, programmable DSP applications. However, you may not be familiar with our FPGA design tools and processes. So, how do you make the best use of our DSP technology with the least amount of effort?

The System Generator for DSP tool allows you to easily target your high-performance DSP designs to Xilinx FPGAs, directly from the familiar MATLAB®/Simulink® environment of The MathWorks.

Using this platform, your designs will make efficient use of the Xilinx device architecture without the need for hardware description languages like VHDL or Verilog. With System Generator's hardware-in-the-loop co-simulation interfaces, you can import HDL code directly into Simulink, as well as accelerate your system-level simulations.



Get the DSP Advantage

System Generator for DSP is a software platform that uses Simulink to represent a high-level, abstract view of your DSP system. It then automatically maps your system to a predictable, highly efficient hardware implementation, enabling you to customize the Xilinx architecture to suit your DSP algorithm.

Model and Implement High-Performance DSP Systems

- **Create multi-rate and high-performance data paths** and develop 300 MSPS real-time processing systems, using our highest performance Virtex-II Pro™ Series FPGAs. For cost-sensitive DSP applications, you can implement programmable designs on Spartan™ Series FPGAs to get the industry's highest ratio of MACs per second per dollar.

Reduce Development Time and Cost

- **Accelerate and verify designs on actual hardware using hardware-in-the-loop.** This enables real-time verification on the actual FPGA, greatly accelerating simulation for complex designs – in some cases, from days to minutes.
- **Incorporate and simulate legacy designs using HDL co-simulation.** Bring in your existing HDL via the black box capability and use Mentor Graphics' ModelSim tool to simulate your legacy code. The link between Simulink and ModelSim is dynamic, allowing simulation data to pass between the two programs.
- **Simplify debug of your real-time system**
  By inserting special low-impact IP debugging cores directly into your System Generator design, you can debug and verify all the internal signals and nodes within your FPGA, capturing signals at or near system operating speeds.

A Powerful, High-level DSP Modeling Environment

System Generator for DSP provides bit-true and cycle-true Simulink libraries for DSP functions, math and digital logic operators, and memories. The co-simulation interfaces allow the hardware designer to seamlessly import HDL code into the system simulation, enabling a much closer coupling with the system architect.

- Block customization allows the user to apply MATLAB code to parameterize the Simulink model. System Generator also supports automatic translation of a hardware-centric subset of the MATLAB language into Simulink and synthesizeable HDL. This is especially useful for state machines and other control logic.
- Arithmetic abstraction automatically provides arbitrary precision fixed-point functions, including quantization and overflow.
- Simulation of double-precision, as well as fixed-point operation, lets the user determine the quantization error at any point.
- Interfaces to the Xilinx ISE environment and the Xilinx CORE Generator™ enables the use of our latest portfolio of hand crafted DSP algorithms when implemented as IP cores.

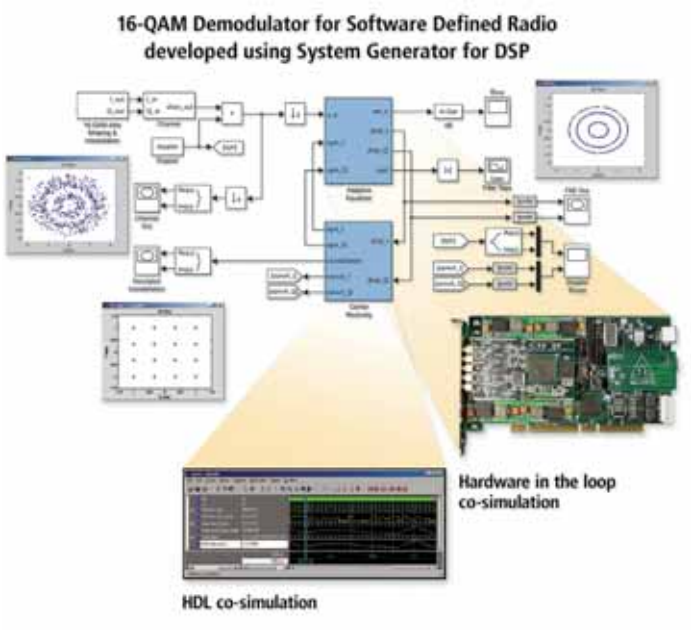
Industry's Best Productivity

The System Generator for DSP generates highly optimized VHDL code and IP cores with the hierarchy preserved. It also generates a number of helpful files, including:

- ISE project generation to simplify design flow
- HDL testbench and test vectors along with .do files for simulation
- Constraint files (.xcf, .ncf) for timing constraint information and I/O allocation
- ModelSim script files for behavioral simulation
- Mixed-language support for Verilog, supporting a dual synthesis flow
- Project files for Synplify Pro, Leonardo Spectrum, and Xilinx XST (a part of the ISE Foundation™ software)
- Multiple demos/tutorials such as 16 QAM demodulator, discrete wavelet transform and Costas loop

System Generator for DSP comes with an unprecedented range of award-winning services and support such as DSP education classes, DSP design services, on-site Xilinx DSP Specialists (via the Titanium service), and personalized web support. Visit **www.xilinx.com/dsp**

Design Example:



Access to Key Device Features

System Generator for DSP is part of the XtremeDSP™ solution which also includes IP cores, DSP classes, DSP boards and the industry's leading FPGAs, with features such as:

- Up to 556 embedded 18x18 multipliers, operating at speeds of 300MHz
- Up to 10 Mbits of on-chip block memory
- SRL16 shift-register logic
- Optional control signals such as clock enable and reset

Take the Next Step

The Xilinx System Generator for DSP is fast, easy to use, and very powerful. (Part # DS-SYSGEN-4SL-PC). For the full details, and access to a **60 day evaluation**, go to: **www.xilinx.com/systemgenerator_dsp**. Or, you can place your order at: **www.xilinx.com/store**. Register for our DSP training classes and training bundle (Part # DS-SYSGEN-4SL-T) at: **www.xilinx.com/support/training/training.htm**

VIRTEX-II PRO™ VIRTEX-II™ SPARTAN-3 XtremeDSP™ Push-button Performance

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Xilinx PCI Express Solution

PCI Express has emerged as the next generation technology replacing PCI. It provides higher performance and increased bandwidth while maintaining the flexibility and familiarity of PCI. Despite the advantages of PCI Express, design challenges associated with this new and complex protocol will directly affect time-to-market.

Xilinx provides a range of FPGA solutions to meet the needs of a variety of PCI Express applications. The breakthrough Virtex-4 and Virtex-II Pro FPGAs offer a fully integrated solution for applications with limited board real estate, utilizing built-in transceivers to implement the entire PCI Express interface in a single device. Alternatively, the low-cost Spartan-3 and Spartan-3E FPGA families can be used along with an external PHY device via the PHY Interface for PCI Express (PIPE).

The Xilinx PCI Express Advantage

The Xilinx PCI Express solution includes the PCI Express 1-lane, 4-lane and 8-lane endpoint IP cores for use with the Virtex-4 and Virtex-II Pro FPGA devices and the PCI Express PIPE 1-lane endpoint IP core for use with the Spartan-3 and Spartan-3E FPGA devices.

High Performance – The RocketIO™ Multi-Gigabit Transceivers (MGTs) on the Virtex-4 and Virtex-II Pro FPGAs give this core a 2.5 Gbps line speed in 1-lane configuration, 10 Gbps line speed in 4-lane configuration and 20 Gbps line speed in 8-lane configuration.

Low-Cost – The Xilinx PCI Express PIPE endpoint core is a high-bandwidth scalable and reliable IP building block for use with the Spartan-3 and Spartan-3E FPGAs. It is ideally suited for a broad range of high volume computing and communications applications requiring a low cost and 100% compliance with the PCI Express Base Specification v1.1a.

Flexibility – The inherently programmable nature of the FPGA allows you to continually modify your design as your performance and interoperability requirements evolve, reducing your risk in adopting the new PCI standard.

General Features

- High-performance, highly flexible, scalable, reliable, and general purpose I/O core
  - Compliant to the PCI Express Base Specification v1.1a
  - Compatible with current PCI software model
- Fully compliant with PCI Express transaction ordering rules
- Supports removal of corrupted packets for error detection and recovery
- Design verified by Xilinx proprietary test bench

PCI Express 1-Lane, 4-Lane and 8-Lane Endpoint Cores

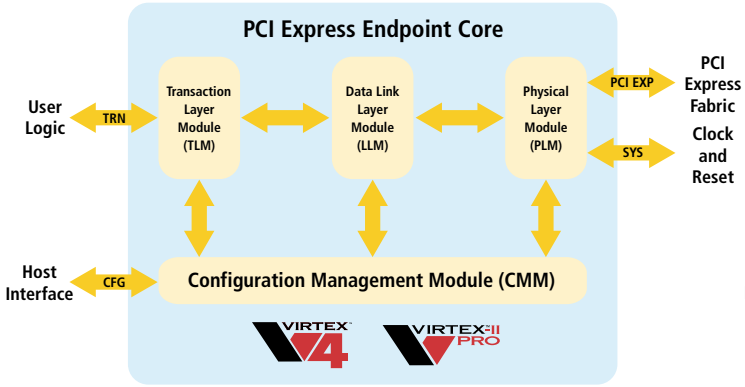
- Incorporates Xilinx Smart-IP™ technology to guarantee critical timing
- Uses the RocketIO Multi-Gigabit Transceivers on the Virtex-4 and Virtex-II Pro FPGA devices to achieve high transceiver capability
  - 2.5 Gbps per lane line speed
  - Supports 1-lane, 4-lane and 8-lane operation (8-lane on Virtex-4 only)
  - Elastic buffers and clock compensation
  - Automatic clock data recovery
- 8b/10b encode and decode
- Offers standardized user interface
  - Easy-to-use packet-based protocol
  - Full-duplex communication
  - Back-to-back transactions enable greater link bandwidth utilization
  - Supports flow control of data and discontinuation of an in-process transaction in the transmit direction
  - Supports flow control of data in the receive direction
  - Transaction traffic class selection enabled
  - Support for automatically handling of error forwarded packets
  - Automatically decodes and removes error forwarding packet indicator from received data
  - Forward compatible with future link widths
- Supports a maximum transaction payload of up to 4096 bytes
- Bandwidth scalability with frequency and/or interconnect width

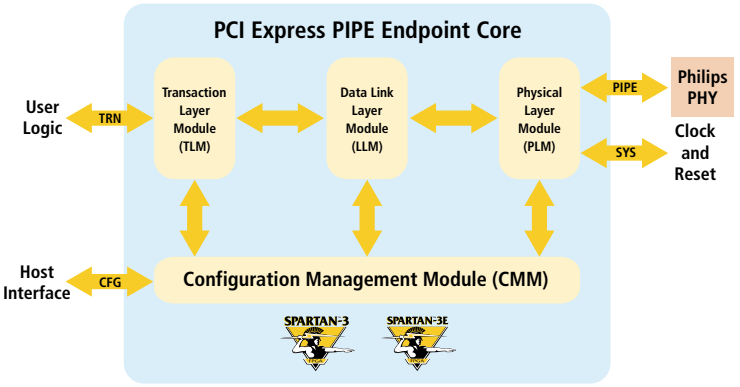
PCI Express PIPE 1-Lane Endpoint Core

- Six individually programmable/configurable BARs and expansion ROM BAR
- Supports MSI and INTX emulation
- 32-Bit internal datapath
- Compatible with PCI/PCI-Express power management functions
  - Active state power management (ASPM)
  - Programmed power management (PPM)
- Used in conjunction with Philips PX1011A PCI Express standalone PHY to achieve high transceiver capability
  - 2.5 Gbps line speed
  - Elastic buffers and clock compensation
  - Automatic clock and data recovery
  - 8b/10b encode and decode
- Offers Xilinx-standardized easy-to-use LocalLink interface
  - Packet-based full-duplex communication
  - Back-to-back transactions enable greater link bandwidth utilization
  - Enables flow control of data and discontinuance of an in-process transaction in the transmit direction
  - Enables flow control of data in the receive direction
  - Automatically decodes and removes error forwarding packet indicator from received data
- Supports a maximum transaction payload of up to 512 bytes

Get Your PCI Express Solution Today

To learn more about the Xilinx PCI Express solution or to download the core, visit **www.xilinx.com/pciexpress.**





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	Feature	*ISE WebPACK™*	*ISE BaseX*	*ISE Foundation™*
Devices*	Virtex™ Series	**Virtex-E:** XCV50E -XCV300E **Virtex-II:** XC2V40 - XC2V250 **Virtex-II Pro:** XC2VP2 **Virtex-4:** **LX:** XC4VLX15, XC4VLX25	**Virtex:** XCV50 - XCV600 **Virtex-E:** XCV50E - XCV600E **Virtex-II:** XC2V40 - XC2V500 **Virtex-II Pro:** XC2VP2 – XC2VP7 **Virtex-4:** **LX:** XC4VLX15, XC4VLX25 **SX:** XC4VSX25 **FX:** XC4VFX12	All
	Spartan™ Series	**Spartan-II:** All **Spartan-IIE:** XC2S50E – XC2S300E **Spartan-3:** XC3S50 – XC3S1500 **Spartan-3E:** XC3S100E – XC3S500E **Spartan-3L:** XC3S1000L, XC3S1500L	**Spartan-II:** All **Spartan-IIE:** All **Spartan-3:** XC3S50 – XC3S1500 **Spartan-3E:** All **Spartan-3L:** XC3S1000L, XC3S1500L	**Spartan-II/IIE:** All **Spartan-3:** All **Spartan-3E:** All **Spartan-3L:** All
	CoolRunner™ XPLA3 CoolRunner-II CoolRunner-IIA	All	All	All
	XC9500 Series	All	All	All
Design Entry	Schematic and HDL Editor	Yes	Yes	Yes
	State Diagram Editor	Microsoft Windows only	Microsoft Windows only	Microsoft Windows only
	CORE Generator™	No	Yes	Yes
	RTL & Technology Viewers	Yes	Yes	Yes
	PACE (Pinout & Area Constraint Editor)	Yes	Yes	Yes
	Architecture Wizards	Yes	Yes	Yes
	Xilinx System Generator for DSP	No	Sold as an Option	Sold as an Option
Embedded System Design	Embedded Design Kit (EDK)	No	Sold as an Option	Sold as an Option
Synthesis	XST – Xilinx Synthesis Technology	Yes	Yes	Yes
	Mentor Graphics Leonardo Spectrum	Integrated Interface (EDIF Interface on Linux)	Integrated Interface (EDIF Interface on Linux)	Integrated Interface (EDIF Interface on Linux)
	Mentor Graphics Precision RTL	Integrated Interface	Integrated Interface	Integrated Interface
	Mentor Graphics Precision Physical	EDIF Interface	EDIF Interface	EDIF Interface
	Synopsys DC-FPGA Compiler	EDIF Interface	EDIF Interface	EDIF Interface
	Synplicity Synplify/Pro	Integrated Interface	Integrated Interface	Integrated Interface
	Synplicity Amplify Physical Synthesis	EDIF Interface	EDIF Interface	EDIF Interface
	ABEL	CPLD (Microsoft Windows only)	CPLD (Microsoft Windows only)	CPLD (Microsoft Windows only)
Implementation	FloorPlanner	Yes	Yes	Yes
	PlanAhead™	No	Sold as an Option	Sold as an Option
	Timing Driven Place & Route	Yes	Yes	Yes
	Modular Design	No	Yes	Yes
	Incremental Design	Yes	Yes	Yes
	Timing Improvement Wizard	Yes	Yes	Yes
Programming	iMPACT / System ACE™ / CableServer	Yes	Yes	Yes
Board Level Integration	IBIS, STAMP, and HSPICE** models	Yes	Yes	Yes
	ELDO Models** (MGT only)	Yes	Yes	Yes
Verification	ChipScope™ Pro	Sold as an Option	Sold as an Option	Sold as an Option
	Graphical Testbench Editor	Microsoft Windows only	Microsoft Windows only	Microsoft Windows only
	ISE Simulator Lite	No	Yes	Yes
	ISE Simulator	No	No	Sold as an Option
	ModelSim XE III Starter	Yes	Yes	Yes
	ModelSim XE III	Sold as an Option	Sold as an Option	Sold as an Option
	Static Timing Analyzer	Yes	Yes	Yes
	FPGA Editor with Probe	No	Yes	Yes
	ChipViewer	Yes	Yes	Yes
	XPower (Power Analysis)	Yes	Yes	Yes
	SMARTModels for PowerPC™ and RocketIO™	No	Yes	Yes
Platforms		Microsoft Windows 2000, XP Red Hat Enterprise Linux 3 (32-bit)	Microsoft Windows 2000, XP Red Hat Enterprise Linux 3 (32-bit)	Microsoft Windows 2000, XP Sun Solaris 2.8 or 2.9, Red Hat Enterprise Linux 3 (32 and 64-bit)

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Function	Vendor Name	Virtex-4	Virtex-II Pro	Virtex-II	Virtex-E	Spartan-3	Spartan-IIE	Spartan-II	Device Utilization	Performance MHz	Device
Audio, Video and Signal Processing											
Accumulator	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Adder Subtracter	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Burst Locked PLL (BURST_PLL)	Pinpoint Solutions, Inc.		V-IIP	V-II		S-3	S-IIE		13%	70	XC2V1000-6
Cascaded Integrator Comb (CIC) Filter	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II			
Color Space Converter, RGB2YCrCb (CSC)	CAST, Inc.			V-II	V-E		S-IIE	S-II	29%	96	XC2S50E-7
Compact Video Controller (logiCVC)	Xylon d.o.o.			V-II				S-II	35%	88	XC2V250-4
Complex Multiplier	Xilinx	V-4	V-IIP	V-II		S-3			0%	445	XC4VSX25-11
CRT Controller (C6845)	CAST, Inc.			V-II	V-E		S-IIE	S-II	47%	134.7	XC2V80-5
Divider, Pipelined	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE	S-II			
FIR Filter using DPRAM	eInfochips Pvt. Ltd.			V-II	V-E		S-IIE	S-II	26%	40	XC2V250-5
FIR Filter, Distributed Arithmetic (DA)	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II			
FIR Filter, MAC	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	16%		XC2V250
FIR Filter, Parallel Distributed Arithmetic	eInfochips Pvt. Ltd.			V-II	V-E		S-IIE	S-II	45%	90	XC2V250-5
Floating Point Adder (DFPADD)	Digital Core Design			V-II				S-II	0%	66	XC2V250-5
Floating Point Comparator (DFPCOMP)	Digital Core Design			V-II				S-II	0%	91	XC2V80-5
Floating Point Divider (DFPDIV)	Digital Core Design			V-II				S-II	0%	53	XC2V250-5
Floating Point Multiplier (DFPMUL)	Digital Core Design			V-II	V-E			S-II	0%	74	XC2V250-5
Floating Point Square Root Operator (DFPSQRT)	Digital Core Design			V-II	V-E			S-II	0%	66	XC2V250-5
Floating Point to Integer Converter (DFP2INT)	Digital Core Design			V-II				S-II	0%	66	XC2V250-5
Floating-Point Cores (Quixilica QxFP)	QinetiQ Limited		V-IIP	V-II	V-E	S-3	S-IIE		7%	263	XC2VP7-7
FPU for Microblaze (Quixilica)	QinetiQ Limited		V-IIP	V-II					52%	105	XC2V1000-4
Integer to Floating Point Converter (DINT2FP)	Digital Core Design			V-II				S-II	0%	73	XC2V250-5
LFSR, Linear Feedback Shift Register	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Longitudinal Time Code Generator	Deltatec S.A.		V-IIP	V-II		S-3	S-IIE		8%	27	XC3S50-4
Multiply Accumulator (MAC)	Xilinx	V-4	V-IIP	V-II		S-3	S-IIE	S-II			
Multiply Generator	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II			
NTSC Color Separator (NTSC-COSEP)	Pinpoint Solutions, Inc.		V-IIP	V-II		S-3	S-IIE		92%	27	XC2V1000-6
Sine Cosine Look Up Table	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	12%	270	XC2V40-6
Twos Complementer	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Compression Codecs											
Discrete Cosine Transform (eDCT)	eInfochips Pvt. Ltd.			V-II	V-E		S-IIE	S-II	35%	83	XC2V1000-5
Discrete Cosine Transform, 2D Inverse (IDCT)	CAST, Inc.			V-II	V-E			S-II	45%	95	XC2V500-5
Discrete Cosine Transform, Combined 2D Forward/Inverse (DCT_FI)	CAST, Inc.			V-II	V-E			S-II	65%	95	XC2V500-5
Discrete Cosine Transform, Forward 2D (DCT)	CAST, Inc.			V-II	V-E			S-II	42%	83	XC2V500-5
Discrete Cosine Transform, forward/inverse 2D (DCT/IDCT 2D)	Barco-Silex			V-II	V-E			S-II	77%	133.6	XC2V250-5
Discrete Wavelet Transform (BA113FDWT)	Barco-Silex		V-IIP	V-II		S-3			36%	161	XC2VP20-6
Discrete Wavelet Transform, Combined 2D Forward/Inverse (RC_2DDWT)	CAST, Inc.			V-II	V-E			S-II	55%	95	XC2V500-5
Discrete Wavelet Transform, Inverse (BA114IDWT)	Barco-Silex		V-IIP	V-II		S-3			35%	122	XC2VP20-6
Discrete Wavelet Transform, Line-based programmable forward (LB_2DFDWT)	CAST, Inc.			V-II	V-E			S-II	72%	51	XC2V500-5
Huffman Decoder (HUFFD)	CAST, Inc.			V-II	V-E		S-IIE	S-II	22%	25	XC2V1000-5
JPEG Fast Codec (JPEG_FAST_C)	CAST, Inc.		V-IIP	V-II	V-E	S-3			78%	47.7	XC3S1000-4
JPEG, 2000 Decoder (BA111JPEG2000D)	Barco-Silex		V-IIP	V-II		S-3			20%	50	XC3S4000-5
JPEG, 2000 Encoder (BA112JPEG2000E)	Barco-Silex		V-IIP	V-II		S-3			23%	56	XC3S4000-4
JPEG, 2000 Encoder (JPEG2K_E)	CAST, Inc.		V-IIP	V-II	V-E				90%	106	XC2V3000-6
JPEG, Fast color image decoder (FASTJPEG_C DECODER)	Barco-Silex			V-II	V-E				78%	56	XC2V1000-4

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Function	Vendor Name	Virtex-4	Virtex-II Pro	Virtex-II	Virtex-E	Spartan-3	Spartan-IIE	Spartan-II	Device Utilization	Performance MHz	Device
JPEG, Fast Decoder (JPEG_FAST_D)	CAST, Inc.		V-IIP	V-II	V-E		S-IIE		68%	106	XC2V1000-6
JPEG, Fast Encoder (JPEG_FAST_E)	CAST, Inc.		V-IIP	V-II	V-E				69%	114	XC2V1000-6
JPEG, Fast gray scale image decoder (FASTJPEG_BW DECODER)	Barco-Silex			V-II	V-E				68%	73	XC2V1000-4
JPEG, Motion Codec V1.0 (CS6190)	Amphion Semiconductor, Ltd.		V-IIP	V-II		S-3	S-IIE		80%	27	XC3S1000-4
JPEG, Motion Decoder (CS6150)	Amphion Semiconductor, Ltd.		V-IIP	V-II		S-3			50%	58	XC3S1000-5
JPEG, Motion Encoder (CS6100)	Amphion Semiconductor, Ltd.		V-IIP	V-II	V-E	S-3	S-IIE		47%	46	XC3S1000-4
Motion JPEG Decoder (JPEG Decoder)	4i2i Communications Ltd.		V-IIP	V-II	V-E	S-3	S-IIE		69%	50	XC3S400-4
Motion JPEG Encoder (JPEG Encoder)	4i2i Communications Ltd.		V-IIP	V-II	V-E	S-3	S-IIE		76%	40	XC3S400-4
MPEG-2 HDTV I & P Encoder (DV1 HDTV)	Duma Video, Inc.			V-II					39%	111	XC2V3000-5
MPEG-2 SDTV I & P Encoder (DV1 SDTV)	Duma Video, Inc.			V-II					77%	108	XC2V1500-5
MPEG-2 Video Decoder (CS6651)	Amphion Semiconductor, Ltd.		V-IIP	V-II		S-3			66%	50	XC3S1000-5
MPEG-4 Video Compression Decoder	4i2i Communications Ltd.		V-IIP	V-II		S-3			39%	54	XC3S1000-4
MPEG-4 Video Compression Encoder	4i2i Communications Ltd.		V-IIP	V-II		S-3			18%	62	XC3S1000-4
Communications											
8b/10b Decoder	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		160	XC2V40-5
8b/10b Encoder	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		160	XC2V40-5
Convolutional Encoder	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	10%	26	XC2V40-6
CORDIC	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Digital Down Converter (DDC)	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II	47%	116	XC2V500-5
Digital Up Converter (DUC)	Xilinx		V-IIP	V-II		S-3			18%	117	XC3S1000 - 5
Direct Digital Synthesizer (DDS)	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	12%	245	XC2V80-6
DOCSIS ITU-T J.83 Modulator, Annex A/C	Xilinx		V-IIP	V-II		S-3			9%		XC3S1000
DOCSIS ITU-T J.83 Modulator, Annex B	Xilinx		V-IIP	V-II		S-3			12%		XC3S1000
DVB Satellite Modulator (MC-XIL-DVBMOD)	Memec Design			V-II	V-E			S-II	59%	45	XC2V80-4
Fast Fourier Transform	Xilinx	V-4	V-IIP	V-II		S-3					
FFT, Pipelined (Vectis HiSpeed)	RF Engines, Ltd.		V-IIP	V-II		S-3				200	XCV2P4-6
FFT, Pipelined (Vectis-QuadSpeed)	RF Engines, Ltd.		V-IIP	V-II		S-3				200	XCV2P20-6
FFT/IFFT for Virtex-II, 1024-Point Complex	Xilinx			V-II					62%	41us, 100	XC2V500
FFT/IFFT for Virtex-II, 16-Point Complex	Xilinx			V-II					37%	123ns 130	XC2V500
FFT/IFFT for Virtex-II, 256-Point Complex	Xilinx			V-II					54%	7.7us, 100	XC2V500
FFT/IFFT for Virtex-II, 64-Point Complex	Xilinx			V-II					38%	1.9us, 100	XC2V500
FFT/IFFT, 1024-Point Complex	Xilinx				V-E						
FFT/IFFT, 16-Point Complex	Xilinx			V-II	V-E						
FFT/IFFT, 256-Point Complex	Xilinx			V-II	V-E						
FFT/IFFT, 32-Point Complex	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II	29%	110	XC2V500-6
FFT/IFFT, 64-, 256-, 1024-Point Complex	Xilinx		V-IIP	V-II		S-3			32%	140	XC2V1500-6
FFT/IFFT, 64-Point Complex	Xilinx				V-E						
High Data Rate Demodulator (Zaltys HDRM-D)	Silicon Infusion Limited		V-IIP	V-II		S-3			66%	100	XC3S2000-5
Interleaver/De-interleaver	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	30%	208	XC2V40-6
Reed Solomon Decoder	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	40%	98	XC2V250-6
Reed Solomon Decoder (MC-XIL-RSDEC)	Memec Design			V-II			S-IIE	S-II	95%	52	XC2S100E-6
Reed Solomon Encoder	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	42%	180	XC2V40-6
Reed Solomon Encoder (MC-XIL-RSENC)	Memec Design			V-II			S-IIE	S-II	12%	86	XC2S50E-6
Reed-Solomon Decoder (RSDX1)	ASICS World Service, Ltd.		V-IIP	V-II	V-E	S-3	S-IIE	S-II	81%	125	XC2VP4-7
Reed-Solomon Encoder (RSEX1)	ASICS World Service, Ltd.		V-IIP	V-II	V-E	S-3	S-IIE	S-II	12%	154	XC2VP2-7
Turbo Decoder, DVB-RCS (S2000)	iCoding Technology, Inc.			V-II	V-E				44%	71	XC2V2000-5
Turbo Decoder, DVB-RCS (TC1000)	TurboConcept			V-II	V-E				65%	75	XC2V1000-6
Turbo Encoder, DVB-RCS (S2001)	iCoding Technology, Inc.			V-II	V-E				2%	69	XC2V2000-5

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Function	Vendor Name	Virtex-4	Virtex-II Pro	Virtex-II	Virtex-E	Spartan-3	Spartan-IIE	Spartan-II	Device Utilization	Performance MHz	Device
Viterbi Decoder, General Purpose	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	38%	128	XC2V500-5
Viterbi Decoder, IEEE 802-compatible	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II	35%	157	XC2V500-5
Bus, Memory & Network Interfaces											
1 Gigabit Ethernet MAC w/PLB interface	Xilinx	V-4	V-IIP							125	Virtex-II Pro (-6)
10/100 Ethernet MAC Lite w/OPB interface	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II		125	XC2V80-5
10/100 Ethernet MAC w/OPB interface	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II		125	XC2V80-5
10/100 Ethernet MAC w/PLB interface	Xilinx		V-IIP							125	Virtex-II Pro (-6)
1394a Link Layer Controller (C1394A)	CAST, Inc.		V-IIP	V-II		S-3				100	XC2VP7-7
1G/2G Fibre Channel	Xilinx	V-4	V-IIP						10%	53.125	XC2VP50-5
ATA Host Controller (HCL ATA)	HCL Technologies, Ltd.		V-IIP	V-II		S-3	S-IIE			100	XC3S400-4
Block Memory, Dual-Port	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Block Memory, Single-Port	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
BRAM Controller w/LMB interface	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE	S-II		125	XC2V80-5
BRAM Controller w/OPB interface	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		125	XC2V80-5
BRAM Controller w/PLB interface	Xilinx	V-4	V-IIP							150	Virtex-II Pro (-6)
BSP Generator (SW only)	Xilinx	V-4	V-IIP							150	Virtex-II Pro (-6)
Content Addressable Memory (CAM)	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Distributed Memory	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
Double Data Rate (DDR) Synchronous DRAM (SDRAM) Controller w/OPB Interface	Xilinx	V-4	V-IIP	V-II		S-3					
Ethernet 1000BASE-X PCS/PMA	Xilinx	V-4	V-IIP						5%-15%	1.25 Gbps	XC2VP4
Ethernet 1000BASE-X PCS/PMA	Xilinx	V-4	V-IIP						5%-15%	1.25 Gbps	XC2VP4
Ethernet MAC, 1 Gigabit Full duplex with GMII	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE		23%	125 (GMII) or 1.25 Gbps	XC2V1000-4
Ethernet MAC, 1 Gigabit Half/Full duplex with GMII	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE		23%	125 (GMII) or 1.25 Gbps	XC2V1000-4
Ethernet MAC, 10 Gigabit Full Duplex with XGMII or XAUI	Xilinx	V-4	V-IIP	V-II					25%	156.25 DDR for XGMII	XC2V3000-5
Ethernet MAC, 10/100	Zuken, Inc.			V-II	V-E				52%	25	XC2V1000-4
Ethernet MAC, 10/100 (MAC)	CAST, Inc.		V-IIP	V-II		S-3	S-IIE		74%	115	XC2V500-6
Ethernet MAC, 10G (XGEMAC)	GDA Technologies, Inc.		V-IIP	V-II					34%	156.2	XC2VP50-6
Ethernet MAC, 1Gigabit (MAC-1G)	CAST, Inc.		V-IIP	V-II					100%	135	XC2VP4-7
Ethernet PCS, 10G (MC-XIL-10GEPCS)	Memec Design			V-II					62%	85	XC2V3000-5
External Memory Controller (EMC) w/OPB interface (Includes support for Flash, SRAM, ZBT, System ACE)	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		125	XC2V80-5
External Memory Controller (EMC) w/PLB interface (Includes support for Flash, SRAM, ZBT, System ACE)	Xilinx	V-4	V-IIP							150	Virtex-II Pro (-6)
FIFO, Asynchronous	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
FIFO, Synchronous	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II			
I2S Receiver (CWda10)	Coreworks, Lda	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	5%	145	XC3S50-4
I2S Transmitter (CWda06)	Coreworks, Lda	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	11%	136	XC3S50-4
PCI 32-bit Master Interface (PCI-M32)	CAST, Inc.		V-IIP	V-II		S-3	S-IIE		15%	33	XC2VP2-5
PCI 32-Bit Multifunction Target Interface (PCI-TMF)	CAST, Inc.		V-IIP	V-II		S-3	S-IIE		14%	33	XC3S200-4
PCI 32-bit Target Interface (PCI-T32)	CAST, Inc.		V-IIP	V-II		S-3	S-IIE		8%	33	XC3S200-4
PCI 64-bit/66-MHz master/target interface (EC240)	Eureka Technology			V-II	V-E				22%	66	XC2V1000-5
PCI Arbiter w/OPB Interface	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		150	Virtex-II Pro (-6)
PCI Express Core (PExCore-254)	NitAl Consulting Services, Inc.		V-IIP			S-3				125	XC2VP40-6-6
PCI Express Endpoint Core (x1, x4)	Xilinx	V-4	V-IIP							Up to 10 Gbps	XC2VP50-6
PCI Express X 1, Xilinx PCI Express scalable endpoint LogiCORE	Xilinx		V-IIP						25%	31.25	XC2VP70 or larger
PCI Express X 4, Xilinx PCI Express scalable endpoint LogiCORE	Xilinx		V-IIP						25%	125	XC2VP20 or larger

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Function	Vendor Name	Virtex-4	Virtex-II Pro	Virtex-II	Virtex-E	Spartan-3	Spartan-IIE	Spartan-II	Device Utilization	Performance MHz	Device
PCI Express x1 eXPIPE I/F Protocol Layer Endpoint LogiCORE	Xilinx	Q205				Q205	Q205		~5KLUT	62.5	S400-5 or larger
PCI, 64-bit Master Interface (PCI-M64)	CAST, Inc.		V-IIP	V-II			S-IIE		6%	66	XC2VP4-5
PCI, 64-bit Target Interface (PCI-T64)	CAST, Inc.		V-IIP	V-II			S-IIE		24%	66	XC2VP2-7
PCI32 Interface Design Kit (DO-DI-PCI32-DKT)	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE	S-II	6%	66	XC2V1000-5
PCI32 Interface, IP Only (DO-DI-PCI32-IP)	Xilinx		V-IIP	V-II	V-E	S-3	S-IIE	S-II	6%	66	XC2V1000-5
PCI32 Single-Use License for Spartan (DO-DI-PCI32-SP)	Xilinx					S-3	S-IIE	S-II	12%	66	XC2S200-6
PCI64 & PCI32, IP Only (DO-DI-PCI-AL)	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II	6 - 7%	66	XC2V1000-5
PCI64 Interface Design Kit (DO-DI-PCI64-DKT)	Xilinx	V-4	V-IIP	V-II	V-E		S-IIE	S-II	7%	66	XC2V1000-5
PCI64 Interface, IP Only (DO-DI-PCI64-IP)	Xilinx		V-IIP	V-II	V-E		S-IIE	S-II	7%	66	XC2V1000-5
PCI-PCI Bridge (EP440)	Eureka Technology		V-IIP	V-II		S-3	S-IIE		48%	33	XC2S400E-7
PCI-X 64/133 Interface for Virtex-II (DO-DI-PCIX64-VE)	Xilinx	V-4	V-IIP	V-II					30%	100	XC2V1000-5
PCI-X 64/66 Interface for Virtex-E (DO-DI-PCIX64-VE).	Xilinx				V-E				30%	66	XCV300E-8
PCI-X Arbiter	SoC Solutions, LLC		V-IIP	V-II	V-E		S-IIE		8%	110	XC2VP2-6
PCI-X Interface (NWL PCI-X)	Northwest Logic		V-IIP	V-II					11%	133	XC2VP30-7
RLDRAM Memory Controller	Avnet Design Services			V-II					46%	200	XC2V1000-6
SDRAM Controller , DDR (DDR-XS-XILINX)	Array Electronics	V-4	V-IIP	V-II		S-3			12%	210	XC2VP4-6
SDRAM Controller w/OPB interface	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		125	XC2V80-5
SDRAM Controller w/PLB interface	Xilinx	V-4	V-IIP							150	Virtex-II Pro (-6)
SDRAM Controller, DDR (EP525)	Eureka Technology		V-IIP	V-II		S-3	S-IIE		16%	83	XC3S400-4
SDRAM Controller, DDR (MC-XIL-SDRAMDDR)	Memec Design			V-II	V-E			S-II	7%	133	XC2V1000-5
SDRAM Controller, DDR (NW)	Northwest Logic		V-IIP	V-II		S-3	S-IIE		11%	133	XC3S1000-4
SDRAM Controller, SDR (NW)	Northwest Logic		V-IIP	V-II		S-3	S-IIE		9%	133	XC3S1000-4
SDRAM Controller, SDR (SDR-XS-XILINX)	Array Electronics	V-4	V-IIP	V-II		S-3	S-IIE		5%	200	XC2VP7-6
Serial ATA I/II Host Controller (SATA_H1)	ASICS World Service, Ltd.		V-IIP	V-II		S-3			62%	145	XC2VP4-7
Smart Card Interface (HCLT SCI)	HCL Technologies, Ltd.	V-4	V-IIP	V-II	V-E	S-3	S-IIE		7%	100	XC3S1000-4
Tri-Mode Ethernet MAC (10/100/1000)	Xilinx	V-4	V-IIP	V-II		S-3			11-18%	125	XC2VP20
USB 2.0 Device Controller (FUSB200)	Faraday Technology Corporation			V-II					35%	30	XC2V3000-5
USB 2.0 Function Controller (CUSB2)	CAST, Inc.		V-IIP	V-II	V-E	S-3	S-IIE		55%	50	XC2VP4-7
USB 2.0 Function Controller (USB2_DEV)	ASICS World Service, Ltd.		V-IIP	V-II	V-E	S-3	S-IIE	S-II	63%	200	XC2VP4-6
USB 2.0 On-The-Go (USB2_OTG)	ASICS World Service, Ltd.		V-IIP	V-II	V-E	S-3	S-IIE		85%	200	XC2VP4-6
USB Function Controller with On-Chip Peripheral Bus (CUSB_OPB)	CAST, Inc.		V-IIP	V-II		S-3	S-IIE		16%	168	XC2VP7-7
Embedded Processing											
Internet Appliance (socPiP-1A_Platform)	SoC Solutions, LLC			V-II	V-E				58%	62	XC2V1000-6
Java Processor, 32-bit (Lightfoot)	Digital Communications Technologies, Ltd.			V-II				S-II	73%	31	XC2S200-6
Java Processor, Configurable (LavaCORE)	Derivation Systems, Inc.			V-II					38%	20	XC2V1000-5
MicroBlaze Microcontroller - REFERENCE DESIGN	Xilinx					S-3					
MicroBlaze Soft RISC Processor	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		150	Virtex-II Pro (-6)
MicroBlaze Source Code	Xilinx	V-4	V-IIP	V-II	V-E	S-3	S-IIE	S-II		150	Virtex-II Pro (-6)
PicoBlaze (XAPP 213: PicoBlaze 8-bit Microcontroller)	Xilinx				V-E		S-IIE	S-II	9%	74	XC2S50E-7
UltraContoller Solution: A lightweight PowerPC Microcontroller (XAPP672)	Xilinx		V-IIP							200	Virtex-II Pro (-7)
UltraController II Solution: Minimal Footprint Embedded Processing Engine (XAPP575)	Xilinx	V-4	V-IIP							450	Virtex-4
UltraController Solution: A lightweight PowerPC Microcontroller (XAPP672)	Xilinx		V-IIP							200	Virtex-II Pro (-7)
VxWorks Board Support Package (BSP)	Xilinx	V-4	V-IIP							150	Virtex-II Pro (-6)

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XAPP577 – HD-SDI Integration Examples for the Serial Digital Video Demonstration Board	*http://www.xilinx.com/bvdocs/appnotes/xapp577.pdf*
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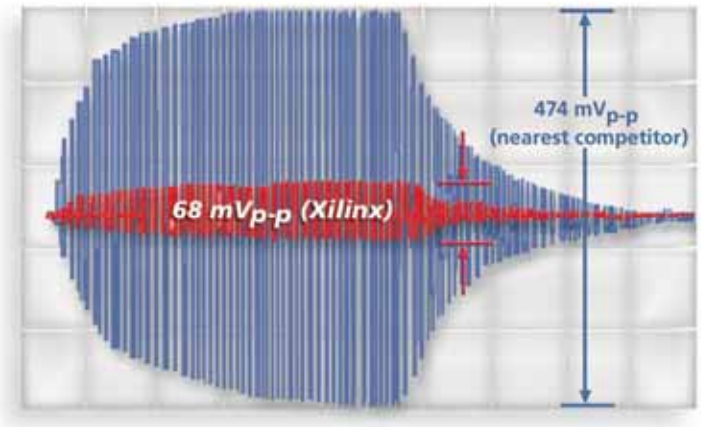

Design Example: 1.5 volt LVCMOS 4mA, I/O, 100 aggressors shown.

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