Stacked & Loaded: Xilinx SSI, 28-Gbps I/O
Yield Amazing FPGAs

by Mike Santarini
Publisher, Xcell Journal
Xilinx, Inc.
mike.santarini@xilinx.com
Xilinx recently added to its lineup two innovations that will further expand the application possibilities and market reach of FPGAs. In late October, Xilinx® announced it is adding stacked silicon interconnect (SSI) FPGAs to the high end of its forthcoming 28-nanometer Virtex®-7 series (see Xcell Journal, Issue 72). The new, innovative architecture connects several dice on a single silicon interposer, allowing Xilinx to field Virtex-7 FPGAs that pack as many as 2 million logic cells—twice the logic capacity of any other announced 28-nm FPGA—enabling next-generation capabilities in the current generation of process technology.

Then, in late November, Xilinx tipped the Virtex-7 HT line of devices. Leveraging this SSI technology to combine FPGA and high-speed transceiver dice on a single IC, the Virtex-7 HT devices are a giant technological leap forward for customers in the communications sector and for the growing number of applications requiring high-speed I/O. These new FPGAs carry many 28-Gbit/second transceivers along with dozens of 13.1-Gbps transceivers in the same device, facilitating the development of 100-Gbps communications equipment today and 400-Gbps communications line cards well in advance of established standards for equipment running at that speed.

**MORE THAN MOORE**

Ever since Intel co-founder Gordon Moore published his seminal article “Cramming More Components onto Integrated Circuits” in the April 19, 1965 issue of *Electronics* magazine, the semiconductor industry has doubled the transistor counts of new devices every 22 months, in lockstep with the introduction of every new silicon process. Like other companies in the semiconductor business, Xilinx has learned over the years that to lead the market, it must keep pace with Moore’s Law and create silicon on each new generation of process technology—or better yet, be the first company to do so.

Now, at a time when the complexity, cost and thus risk of designing on the latest process geometries are becoming prohibitive for a greater number of companies, Xilinx has devised a unique way to more than double the capacity of its next-generation devices, the Virtex-7 FPGAs. By introducing one of the semiconductor industry’s first stacked-die architectures, Xilinx will field a line of the world’s largest FPGAs. The biggest of these, the 28-nm Virtex-7 XC7V2000T, offers 2 million logic cells along with 46,512 kbits of block RAM, 2,160 DSP slices and 36 GTX 10.3125-Gbps transceivers. The Virtex-7 family includes multiple SSI FPGAs as well as monolithic FPGA configurations. Virtex-7 is the high end of the 7 series, which also includes the new low-cost, low-power Artix™ FPGAs and the midrange Kintex™ FPGAs—all implemented on a unified Application Specific Modular Block Architecture (ASMBL) architecture.

The new SSI technology is more than just a windfall for customers itching to use the biggest FPGAs the industry can muster. The successful deployment of stacked dice in a mainstream logic chip marks a huge semiconductor engineering accomplishment. Xilinx is delivering a stacked silicon chip at a time when most companies are just evaluat-
ing stacked-die architectures in hopes of reaping capacity, integration, PCB real-estate and even yield benefits. Most of these companies are looking to stacked-die technology to simply keep up with Moore’s Law—Xilinx is leveraging it today as a way to exceed it and as a way to mix and match complementary types of dice on a single IC footprint to offer vast leaps forward in system performance, bill-of-materials (BOM) savings and power efficiency.

THE STACKED SILICON ARCHITECTURE

“This new stacked silicon interconnect technology allows Xilinx to offer next-generation density in the current generation of process technology,” said Liam Madden, corporate vice president of FPGA development and silicon technology at Xilinx. “As die size gets larger, the yield goes down exponentially, so building large dice is quite difficult and very costly. The new architecture allows us to build a number of smaller dice and then use a silicon interposer to connect those smaller dice lying side-by-side on top of the interposer so they appear to be, and function as, one integrated die” (Figure 1).

Each of the dice is interconnected via layers in the silicon interposer in much the same way that discrete components are interconnected on the many layers of a printed-circuit board (Figure 2). The die and silicon interposer layer connect by means of multiple microbumps. The architecture also uses through-silicon vias (TSVs) that run through the passive silicon interposer to facilitate direct communication between regions of each die on the device and resources off-chip (Figure 3). Data flows between the adjacent FPGA die across more than 10,000 routing connections.

Madden also notes that the microbumps are not directly connected to the package. Rather, they are interconnected to the passive interposer, which in turn is linked to the adjacent die. This setup offers great advantages by shielding the advantages. “We use regular silicon interconnect or metallization to connect up the dice on the device,” said Madden. “We can get many more connections within the silicon than you can with a system-in-package. But the biggest advantage of this approach is power savings. Because we are using chip interconnect to connect the dice, it is much more economical in power than connecting dice through big traces, through packages or through circuit boards.”

In fact, the SSI technology provides more than 100 times the die-to-die connectivity bandwidth per watt, at one-fifth the latency, without consuming any high-speed serial or parallel I/O resources.

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Figure 1 – The stacked silicon architecture places several dice (aka slices) side-by-side on a silicon interposer.
microbumps from electrostatic discharge. By positioning dice next to each other and interfaced to the ball-grid array, the device avoids the thermal flux, signal integrity and design tool flow issues that would have accompanied a purely vertical die-stacking approach.

As with the monolithic 7 series devices, Xilinx implemented the SSI members of the Virtex-7 family in TSMC’s 28-nm HPL (high-performance, low-power) process technology, which Xilinx and TSMC developed to create FPGAs with the right mix of power efficiency and performance (see cover story sidebar, Xcell Journal, Issue 72).

**NO NEW TOOLS REQUIRED**

While the SSI technology offers some radical leaps forward in terms of capacity, Madden said it will not force a radical change in customer design methodologies. “One of the beautiful aspects of this architecture is that we were able to establish the edges of each slice [individual die in the device] along natural partitions where we would have traditionally run long wires had these structures been in our monolithic FPGA architecture,” said Madden. “This meant that we didn’t have to do anything radical in the tools to support the devices.” As a result, “customers don’t have to make any major adjustments to their design methods or flows,” he said.

At the same time, Madden said that customers will benefit from adding floor-planning tools to their flows because they now have so many logic cells to use.

**A SUPPLY CHAIN FIRST**

While the design is in and of itself quite innovative, one of the biggest challenges of fielding such a device was in putting together the supply chain to manufacture, assemble, test and distribute it. To create the end product, each of the individual dice must first be tested extensively at the wafer level, binned and sorted, and...
then attached to the interposer. The combined structure then needs to be packaged and given a final test to ensure connectivity before the end product ships to customers.

Madden’s group worked with TSMC and other partners to build this supply chain. “This is another first in the industry, as no other company has put in place a supply chain like this across a foundry and OSAT [outsourced semiconductor assembly and test],” said Madden.

“Another beautiful aspect of this approach is that we can use essentially the same test approach that we use in our current devices,” he went on. “Our current test technology allows us to produce known-good dice, and that is a big advantage for us because in general, one of the biggest barriers of doing stacked-die technology is how do you test at the wafer level.”

Because the stacked silicon technology integrates multiple Xilinx FPGA dice on a single IC, it logically follows that the architecture would also lend itself to mixing and matching FPGA and other dice to create entirely new devices. And that’s exactly what Xilinx did with its ultrafast Virtex-7 HT line, announced just weeks after the SSI technology rollout.

**DRIVING COMMUNICATIONS TO 400 GBPS**

The new Virtex-7 HT line of devices is targeted squarely at communications companies that are developing 100- to 400-Gbps equipment. The Virtex-7 HT combines on a single IC multiple 28-nm FPGA dice, bearing dozens of 13.1-Gbps transceivers, with 28-Gbps transceiver dice. The result is to endow the final device with a formidable mix of logic cells as well as cutting-edge transceiver performance and reliability.

The largest of the Virtex-7 HT line includes sixteen GTZ 28-Gbps transceivers, seventy-two 13.1-Gbps transceivers plus logic and memory, offering transceiver performance and capacity far greater than competing devices (see Video 1, http://www.youtube.com/user/XilinxInc#p/c/71A9E924ED61B8F9/1/eTHjt67ViK0).

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**Figure 3** – Actual cross-section of the 28-nm Virtex-7 device. TSVs can be seen connecting the microbumps (dotted line, top) through the silicon interposer.

**Video 1** – Dr. Howard Johnson introduces the 28-Gbps transceiver-laden Virtex-7 HT. http://www.youtube.com/user/XilinxInc#p/c/71A9E924ED61B8F9/1/eTHjt67ViK0.

**Video 2** – Dr. Howard Johnson explains the benefits of using TSVs. http://www.youtube.com/user/XilinxInc#p/c/71A9E924ED61B8F9/1/eTHjt67ViK0.
Communications equipment design teams traditionally have used FPGAs to receive signals sent to equipment in multiple protocols, translate those signals to common protocols that the equipment and network use, and then forward the data to the next destination. Traditionally companies have placed a processor in between FPGAs monitoring and translating incoming signals and those FPGAs forwarding signals to their destination. But as FPGAs advance and grow in capacity and functionality, a single FPGA can both send and receive, while also performing processing, to add greater intelligence and monitoring to the system. This lowers the BOM and, more important, reduces the power and cooling costs of networking equipment, which must run reliably 24 hours a day, seven days a week.

In a white paper titled “Industry’s Highest-Bandwidth FPGA Enables World’s First Single-FPGA Solution for 400G Communications Line Cards,” Xilinx’s Greg Lara outlines several communications equipment applications that can benefit from the Virtex-7 HT devices (see http://www.xilinx.com/support/documentation/white_papers/wp385_V7_28G_for_400G_Comm_Line_Cards.pdf).

To name a few, Virtex-7 HT FPGAs can find a home in 100-Gbps line cards supporting OTU-4 (Optical Transfer Unit) transponders. They can be used as well in muxponders or service aggregation routers, in lower-cost 120-Gbps packet-processing line cards for highly demanding data processing, in multiple 100G Ethernet ports and bridges, and in 400-Gbps Ethernet line cards. Other potential applications include base stations and remote radio heads with 19.6-Gbps Common Public Radio Interface requirements, and 100-Gbps and 400-Gbps test equipment.

JITTER AND EYE DIAGRAM
A key to playing in these markets is ensuring the FPGA transceiver signals are robust, reliable and resistant to jitter or interference and to fluctuations caused by power system noise. For example, the CEI-28G specifications call for 28-Gbps networking equipment to have extremely tight jitter budgets.

Signal integrity is an extremely crucial factor for 28-Gbps operation, said Panch Chandrasekaran, senior marketing manager of FPGA components at Xilinx. To meet the stringent CEI-28G jitter budgets, the transceivers in the new Xilinx FPGAs employ phase-locked loops (PLLs) based on an LC tank design and advanced equalization circuits to offset deterministic jitter.

“Noise isolation becomes a very important parameter at 28-Gbps signaling speeds,” said Chandrasekaran. “Because the FPGA fabric and transceivers are on separate dice, the sensitive 28-Gbps analog circuitry is isolated from the digital FPGA circuits, providing superior isolation compared to monolithic implementations” (Figures 4a and 4b).

The FPGA design also includes features that minimize lane-to-lane skew, allowing the devices to support stringent optical standards such as the Scalable Serdes Framer Interface standard (SFI-S).

Further, the GTZ transceiver design eliminates the need for designers to employ external reference resistors, lowering the BOM costs and simplifying the board design. A built-in “eye scan” function automatically measures the height and width of the post-equalization data eye. Engineers can use this diagnostic tool to perform jitter budget analysis on an active channel and optimize transceiver parameters to get optimal signal integrity, all without the expense of specialized equipment.

ISE® Design Suite software tool support for 7 series FPGAs is available today. Virtex-7 FPGAs with massive logic capacity, thanks to the SSI technology, will be available this year. Samples of the first Virtex-7 HT devices are scheduled to be available in the first half of 2012. For more information on Virtex-7 FPGAs and SSI technology, visit http://www.xilinx.com/technology/roadmap/7-series-fpgas.htm.

Figure 4a – Xilinx 28-Gbps transceiver displays an excellent eye opening and jitter performance (using PRBS31 data pattern).

Figure 4b – This is a competing device’s 28-Gbps signal using a much simpler PRBS7 pattern. The signal is extremely noisy with a significantly smaller eye opening. Eye size is shown close to relative scale.