2018 Xilinx Security Design Workshop (XSDW) San Jose, CA Agenda

Fairmont San Jose, 170 South Market Street, San Jose, California 95113, USA

Monday, October 1, 2018 All Presentations in Atherton Room	
Topic	**Time**
Introduction to Xilinx Security	8:30 - 9:00
What's "In the Box" and What's "Out of the Box"	9:00 - 10:00
Break	10:00 - 10:30
Next Generation Security / Survey	10:30 - 12:00
Lunch	12:00 - 1:00
Zynq UltraScale+ MPSoC Security	1:00 - 2:00
Break	2:00 - 2:30
Zynq UltraScale+ MPSoC Secure Boot	2:30 - 3:30
Zynq UltraScale+ MPSoC Trusted Execution Environment	3:30 - 4:15
Break	4:15 - 4:45
UltraScale and UltraScale+ FPGA Security	4:45 - 5:30
Day 1 Wrap Up / Summary Statements	5:30 - 5:45

2018 Xilinx Security Design Workshop (XSDW) San Jose, CA Agenda

Fairmont San Jose, 170 South Market Street, San Jose, California 95113, USA

Tuesday, October 2, 2018		
Keynote : Victor Peng, President and CEO Presented in Imperial Ballroom 9:00 - 10:30		
Lectures : Atherton Room	**Time**	**Demonstrations : Belvedere Room**
All Hands Day 2 Re-Greet	10:30 - 10:45	**(No Demo This Period)**
Guidance on Essential Security Design Resources/Information	10:45 - 11:15	**UltraScale and UltraScale+ FPGA Secure Configuration**
Security Monitor (SecMon) IP	11:15 - 12:15	**Functional and Physical Isolation Within the Zynq UltraScale+ MPSoC**
Lunch	12:15 - 1:15	**Lunch**
Security in Automotive Applications	1:15 - 2:15	**Zynq UltraScale+ MPSoC Secure Boot**
Security in Industrial IoT applications	2:15 - 3:15	
Break	3:15 - 3:45	**Break**
Security in FPGA as Service (FaaS) Applications	3:45 - 4:15	**Zynq UltraScale+ MPSoC Enhanced Key Revocation**
Security in DataCenter Applications	4:15 - 4:45	**Secure Storage Using the Zynq UltraScale+ MPSoC Physical Unclonable Function (PUF)**
	4:45 - 5:15	**UltraScale and UltraScale+ FPGA Tamper Logging and Penalty Response**
XSDW 2018 Adjournment and Door Prizes	5:15 - 5:30	**(No Demo This Period)**