De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement

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ALL PROGRAMMABLE.

January 28-31, 2014 I Santa Clara Convention Center I Santa Clara, CA
Outline

- 28 Gb/s SERDES Channel Overview
- Design Analysis for Band Limited Fixture Removal
- Fixture Removal Methods
- 28 Gb/s SERDES Measurements at the DUT
28nm FPGA with GTZ XCVR 7H580T

Heterogeneous VH580T

VH580T GTZ TX
Eye Diagram: 28.05Gb/s

VH580T GTZ
RX Eye Scan: 28.05Gb/s
Through a 12.5 dB Lossy Trace
28 Gb/s Channel

Xilinx Virtex-7 FPGA
28G Tx

Package Substrate

PCB Traces

Samtec® BullsEye™ Test Connector

PCB-Connector Transition

SMA

SMA
**Physical Description PCB Stackup**

**PCB Stackup**

- 22 Layers
- HS signal layers: Panasonic Megtron6
- Other layers: ISOLA 370HR - FR4
- For Megtron6 and 370HR interleaved in lower layers for mechanical stability

*Note: For economic reasons other layers are standard FR4 (ISOLA 370HR)*
Physical Description Pin/Via Breakout

BGA Pin Via Field

- High-speed Signal Via (Backdrilled)
- Standard Signal Via (Not Backdrilled)
- Ground Via (Not Backdrilled)

Via Topology

- 10 mil Drill
- 20 mil pad
- 28 mil anti-pad
- Backdrill – 8 mils from target layer +/- 3mils
Physical Description - PCB Layout

BGA Pin Via Field

PCB Stripline Routing

Connector Pin Via Field

Differential Pair Routing: 3.5 mil Traces with 10 mil gap
28 Gb/s Tx Measurement Challenge

Measurement Fixture
- Coaxial Adapters
- Cable Assembly
- PCB Routing
- BGA Via Field

Agilent 86100D DCA-X Wide-Bandwidth Oscilloscope

Test Fixture and cable to be characterized and de-embedded (Device Under Test or DUT)

Xilinx Virtex-7 FPGA
Band-Limited S-Parameters for De-Embedding

**Frequency to Time Domain**

**Inverse Fourier Transform**

**Summation of Sine Waves**

**Case 1**

*Infinite Sum of Sine Waves*

- Rise Time 13 ps
- 3 dB B.W.: 17 GHz
- 3rd Harmonic: 42 GHz
- 5th Harmonic: 70 GHz

**Case 2**

*Finite Sum of Sine Waves*

- Rise Time 5 ps
- 3 dB B.W.: 44 GHz
- 3rd Harmonic: 42 GHz
- 5th Harmonic: 70 GHz

**Non-Causal Ripple - Gibbs Phenomena**
Error Due to Gibbs Phenomena

Time Domain Simulated Pulse
- Rise Time: 13 ps
- Pulse Width: 216 ps

Frequency Domain (FFT of Pulse)
- Bandwidth: 200 GHz
- Small amplitude at the band-limit.

Time Domain i-FFT of Bandlimited Frequency Domain Data
- Rise Time: 20 ps
- 5% Ripple
- Pulse Width: 216 ps

Frequency Domain (FFT of Pulse)
- Bandwidth: 17 GHz
- Brick-wall Windowing
Required Channel Bandwidth

Time Domain

- **i-FFT of 34 GHz Bandlimited Data**
  - Rise Time: 15 ps
  - Ripple: ~1%

- **i-FFT of 50 GHz Bandlimited Data**
  - Rise Time: 13 ps
  - Ripple: ~0.2%

Frequency Domain

- **Bandwidth 34 GHz**
  - Brickwall

- **Bandwidth 50 GHz**
  - Brickwall
**Eye Diagrams with Band-Limited S-Parameters**

28 Gb/s, PRBS 7 Eye Diagrams

<table>
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<tr>
<th>Bandlimited</th>
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<tbody>
<tr>
<td>17 GHz S-Parameters</td>
<td>34 GHz S-Parameters</td>
<td>50 GHz S-Parameters</td>
<td>100 GHz S-Parameters</td>
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Inverse Fourier Transform with 4th Order Bessel Windowing

Hilbert Transform with Causality Enforcement
**Fixture De-Embedding Methods**

**Channel Model De-Embedding Options**

1) **Direct Probe** Measurement

2) **Test Coupon** Structure with AFR

3) **Hybrid** Multi-Path Simulation with Minimal Test Structures

4) **Direct Reflect** Measurement with AFR algorithm.

*New Technique for 2014*
Fixture Removal Review

**BEFORE**
- FIXTURE + Resonant Beatty Structure
- S-Parameters before Fixture De-Embed

**AFTER**
- DUT with Fixture Removed
- S-Parameters after Fixture De-Embed

**FIXTURE DE-EMBED**

**T-Matrix**
New 1-Port Automatic Fixture Removal

1-Port AFR
1-Port, Open at DUT
In-Situ Path Measurement

Note: Only 4 S-Parameters are used to calculate the differential .s4p fixture behavioral model.

Compare
2x Thru AFR
1-Port AFR
TRL Multiple Stds

Time Domain
TDR Impedance

Frequency Domain
Insertion Loss – S21
### Partial vs. Full De-Embedding

**Partial De-embedding:**
- Removes insertion loss
- Does NOT remove reflections (assumes an ideal source, receiver)
- Easier to implement

**This paper’s focus.**

**Full De-embedding:**
- Removes insertion loss and reflections between circuit elements
- More accurate (but less forgiving if models/delays are not correct)
Partial S21 De-Embedding for 28 Gb/s Fixture

**Fixture Behavioral Models**

- **Frequency Domain**
  - S-parameter Behavioral Fixture Models
  - S21 Red = ADS Simulated Model
  - S21 Green = Gen 2 AFR with 1-port

- **Time Domain Impedance**
  - TDR Blue = Gen 1 AFR with 2X THRU
  - TDR Green = Gen 2 AFR with 1-port

**Partial vs. Full De-Embedding**

- **Fixture on Each Side: Beatty DUT**
  - Full S-Matrix Fixture De-Embed
  - Partial S21 Fixture De-Embed
  - Beatty Standard with Fixture Included

- **Fixture on One Side: Active Tx DUT**
  - Partial S21 De-Embed with .1 nF excess L at DUT
  - Partial S21 De-Embed with Ideal Zo matched DUT
  - Full S-Matrix De-Embed with 12 mil length difference

**Tx PRBS7 Spectrum Before and After Partial De-Embedding**

Beatty

Active Tx
Device Characterization
Measurements used to compare de-embed models

• Waveform
  – Compare specific bit sequences (bits onscreen)
  – Rise/Fall Time
  – Amplitude

• Eye Diagram
  – Fast and efficient, examine all bits in a pattern
  – Rise/Fall Time
  – Eye Amplitude
  – Eye Height

• Jitter and Amplitude Analysis
  – Isolate random and deterministic components
  – Focus on inter-symbol interference (ISI)
    (check efficacy of S-parameter models used for de-embedding)
Clock Recovery (CR) Basics

Clock Recovery is required for compliant jitter measurements.

PLL “Jitter Transfer Function” (JTF)
- indicates how much of the jitter on the input signal is “transferred” to the recovered clock (output)
- low-pass filter function (LPF)

JTF = Closed loop gain
\[
\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{A(s)}{1 + A(s)} = G(s) = |G(s)|e^{j\delta(s)}
\]

“Observed Jitter Transfer Function” (OJTF)
- indicates the jitter that is “observed” by the receiver (scope)
- high frequency jitter on the data stream is “transferred” to the receiver (HPF)

OJTF = 1 – JTF
\[
= 1 - G(s) = 1 - |G(s)|e^{j\delta(s)}
\]

Standards Specify:
- PLL Order/Type
- PLL Bandwidth
- Peaking (Damping Factor)
28 Gb/s Performance of Fixture Removal Methods

Test Equipment Setup

Agilent 86100D DCA-X with 86108B module
- Bandwidth: 50 GHz
- Intrinsic Random Jitter: < 50 fs rms
- Integrated Clock Recovery
  - Data Rate (DR): 28.05 Gb/s
  - Loop Order: 1st Order (0 dB Peaking)
  - PLL Bandwidth: 16.8 MHz (DR/1667)

Note 1 – the "Align" function simply removes filter delay and aligns waveforms making it easier to compare waveforms.
Waveform Measurements

1-Port AFR Model:
- Rise time (20%-80%): 2.6 ps faster (20% improvement)
- Amplitude: 163 mV higher (27% improvement)
Waveform Measurements

- Where does the ringing come from after de-embedding?
Eye Diagram Measurements

1-Port AFR Model:
• Rise time (20%-80%): 3.1 ps faster (20% improvement)
• Eye Amplitude: 204 mV higher (25% improvement)
Jitter Measurements

1-Port AFR Model (PRBS7):
- Total Jitter (1E-12): 6.05ps (1.7ps lower)
- Random Jitter (RJ): 267 fs (~ unchanged)
- Deterministic Jitter (DJ): 2.4ps (1.7ps lower)
- Inter-Symbol Interference (ISI): 2.37ps (1.4 ps lower)

1-Port AFR Model (PRBS15):
- ISI: 4.98ps (1.8 ps lower)
Summary

• Fixture de-embedding Lessons Learned:
  – Test Fixture is simple to build and measure
  – Full de-embedding is sensitive to reference plane errors.
  – Partial de-embedding
    • A practical solution when Tx is impedance matched.
    • Substantially less effort than full de-embed
    • Results are sufficient in most cases
  – 1-Port AFR enables simple in-situ fixture channel measurement.
Conclusion

• This methodology is useful
  – Economical use of time and resources
  – Does not require elaborate measurement equipment and set up
  – Results are adequate without expensive effort and resources

“Accurate 28 Gb/s Tx real-time measurements at the DUT package require fixture de-embedding.”
Acknowledgements

• Fangyi Rao of Agilent for his patience in explaining causal frequency to time domain transforms.

• Jim Stimple of Agilent for his explanation of the band limiting differences between real-time scopes with arbitrary data and sampling scopes with repetitive data.