Comprehensive Full-Chip Methodology To Verify Electro-Migration and Dynamic Voltage Drop On High Performance FPGA Designs In The 20nm Technology

Sujeeth Udiipi (Xilinx)
Karan Sahni (Ansys)
About Xilinx

- Xilinx makes FPGA chips.
  - Successful tape-out at 20nm.
  - The Xilinx design is a mosaic of functional tiles.
    - For example: RAM tiles, programmable logic tiles, IO tiles, etc.
    - Design mix is dominated by custom designs of moderate size.
  - We are limited by vector generation:
    - A complete vector set is generally unavailable.
    - Vectors come in late in the design cycle.
    - Designers often use manually generated, functional vectors.
    - Most vectors are of limited duration.
    - Long vectors result in long runtimes.
Xilinx EM-IR Philosophy

• We must have 100% coverage:

• We must have “acceptable” accuracy:
  – Accuracy must be “within acceptable bounds” for all design styles.
  – Results must trend as per user intuition.

• Default methodology must never be optimistic.
  – Methodology/tool limitations may cause inaccuracy in result.
  – This inaccuracy must always be “bounded and pessimistic”.

• We must have user overrides to overcome limitations of default methodology and accuracy.

• Signal-EM penalty is paid for within a fixed time interval.
  – EM result should not depend on the number of transitions in vector.
  – User overrides for activity factor are allowed.
Signal-EM Dependence On Vector *

* Inverter testcase, constant load; current values are for PMOS device of inverter.

<table>
<thead>
<tr>
<th>Time</th>
<th>Iavg</th>
<th>Irms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle</td>
<td>12uA</td>
<td>42uA</td>
</tr>
<tr>
<td>SimTime</td>
<td>12uA</td>
<td>42uA</td>
</tr>
</tbody>
</table>

Fig. 1 - For clock nets, AVG and RMS currents match for CYCLE and SIM time.

<table>
<thead>
<tr>
<th>Time</th>
<th>Iavg</th>
<th>Irms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle</td>
<td>12uA</td>
<td>42uA</td>
</tr>
<tr>
<td>SimTime</td>
<td>9.2uA</td>
<td>37uA</td>
</tr>
</tbody>
</table>

Fig 2 & 3 - For data nets, AVG and RMS currents depend on the number of transitions in any given time interval.

<table>
<thead>
<tr>
<th>Time</th>
<th>Iavg</th>
<th>Irms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle</td>
<td>12uA</td>
<td>42uA</td>
</tr>
<tr>
<td>SimTime</td>
<td>3.8uA</td>
<td>24.3uA</td>
</tr>
</tbody>
</table>
The idea is to pay the EM penalty within a fixed time period of one cycle.

- Let’s say you have a four cycle simulation (CYCLE1 to CYCLE4)
- Initial delay is 2ns, and each subsequent cycle is 2ns wide.

**Simulation Settings:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQ</td>
<td>500e06</td>
</tr>
<tr>
<td>DYNAMIC_SIMULATION_TIME</td>
<td>8n</td>
</tr>
<tr>
<td>DYNAMIC_TIME_STEP</td>
<td>10p</td>
</tr>
</tbody>
</table>

**Cycle Definitions:**

- CYCLE1 “ ” “ ” 2ns 4ns
- CYCLE2 “ ” “ ” 4ns 6ns
- CYCLE3 “ ” “ ” 6ns 8ns
- CYCLE4 “ ” “ ” 8ns 10ns
All designs must pass the following checks:

<table>
<thead>
<tr>
<th>Flow</th>
<th>Must Pass</th>
<th>Coverage</th>
<th>What Is Checked</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td>IR / AVG-EM</td>
<td>100%</td>
<td>PG gross-checker on all designs</td>
</tr>
<tr>
<td>Dynamic</td>
<td>IR / AVG-EM / RMS-EM</td>
<td>&lt;100%</td>
<td>Large drivers / Large arrays Decap check / Jitter Concerns</td>
</tr>
<tr>
<td>Signal-EM</td>
<td>AVG-EM / RMS-EM</td>
<td>100%</td>
<td>Mixed-Mode Signal-EM enables 100% coverage</td>
</tr>
</tbody>
</table>

Level at which EM-IR is run must capture context adequately:
- Design size must be large enough, comparable to bump pitch.
- Design must comprise upper metal layers, must include decaps, etc.

EM result must be independent of the quality of vectors.
- By default, clock nets are analyzed at TR=2, while non-clock nets at TR=1.

Design must pass FIT.
- AVG-EM violations can be waived if design passes FIT.
What is FIT?

- FIT stands for “Failure In Time.”
- A fullchip FIT of “1” indicates that the failure rate of the part will be 0.1% after 10 years.
  - The fullchip FIT budget is split between AVG EM and TDDB.
  - The fullchip budget is divided into subblock budgets.
- Subblock FIT budget depends on:
  - Area of the subblock
  - Frequency of the subblock
  - Design Style
FIT-Based EM Check versus Rule-Based EM Check

- **Budget** represents how much design is *allowed* to contribute to Product Failure Rate (FIT)

- Rule-based check might be too conservative (top) or overlook actual risk (bottom).
EM-IR Corner Methodology

- The EM-IR corner is:
  - Fast Transistors
  - High Temperature
  - Extraction is Typical
  - Nominal Supply voltages
- EM-IR corner must match:
  - Power Corner
  - Timing Corner
  - SPICE corner for spice simulations
• Transistor-level Power EM-IR flows can be run in two modes:
  – Static:
    • Power is distributed over all transistors in the design.
    • Transistor current is assigned as below:
      \[ I_{\text{transistor}} = \frac{P_{\text{sup}}}{V_{\text{sup}}} \times \frac{W_{\text{transistor}}}{\sum W_{\text{transistor}}} \]
    • The Static check is a gross-checker, but it gives 100% coverage.
  – Dynamic (Vectored)
    • Only the active/switching areas of the design get any current assignment.
    • All transistor currents are probed through a SPICE simulation.
    • The Dynamic check is accurate, but gives limited coverage.
Device Current Distribution: Static vs. Dynamic

Total power in both cases was the same,
Dynamic Drop - Decap Efficiency Test

This simulation tests the following:

Location of power noise sources, distance to sensitive circuitry, amount of DvD noise, effect of decap on DvD, etc.

The purpose of Dynamic Analysis is to measure this.

A very long simulation will end up measuring this.
Dynamic Drop - Distance Of Decap

Decap Regions

Distance=D1
Distance=D2
Distance=D3
Distance=D4
Distance=D5

Active Regions
Dynamic Drop - Distance Of Decap

Distance = D1

Distance = D2

Distance = D3

Distance = D4

Distance = D5
Decap Placement Recommendation

D is distance: D5 >> D4 >> D3 >> D2 >> D1
R is decap ratio: R5 >> R4 >> R3 >> R2 >> R1
Power Delivery System Overview

Diagram showing the power delivery system with components labeled as:
- On-die
- Package
- Board
- Regulator

Additional labels:
- Power grid
- Circuits
- VID
- Board
- Package
- Die
IR Drop Limit – Static vs. Dynamic

• Components of IR drop:
  – Package Drop
  – On-die Drop

• How to arrive at a Static IR limit?
  – An arbitrary low number!
  – Average drop over time – average drop from a worst case scenario.
  – Static Limit can match DC offset used in timing characterization.

• How to arrive at a Dynamic IR limit?
  – Timing characterization
  – Clock Jitter simulations
  – Pay attention to large drivers and sensitive circuitry
  – Total IR drop budget is split between off-die and on-die IR drop
  – Simulations include package inductor model
EM Budgeting / Failure Mechanisms

• Safety margins are built in:
  – Process/Fab Margin
  – Design Margin

• Failure Mechanisms in EM:
  – AVG EM limit is linked to metal voids.
  – RMS EM limit is linked to heating.
  – Heating causes further drop in AVG EM limit.

• Unidirectional / bidirectional segments:
  – Unidirectional more susceptible to AVG EM failures
  – Bi-directional more susceptible to RMS failures

• Poly/Metal Resistor Instances and Inductors:
  – Resistor instance paths are not valid candidates for the IR drop limit rules.
  – We “break” these paths so IR analysis is done up to the first resistor or inductor instance only and EM analysis is done on the internal path.
Why We Should Model Heat Flow

- More EM violations
- Less Design Margin

- 20nm Process Node

- Generational increase in Slew/Fanouts
- Bidir wires susceptible
- Generational Increase in RMS current

- Unidir wires susceptible
- Less design margin

- More EM violations
- More Design Margin

- Increased wire density
- Better heat dissipation
- Drive current drops with higher temperature

- More design margin
- Leverage FIT

- Reduces AVG EM Limit
- Decrease in RMS current
- Increased wire density
- Better heat dissipation
- Drive current drops with higher temperature

- Leverage FIT
Vectorless Signal-EM – Driver Current Profiles

\[ I_{sw(bidir)} = F(C_{load}, V_{dd}, Slew) \]
\[ I_{crowbar(unidir)} = SF \cdot I_{sw} \]
\[ SF \text{ user specified scaling factor} \]

- Single cycle simulation will be performed (1 charge, 1 discharge) for different frequency domains.
- Uni-directional current (crowbar) will be scaled during post-processing (w/o simulation).
- Toggle rate will be used for \( I_{avg} / I_{rms} \) computation only (not for constructing current waveforms).

\[ I_{avg} = I_{avg(1cyc)} \cdot TR \cdot \text{Freq} \]
\[ I_{rms} = I_{rms(1cyc)} \cdot TR \cdot \text{Freq} \]
\[ I_{peak} = I_{peak(waveform)} \]
• Vectorless gives 100% coverage!
  – Default values are set to be aggressive.
• Results scale with frequency, slew rate and toggle rate.
  – Assuming the following reference EM settings:
    • Frequency \( f_1 \); Slew \( \text{slew}_1 \); Load \( \text{load}_1 \); Toggle Rate \( \text{TR}_1 \)
  – Assuming the following DUT settings:
    • Frequency \( f_1 \); Slew \( \text{slew}_1 \); Load \( \text{load}_1 \); Toggle Rate \( \text{TR}_2 \)

<table>
<thead>
<tr>
<th>EM Scaling with Electrical Parameters</th>
<th>AVG</th>
<th>RMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>( f_2/f_1 )</td>
<td>( \sqrt{f_2/f_1} )</td>
</tr>
<tr>
<td>Slew</td>
<td>No change</td>
<td>( \sqrt{\text{slew}_2/\text{slew}_1} )</td>
</tr>
<tr>
<td>Load</td>
<td>( \text{load}_2/\text{load}_1 )</td>
<td>( \sqrt{\text{load}_2/\text{load}_1} )</td>
</tr>
<tr>
<td>Toggle Rate</td>
<td>( \text{TR}_2/\text{TR}_1 )</td>
<td>?</td>
</tr>
</tbody>
</table>
RMS EM dependence on peak current.

- RMS is the SQRT of the average of the square of the current.

<table>
<thead>
<tr>
<th>Case</th>
<th>Avg i</th>
<th>Avg $i^2$</th>
<th>RMS i</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>2</td>
<td>8</td>
<td>2.8</td>
</tr>
<tr>
<td>Case 2</td>
<td>2</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Case 1 @ half TR</td>
<td>1</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Case 2 @ half TR</td>
<td>1</td>
<td>2</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Higher peak causes higher RMS current for same total charge*.

Halving of the TR reduces RMS by sqrt (2).

* This assumes current profiles are completely enclosed within the same cycle time of 2.
RMS EM is strongly influenced by peak current.

– RMS is the SQRT of the average of the square of the current.

<table>
<thead>
<tr>
<th></th>
<th>Avg i</th>
<th>Avg i^2</th>
<th>RMS i</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>2</td>
<td>10.6</td>
<td>3.3</td>
</tr>
<tr>
<td>Case 2</td>
<td>2</td>
<td>5.3</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Halving of the slew reduces RMS by sqrt (2)

* This assumes current profiles are completely enclosed within the same cycle time of 2.
Should I run Vectored Or Vectorless Signal-EM?

Start

Analog Or Digital?

Vectors available?

Yes

Run Vectored
(set current threshold)

Moderately Pessimistic
(OK for TO)

Most Accurate
(POR for custom/analog)

No

Run Vectorless

Least Accurate
(Not advised)

Slew data available?

Yes

Vectorless with slews from NT

Slightly pessimistic
(POR for digital)

No

Vectorless with default slews

Recommended

Custom/Analog

Digital

Recommended
How the methodologies are linked...
Accuracy – Transistor Level Vectored IR

- Y-axis represents % of the total count of destination device diffusions.
- X-axis is the accuracy range -10mV to 40mV.
- Sample size: 10,000 worst transistors from 6 testcases.
- Both analog and digital testcases were considered.

![Graph showing accuracy distribution with three curves: RC-golden, Conly, and Conly-derate. The graph indicates increasing pessimism and outliers.]
Accuracy – Transistor Level Vectored Signal-EM

- Y-axis is normalized to %.
- X-axis is the accuracy range -50% to +50%.
- Sample size small ~ 200 nets
- Both analog and digital blocks were considered.
Various Design Styles

- Our EM-IR Tools:
  - Totem  □ For transistor level designs
  - Redhawk  □ For cell based designs

- We will have the following design styles:
  - PNR Blocks
  - Custom Blocks
  - Mixed Blocks (Custom + PNR blocks)

- Blocks come in different sizes:
  - Medium (no capacity issues)
  - Big (possible capacity issues)

- Levels of Hierarchy / Analysis:
  - Block level
  - Subblock level
  - Arbitrary level (for exceptional cases)
Fullchip Partitioning

A high level view of fullchip:

- Anatomy of a “Mixed” block:
  - Lib/Macro/Custom
  - PNR Boundary
Design Styles And Tool Considerations

• Common Design Styles:

<table>
<thead>
<tr>
<th>Type</th>
<th>Flow</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Cell</td>
<td>Cell Level</td>
<td>Can’t do FIT</td>
</tr>
<tr>
<td>Custom</td>
<td>Transistor level</td>
<td>100% coverage</td>
</tr>
<tr>
<td>Mixed Blocks</td>
<td>Cell and/or Transistor Level</td>
<td>Some coverage loss</td>
</tr>
</tbody>
</table>

• Size Considerations:

<table>
<thead>
<tr>
<th>Size</th>
<th>Runtime*</th>
<th>Cell Flow</th>
<th>Transistor Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small</td>
<td>3 hours ?</td>
<td>1 million instances</td>
<td>0.3 million transistors</td>
</tr>
<tr>
<td>Medium</td>
<td>1-2 days</td>
<td>n/a</td>
<td>1 million transistors</td>
</tr>
<tr>
<td>Large</td>
<td>2-4 days</td>
<td>n/a</td>
<td>2+ million transistors</td>
</tr>
</tbody>
</table>

* This excludes SPICE run time. Assumes dedicated machine.
“Divide And Conquer” Approach

• How to break hierarchies?
  – Level of analysis must be considered early in design cycle.
  – Choice of subblock hierarchy impacts fullchip analysis.
  – Poor planning results in loss of coverage and loss of accuracy.

• Recommendations:
  – Fullchip analysis should traverse down to level of subblock analysis.
  – Subblock models must be propagated to fullchip analysis.

<table>
<thead>
<tr>
<th>Required To Run</th>
<th>At Level</th>
<th>Flow</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static and Dynamic Power EM-IR</td>
<td>Block level</td>
<td>Transistor</td>
<td></td>
</tr>
<tr>
<td>AVG and RMS Signal-EM</td>
<td>Block level</td>
<td>Transistor</td>
<td>Run Vectorless Signal-EM</td>
</tr>
<tr>
<td>Static and Dynamic Power EM-IR</td>
<td>Custom Cell</td>
<td>Transistor</td>
<td>Follow directions for “Custom” blocks</td>
</tr>
<tr>
<td>AVG and RMS Signal-EM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Design Types And Flow Styles

<table>
<thead>
<tr>
<th>BLOCK TYPE</th>
<th>ANALYSIS</th>
<th>BLOCK DYNAMIC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Vectored</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vectorless</td>
</tr>
<tr>
<td>Custom</td>
<td>Power EM/IR</td>
<td>Transistor Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vectored</td>
</tr>
<tr>
<td>Signal EM</td>
<td></td>
<td>Transistor Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Analog □ Vectored/Mix-Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Digital □ Vectorless</td>
</tr>
<tr>
<td>P&amp;R</td>
<td>Power EM/IR</td>
<td>Cell Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vectorless</td>
</tr>
<tr>
<td>Signal EM</td>
<td></td>
<td>Cell Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vectorless</td>
</tr>
</tbody>
</table>
Package Simulations With On-Die Models
Interposer Simulations

- Interposers:
  - Stand-alone run
  - Static Simulation
  - Very low IR budget allowed
  - Must fix AVG EM
  - Regional power assignments
Summary

• **Highlights:**
  – We have very high design coverage (~100%).
  – We have very good accuracy.
  – Default methodology is conservative.
  – EM-IR methodology has withstood the scrutiny of the design community.

• **Areas Of Improvement:**
  – Handling super large designs (capacity and runtime)
  – Managing hierarchy / Integrating multiple runs to analyze in-between metal
  – Hierarchical FIT
Thank You!