Distributed Modeling and Characterization of On-Chip/System Level PDN and Jitter Impact

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• **Power integrity challenges**
  - More logic with each new generation of ICs
  - Higher data rates
  - Lower supply voltages
  - Shrinking timing margins
  - Cost optimization

• **To create a successful design need to**
  - Develop system-level PDN modeling methodology
  - Work out design specs and performance metrics
  - Develop characterization methodology
  - Correlate measured results with simulation predictions
  - Learn from the correlation, make adjustments
  - Repeat...
In This Presentation

- PDN components, their physical nature and contribution to voltage noise
- Approach to modeling
- Time domain and frequency domain metrics
- Simulation results
- Characterization options offered by FPGAs
- Measurement and correlation
- Voltage noise impact on system timing. Jitter
PDN Components
PDI Impedance

- **Resonances**
  - On-die capacitance & package inductance
  - Package decoupling capacitors & PCB inductance
  - Smaller PCB decoupling capacitors & board-level PDN inductance
  - Bulk PCB decoupling capacitors & VRM
Voltage Noise

\[ \delta(t) \]

High Frequency Switching

\[ \mu(t) \]

Event Driven

DESIGNCON 2013

VCCINT, Ideal Step, Load, Probe2, L_Probe2, A

Time, nsec

-20 | -10 | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 170 | 180 | 190 | 200 | 210 | 220

Time, nsec
Voltage Noise

- $V_{nom}$
- $V_{DL,typ}$
- $V_{DE,typ}$
- $+/V_{DB,Switching}$
- Leakage+min_activity
- Peak Load

- Switching activity starts
- Undershoot

Noise
CLK

Inset: Impedance, mΩ vs. Frequency, MHz
PDN Model

- **Layout**
  - 2.5D EDA Tool
  - 2.5D EDA Tool
  - HSPICE, CPM

- **PCB**
  - Board PDN (S-parameters)

- **Package**
  - Package PDN (S-parameters)
  - On-Package Decoupling Capacitors (S-parameters)

- **Chip**
  - On-Die PDN (Lumped RC)

- **Current Load**
  - Switching current profile
  - Ideal step load
Location, Location, Location

PCB
Board PDN (S-parameters)

Package
Package PDN (S-parameters)

Chip
On-Die PDN (Lumped RC)

Current Load

V_pkg

V_pkg_cap

V_die

(a)

(b)

ΔV_supply (mV)

Capacitors

Die area

Capacitors

Position X

Position Y

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Ideal Step Load vs. Realistic One
**Simulated Impedance Profiles**

- **System A** – SoC, medium-sized, flip-chip
- **System B** – Large monolithic FPGA, flip-chip
- **System C** – Smaller FPGA, wire-bond
Measurements. Probing solutions
Transient Step Response. System C
Step Response. System A
Impulse Response. System A
Full Cycle. System A
Impedance Measurement

- If we create a known excitation $i(t,f)$ and measure the response $v(t,f)$, we can derive $Z(f)$.

- **Time-domain measurements**
  - Only characteristic frequencies (resonances)
  - Impedance magnitude at resonance frequencies

- **Frequency-domain characterization**
  - Complete impedance profile of the system
Correlation. System A

- **System A** has a suboptimal board-level decoupling solution
System B has a larger die than System A → die/package resonance is at a lower frequency
**Correlation. System C**

- **System C** has no on-package decoupling capacitors → single resonance peak
- **System C** has a wire-bond package → high value of PDN impedance
Supply Noise Impact on System Timing

- Can be characterized as **phase noise** in frequency domain and translated into **jitter** in time domain
Excitation Options

- What is the “best” way to create noise?

\[ \left( \int i(f) \cdot z(f) df \right) \times \text{Jitter Sensitivity} \Rightarrow \text{jitter} \]
Correlation. System A

- Impedance profile shapes the phase noise curve

\[ \left( \int i(f) \cdot z(f) df \right) \times JitterSensitivity \Rightarrow jitter \]
Correlation. System B

\[
\left( \int i(f) \cdot z(f) \, df \right) \times \text{Jitter Sensitivity} \Rightarrow \text{jitter}
\]
Summary and Conclusions

- System-level approach to power integrity
- Time domain and frequency domain characteristics, metrics and specs
- Time domain and frequency domain cross-correlation
- Leveraging FPGA flexibility to create test setups with well-controlled conditions
- Complete impedance profile of system-level PDN
- PDN impact on system timing. Phase noise and jitter