ULTRASCALE FPGA DDR4 2400 MBPS SYSTEM LEVEL DESIGN OPTIMIZATION AND VALIDATION
FPGA High Speed High Bandwidth Unique Challenges

- Massive amount of High Performance IO can be used for DDR4

<table>
<thead>
<tr>
<th>Feature</th>
<th>Kintex</th>
<th>Kintex Ultra-Scale</th>
<th>Virtex Ultra-Scale</th>
<th>Virtex</th>
<th>Virtex Ultra-Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells (LC)</td>
<td>478</td>
<td>1,161</td>
<td>1,995</td>
<td>4,407</td>
<td></td>
</tr>
<tr>
<td>Block RAM (BRAM; Mbits)</td>
<td>34</td>
<td>76</td>
<td>68</td>
<td>115</td>
<td></td>
</tr>
<tr>
<td>DSP48</td>
<td>1,920</td>
<td>5,520</td>
<td>3,600</td>
<td>2,880</td>
<td></td>
</tr>
<tr>
<td>Peak DSP Performance (GMACs)</td>
<td>2,845</td>
<td>8,180</td>
<td>5,335</td>
<td>4,268</td>
<td></td>
</tr>
<tr>
<td>Transceiver Count</td>
<td>32</td>
<td>64</td>
<td>96</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>Peak Transceiver Line Rate (Gbps)</td>
<td>12.5</td>
<td>16.3</td>
<td>28.05</td>
<td>32.75</td>
<td></td>
</tr>
<tr>
<td>Peak Transceiver Bandwidth (Gbps)</td>
<td>800</td>
<td>2,086</td>
<td>2,784</td>
<td>5,101</td>
<td></td>
</tr>
<tr>
<td>PCI Express Blocks</td>
<td>1</td>
<td>6</td>
<td>4</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>100G Ethernet Blocks</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>150G Interlaken Blocks</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>Memory Interface Performance (Mbps)</td>
<td>1,866</td>
<td>2,400</td>
<td>1,866</td>
<td>2,400</td>
<td></td>
</tr>
<tr>
<td>I/O Pins</td>
<td>500</td>
<td>832</td>
<td>1,200</td>
<td>1,456</td>
<td></td>
</tr>
</tbody>
</table>
High Speed High Performance IO supports many memory interface; hence, the IO capacitance is higher than in ASIC design.

<table>
<thead>
<tr>
<th></th>
<th>Memory IO Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR4</td>
<td>POD12</td>
</tr>
<tr>
<td>DDR3</td>
<td>SSTL15</td>
</tr>
<tr>
<td>DDR3L</td>
<td>SSTL135</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>HSUL</td>
</tr>
<tr>
<td>RLDRAM3</td>
<td>SSTL12</td>
</tr>
<tr>
<td>QDR4</td>
<td>HSTL/SSTL:1.2V,1.25V POD:1.1V,1.2V</td>
</tr>
<tr>
<td>QDR2+</td>
<td>HSTL:1.2V,1.8V</td>
</tr>
</tbody>
</table>
High Performance IOs are located at the center of the package, IO breakouts are more susceptible to cross talk.
High Speed Parallel Bus System Considerations

What is the memory interface speed?
What is the memory devices variations & electrical limits?
What is the electrical channel characteristics?
What is the optimal design space?
High Speed Parallel IO Bus System Design Flow

1. Memory System Analysis Start
   - $i = 0$
   - Channel Config$_i$
   - Set Up Design Of Experiment Runs
   - Analyze Factors Main Effects On Output Response

2. Enablers
   - $i = i++$
   - Meet Budget ?

3. End
   - Yes
   - No
Statistical Design Of Experiment Approach

1. Identify the performance output (Response)
2. Identify the design factors (parameters) limits
3. Create design run table & simulate response(s)
4. Analyze response & Identify key design parameters from Prediction Profiles
Design Parameter Table & Design Data Eye Response

<table>
<thead>
<tr>
<th>Design Factors</th>
<th>Low Limits</th>
<th>Up Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drv Slew Rate (V/ns)</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>Drv Impedance (Ω)</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>Drv Supply (V)</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Impedance (Ω)</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>Board</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Impedance (Ω)</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>DRAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dram Cap Load</td>
<td>-1</td>
<td>+1</td>
</tr>
<tr>
<td>Rtt</td>
<td>-1</td>
<td>+1</td>
</tr>
</tbody>
</table>
IO Key Features to Enable DDR4 Interface

- **Mother Board via Improvement Quantification**
  - Upper Routing vs Lower Routing improvement

- **Tx Feature**
  - POD12 Driver with De-emphasis Equalization

- **Rx Feature**
  - Continuous Time Linear Equalization

- **De-skew Feature**
  - Data (DQ) & Data Strobe (DQS) per bit de-skew
Mother Board Via Cross Talk Quantification

Graph showing the quantification of via cross talk with frequency (GHz) on the x-axis and dB on the y-axis. Two sets of via connections are illustrated, one with Via effective length indicated, and the other with routing on upper and lower layers. The graph compares Blue: deep layer via vs Red: upper layer via.
Upper and Lower Routing Eye Diagram Comparison

Lower Layer

Upper Layer

~ 7.2% jitter improvement using upper layer
2 tap De-emphasis Spec(dB) = \(-20 \log_{10}\left(\frac{V_{shelf}}{V_{swing}}\right)\)

\[
\sum_{k=0}^{\infty} |c_k| = 1
\]
Write Data Eye Improvement with De-emphasis

\[ S21(\text{dB}) \rightarrow \text{With De-emphasis} \sim 4\% \text{ improvement} \]
Receiver Continuous Time Linear Equalizer

Level1
Level2
Level3
Level4

FPGA

DQ0 (I/O)
DQ1 (I/O)
DQS (I/O)
DQS# (I/O)
CTLE
RCV
DQ7 (I/O)

DRAMs

DQ0 (I/O)
DQ1 (I/O)
DQS (I/O)
DQS# (I/O)
DQ7 (I/O)
Read Data Eye Improvement with CTLE Improvement

\[ \text{S21 (dB)} \]

\[ \rightarrow \text{With CTLE} \sim 9.6\% \text{ improvement} \]
Per Bit De skew Capability

FPGA

CK_GEN

Delay

DRAMs
Experimental Data Validation

- Validation System Configuration
- Write Shmoo Procedure Overview
- Read Shmoo Procedure Overview
- Data Eye Scope Capture
- Over Clocking Results
Validation System

- DIMM
- FPGA
- 4 DRAMs
- 5 DRAMs
- 9 DRAMs
Write Shmoo Margining Test Flow

Write DQS pushes to find the min. passing eye

Margining
Shmoo

DQ[7:0]
DQS_w

Delayed DQS_w

Margin

FPGA

Write DQ[7:0] FPGA Internal Cal.

Strobe position

DRAM @Vref_i

DQ[7:0] DQS_r

DRAM Vref_i+1

DRAM Vref_i

DRAM Vref_i-1

= Starting Pt

After Calibration

= FPGA Internal Cal.

Strobe position

#DC15
Read Shmoo Margining Test Flow

Write Data Send to DRAM (like regular Write)

FPGA @Vref_ j

Read Margining

DQ[7:0]

DQS_w

DRAM

= Starting Pt

After Calibration

= FPGA Internal Cal. Strobe position

FPGA Vref_ j+1

FPGA Vref_ j

FPGA Vref_ j-1

DQ[7:0]

DQS_r
Write and Read Eye Shmoo at 2400MTs

Write Eye Shmoo

Read Eye Shmoo

UI
DDR4 Memory Write Eye (Scope) Measurement
Write Eye Capture at 2400MTs

Probes Attachment

Write Data Eye Capture
Over Clocking Results
(at 2933MTs)

No Error

System Clock has low Jitter.

Data Eye has sufficient margin.
Summary & Conclusions

- A top down systematic approach using statistical DOE enabled an effective method to ensure design robustness.
- System enablers such as routing selection, IO equalization circuits improvement were quantified.
- Validation procedures and empirical data showed healthy margin for the DDR4 running at 2400MTs.
- Over clocking data indicated that the Interface is functioning at 2993MTs with lower system clock jitter and sufficient data eye margin.