ULTRASCALE DDR4 DE-EMPHASIS AND CTLE FEATURE OPTIMIZATION WITH STATISTICAL ENGINE FOR BER SPECIFICATION
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Outline

- DDR4 feature and design challenge
- FPGA DDR system design challenge
- DDR4 statistical simulation method
- DDR4 De-emphasis and CTLE optimization result discussion
# DDR4 Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.5V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Max Datarate (Mbps)</td>
<td>2133</td>
<td>3200</td>
</tr>
<tr>
<td>DQ Bus</td>
<td>SSTL15</td>
<td>POD12</td>
</tr>
<tr>
<td>DQ Vref</td>
<td>external</td>
<td>Internal</td>
</tr>
<tr>
<td>DQ Driver</td>
<td>40 (ohm)</td>
<td>48(ohm)</td>
</tr>
</tbody>
</table>
FPGA DDR4 Design Challenges

- DDR4 Design Challenge
  - Higher datarate, Higher loss, intensified ISI

- FPGA Configurable I/O standards
  - DDR3, DDR3L, DDR4, LPDDR2, LPDDR3, RLDRAM3, QDR2+, QDR4
  - High pad capacitance: FPGA ~3.5pF Vs. ~1.8pF ASIC

- FPGA High I/O count
  - Up to ~1400 IO counts in Ultrascale family
  - High density signal routing
  - High signal to ground ratio

- Signal enhancement techniques to mitigate
  - De-emphasis & CTLE
FPGA DDR4 Design Challenges
Traditional DDR Design Methodology

- Run transient simulation using IBIS or SPICE models of controller and memory
- Measure setup and hold times on waveforms
ISI at Low Speed

800 Mb/s

- Timing margin deceases by 1% UI from $10^3$ bits to $10^{16}$ bits
- At low speed, limited number of bits is adequate for system verification

Border of traces of $10^3$ bits

Border of traces of $10^{16}$ bits

5” DQ line
ISI at High Speed

3200 Mb/s

- Timing margin decreases by 9% UI from $10^3$ bits to $10^{16}$ bits
- At high speed, design needs to be verified at target BER
DQ Rx Mask Spec in DDR4

- Mask consists of deterministic and random portions
- BER inside the total mask must be below $10^{-16}$
Statistical Simulation for BER

- It’s impractical to simulate $10^{16}$ bits to estimate BER at $10^{-16}$
- Statistical method can be employed to calculate eye probability distributions
- Equivalent to running infinite number of bits
- BER can be obtained rigorously at arbitrarily low level
Linear Superposition

\[ v(t) = \sum_{i} \left\{ R[t - n_r(i) \cdot T - \tau(n_r(i))] - F[t - n_f(i) \cdot T - \tau(n_f(i))] \right\} + v_0 \]

\( R(t) \): rise edge step response
\( F(t) \): fall edge step response
\( T \): UI
\( \tau \): transmitter jitter
Transmitter Jitter

Jitter components include DCD, SJ and RJ

\[
\tau(n_r) = - \frac{DCD_{pp}^{data}}{2} - (-1)^{n_r} \frac{DCD_{pp}^{clk}}{2} + A \sin(2\pi f n_r T + \phi) + \rho(n_r)
\]

\[
\tau(n_f) = \frac{DCD_{pp}^{data}}{2} - (-1)^{n_f} \frac{DCD_{pp}^{clk}}{2} + A \sin(2\pi f n_f T + \phi) + \rho(n_f)
\]

DCD_{pp}^{data} : peak-to-peak data DCD
DCD_{pp}^{clk} : peak-to-peak clock DCD
A & f: SJ amplitude and frequency
\rho: RJ
Eye Probability Distribution

\[ p(v,t) = \frac{1}{2\pi} \int_{0}^{2\pi} d\phi \frac{1}{2^M} \sum_{m=1}^{2^M} \int \delta[v - v^{(m)}(t)] \prod_{i} g[\rho(n_{r}^{(m)}(i))] \cdot g[\rho(n_{f}^{(m)}(i))] \cdot d\rho(n_{r}^{(m)}(i)) \cdot d\rho(n_{f}^{(m)}(i)) \]

- \( m \): pattern index
- \( M \): step response settle time in bit
- \( g \): RJ PDF

- Tx jitter affects the output distribution through channel step responses
- Jitter effect is directly handled in PDF calculation instead of post-processing
- PDF is computed rigorously using efficient algorithms w/o approximation
- Accurate prediction of BER
Crosstalk

Crosstalk is additive noise to victim signal

Included by convolution between victim PDF and crosstalk PDF

\[ p(v, t) = \int p_{\text{victim}}(v - v_1 - v_2 \cdots - v_n, t) p_{\text{xtlk}}^{(1)}(v_1, t) p_{\text{xtlk}}^{(2)}(v_2, t) \cdots p_{\text{xtlk}}^{(n)}(v_n, t) dv_1 dv_2 \cdots dv_n \]
Driver De-emphasis

w/o de-emphasis

3dB de-emphasis
Rx CTLE

\[ H(s) = A \frac{(s - z_1) \ldots (s - z_n)}{(s - p_1) \ldots (s - p_k)} \]
Asymmetric Rise and Fall Edges Capability

- Rise time > fall time
- Rise time < fall time
Timing and Voltage Margins

- Timing and Voltage margins are measured at each mask corner
- Ring-back is captured by minimum voltage margins
CTLE Optimization

- **CTLE design parameters**
  - f_z (zero), f_p1 (first pole), f_p2 (second pole), G_{dc} (dc gain)

\[
H_{CTLE}(s) = c \frac{(s + w_{zero})}{(s + w_{pole1})(s + w_{pole2})}
\]

\[
c = G_{dc} \frac{w_{pole1} \cdot w_{pole2}}{w_{zero}}
\]
CTLE Optimization

- CTLE fz sensitivity sweep for two study channels
  - BER $10^{-16}$ eye width @ Vref +/−68mV saturated after 600Mhz fz
CTLE Optimization

**CTLE fp1 Vs. Gain_dc sensitivity sweep at 4.5GHz bandwidth**

- BER $10^{-16}$ eye width not sensitive to fp1 around 1.2GHz
- BER $10^{-16}$ eye width increase with higher Gain_dc

BER 10-16 eye width from fp1 and gain_dc at 4.5GHz bandwidth (fp2)
CTLE Optimization

CTLE fp1 Vs. Gain_dc sensitivity sweep at 6 GHz bandwidth

- BER $10^{-16}$ eye width not very sensitive to fp2 around 5GHz
- BER $10^{-16}$ eye width increase with higher Gain_dc
CTLE Optimization -- 2400Mbps DDR4

significant BER $10^{-16}$ eye width opening is achieved with optimized CTLE
De-emphasis Optimization

- De-emphasis dB level is defined as
  \[ 20 \log_{10}(V_{de}/V_{pre}) \]
De-emphasis Optimization

Optimal De-emphasis dB can be identified for driver slew rate

[Graph showing eye width (ps) at Vref +/- 68mV vs. De-emphasis dB and Driver slew rate rise time (ps)]
De-emphasis Optimization – 2400Mbps DDR4

- 10-20ps BER $10^{-16}$ eye width opening achieved with optimized dB setting
Summary

- A statistical simulation engine is introduced for designing DDR4 system to JEDEC 10-16 BER target.
- Effects of driver de-emphasis and Rx CTLE on DDR4 timing at BER target of 10-16 are investigated.
- De-emphasis and CTLE are effective techniques to mitigate jitter and achieve DDR4 design target after optimization.