Characterization of DDR4 Receiver Sensitivity Impact on Post-equalization Eye

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Outline

- Typical DDR System Configuration
  - Channel Signal Attenuation
  - Simple DDR Receiver and Input Mask
  - Jitter Measurement Point for Simple DDR Receiver

- Problem Statement
  - Traditional Simulation Approach with CTLE receiver

- CTLE Receiver and Output Eye Mask
  - Overview of CTLE in Signal Improvement
  - CTLE Receiver incorporation in Memory System & Output Mask Definition

- Channel Simulation in DDR4 system
  - Traditional Simulation Approach with CTLE receiver
  - DJ Incorporation in Statistical Simulation approach

- Conclusion
A Typical DDR System & Channel Attenuation

→ DDR Channel Attenuation becomes more significant as data rate increases!
Voltage and Timing Sensitivity (Rx Mask) is to guarantee Rx to capture correct signal state.
Jitter Measurement Point for Simple DDR Receiver

Timing jitter measurement at the Rx Mask defined threshold.
CTLE improves incoming signal jitter.
One way is to impose Rx input threshold to the output of the CTLE Rx.
This leads to pessimistic jitter measurement!
CTLE High Frequency Roll Off

→ CTLE has active gain stage.
→ CTLE uses degeneration resistor & capacitor to tune low to high freq. ratio

\[ \omega_z = \frac{1}{CR} \]  \hspace{1cm} (1)

\[ \omega_{p1} = \frac{1+g_mR/2}{CR} \]  \hspace{1cm} (2)

\[ \omega_{p2} = \frac{1}{C_L R_L} \]  \hspace{1cm} (3)

Diagram showing frequency response, gain over frequency, and high frequency roll-off.
CTLE in Memory System (One Byte)

→ CTLE implemented in a DDR System.
CTLE in Memory System Improvement

→ CTLE improves incoming signal edge rate.
Data Signal Eye Improvement after CTLE

→ CTLE output will have common mode variation.
Channel Simulation in DDR4 System

→ Jitter should be considered with CLTE output common mode variation.
→ Sampling Flop Set up time reference to Vtrip of CMOS logic.
Proposed Simulation Approach at Post Equalization Eye with Rx Sensitivity Impact

→ Jitter measurement with mapping Rx DJ to Rx Vref.
→ Similar concept can apply to incorporate power supply noise induced DJ
DDR4 Channel Simulation Test Bench

→ Using Input threshold for post CTLE jitter measurement lead to pessimism.
Measure Functional Eye for sampling flop.
→ Functional Eye measured at Vref is within 5% of prediction.
→ Relative Light Traffic Test Case.
Post CTLE DQ Eye Jitter with Power Supply Noise

→ Jitter measurement after mapping to $V_{trip}$ for sampling flop.
Summary & Conclusions

- DDR Channel Attenuation becomes more significant as data rate increase.
- More precise system timing methodology is needed to accurate predict the timing analysis.
- New approach to analyze the system timing was presented using DJ to map the jitter measurement threshold voltage point to the $V_{trip}$.
- New design features for jitter measurement was proposed as a critical design parameters.
- Receiver and Channel co-design is critical in future DDR interface design to enable robust channel timing.
Thank you!

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QUESTIONS?