End-to-End System-Level Simulations with Repeaters for PCIe Gen4: A How-To Guide

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PCI-Express Gen-4 Overview

- **PCI-Express Gen-4:**
  - Base Specification revision 4.0 expected to reach version 1.0 in 2017
  - Maximum speed: 16 Gbps / Lane / direction
  - Single- or multi-lane links to scale aggregate bandwidth: x1, x2, x4, x8, x16, and x32

- **Applications:**
  - Servers: CPU-to-network and CPU-to-storage interconnects
  - Client compute: CPU-to-peripheral (i.e. graphics card) interconnect
  - High-performance compute / Compute clusters: CPU-to-CPU interconnect
PCI-Express Gen-4 System Topologies

- System designers anticipate various topologies ranging from one to five connectors.

- High channel attenuation:
  - ~5 dB from CPU package
  - ~3 dB from End Point package
  - ~1 dB from each connector
  - ~1 dB / inch from PCB

- Linear Repeaters are commonly used to achieve reach extension while minimizing added latency, cost, and power consumption.

- System designers need a way to gain confidence in their chosen topology and its viability.

- System-level simulations are one way to achieve this goal.
End-to-End System-Level Simulations

- The proposed methodology for simulating a \textit{Tx+Repeater+Rx system} in the context of PCIe Gen-4:
  1. Determine if a Repeater is required.
  2. Define a simulation space.
  3. Define evaluation criteria.
  4. Execute the simulation matrix and analyze the results.

- **Goal:** Reach a conclusion regarding the optimum configuration of the system in an efficient and timely manner.
Step 1: Determine if a Repeater is Necessary

Two ways to determine if a Repeater is necessary:

1. Compare end-to-end channel loss to PCIe channel requirements
2. Simulate end-to-end channel s-parameter in Seasim

PCIe Gen-4 topology considered for this presentation:

Add-in Card (AIC)

- RC
- EP
- Package
- AC cap
- PCIe connector

Main Board

- RC
- Package
- AC cap
- PCIe connector
- ~7 inches
- ~4 inches
- ~2 inches
- ~2 inches
- ~1 inch
- ~5 inches

When Repeater on Main Board
When Repeater on Riser Card
Step 1: Determine if a Repeater is Necessary

<table>
<thead>
<tr>
<th>Channel analysis method</th>
<th>Value</th>
<th>PCIe Requirement</th>
<th>Conclusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. End-to-end channel insertion loss</td>
<td>38.8 dB at 8 GHz</td>
<td>≤ 20.5 dB at 8 GHz</td>
<td>Repeater is required</td>
</tr>
<tr>
<td>2. Channel simulation with behavioral Tx, Rx, and package</td>
<td>EH = 8.7 mV EW = 0.395 UI</td>
<td>EH ≥ 15 mV EW ≥ 0.3 UI</td>
<td>Repeater is required</td>
</tr>
</tbody>
</table>
Step 2: Define a Simulation Space

The system-level simulation task is broken down into two sequential phases:

1. **Initial link performance analysis.** Analyze the impact of Repeater placement and Tx/Repeater/Rx settings on link performance.

2. **Sensitivity analysis.** Quantify the sensitivity of link performance to process/voltage/temperature (PVT) variation and to variations in Repeater placement.

<table>
<thead>
<tr>
<th>Simulation Phase</th>
<th>RC Tx Parameters</th>
<th>Repeater Parameters</th>
<th>EP Rx Parameters</th>
<th>Channel Parameters</th>
</tr>
</thead>
</table>
| 1. Initial link performance analysis | Presets: 0, 1, ..., 9  
VOD: 1000 mVppd | Boost: Sweep six values  
Wide-band gain: -1 dB | Rx parameters automatically adaptive | Channel topologies considered:  
1. Repeater placed on Main Board  
2. Repeater placed on Riser Card |
| 2. Sensitivity analysis | Presets: 0, 1, ..., 9  
VOD: 1000 mVppd | Boost: Optimum setting from Phase 1  
Wide-band gain: ±4 dB | Rx parameters automatically adaptive | Focus on optimum topology. Vary specific Repeater placement by ±2 inch to assess sensitivity to placement. |
Root Complex Tx Parameters

- A Xilinx FPGA SerDes is used as the Root Complex Tx in this analysis.
- It implements a three-tap FIR filter which can be configured to achieve any of the ten PCIe Presets.

<table>
<thead>
<tr>
<th>Preset #</th>
<th>Preshoot (dB)</th>
<th>De-emphasis (dB)</th>
<th>$c_1$</th>
<th>$c_{+1}$</th>
<th>Va/Vd</th>
<th>Vb/Vd</th>
<th>Vc/Vd</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4</td>
<td>0.0</td>
<td>0.0</td>
<td>0.000</td>
<td>0.000</td>
<td>1.000</td>
<td>1.000</td>
<td>1.000</td>
</tr>
<tr>
<td>P1</td>
<td>0.0</td>
<td>-3.5 ± 1</td>
<td>0.000</td>
<td>-0.167</td>
<td>1.000</td>
<td>0.668</td>
<td>0.668</td>
</tr>
<tr>
<td>P0</td>
<td>0.0</td>
<td>-6.0 ± 1.5</td>
<td>0.000</td>
<td>-0.250</td>
<td>1.000</td>
<td>0.500</td>
<td>0.500</td>
</tr>
<tr>
<td>P9</td>
<td>3.5 ± 1</td>
<td>0.0</td>
<td>-0.166</td>
<td>0.000</td>
<td>0.668</td>
<td>0.668</td>
<td>1.000</td>
</tr>
<tr>
<td>P8</td>
<td>3.5 ± 1</td>
<td>-3.5 ± 1</td>
<td>-0.125</td>
<td>-0.125</td>
<td>0.750</td>
<td>0.500</td>
<td>0.750</td>
</tr>
<tr>
<td>P7</td>
<td>3.5 ± 1</td>
<td>-6.0 ± 1.5</td>
<td>-0.100</td>
<td>-0.200</td>
<td>0.800</td>
<td>0.400</td>
<td>0.600</td>
</tr>
<tr>
<td>P5</td>
<td>1.9 ± 1</td>
<td>0.0</td>
<td>-0.100</td>
<td>0.000</td>
<td>0.800</td>
<td>0.800</td>
<td>1.000</td>
</tr>
<tr>
<td>P6</td>
<td>2.5 ± 1</td>
<td>0.0</td>
<td>-0.125</td>
<td>0.000</td>
<td>0.750</td>
<td>0.750</td>
<td>1.000</td>
</tr>
<tr>
<td>P3</td>
<td>0.0</td>
<td>-2.5 ± 1</td>
<td>0.000</td>
<td>-0.125</td>
<td>1.000</td>
<td>0.750</td>
<td>0.750</td>
</tr>
<tr>
<td>P2</td>
<td>0.0</td>
<td>-4.4 ± 1.5</td>
<td>0.000</td>
<td>-0.200</td>
<td>1.000</td>
<td>0.600</td>
<td>0.600</td>
</tr>
</tbody>
</table>

De-emphasis = 20 log₁₀ Vb/Va
Preshoot = 20 log₁₀ Vc/Va
Boost = 20 log₁₀ Vd/Vb
Repeater Parameters

- A Texas Instruments Linear Repeater is used to extend the reach between the RC and EP.
- Linear Repeaters conventionally provide two mechanisms for signal conditioning: **High-frequency boost** and **wide-band amplitude gain**.

![Graph showing gain vs. frequency for Linear Repeaters](image)

- Linear Repeaters are usually configured to slightly under-equalize the pre-channel.
- Small wide-band gain (-1dB) simulated for Phase 1.
Step 3: Define Pass/Fail Criteria

- Bit error rate (BER) is the ultimate gauge of link performance, but an accurate measure of BER is not possible in relatively short, multi-million-bit simulations.

- Instead, the methodology proposed here uses two criteria to establish link performance:
  1. A link must meet receiver’s EH and EW requirements
  2. A link must meet criterion 1 for all Tx Preset settings

Criterion 1 establishes that there is a viable set of settings which will result in the desired BER.

Criterion 2 ensures that the link has adequate margin and is not overly-sensitive to the Tx Preset setting.
Step 4: Execute and Analyze

- IBIS-AMI models are used for each active component: RC and EP SerDes from Xilinx and Linear Repeater from Texas Instruments.

- Keysight ADS is used to execute the IBIS-AMI simulations, measure the extrapolated EH and EW, and plot post-equalized eye.

Simulation Schematic used for this Analysis
The focus of Phase 1 is to run a broad set of relatively short simulations to explore the design solution space. Minimizing the simulation time for each simulation is crucial.

<table>
<thead>
<tr>
<th>Simulation Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>16.0 GT/s</td>
</tr>
<tr>
<td>Data Pattern</td>
<td>PRBS31</td>
</tr>
<tr>
<td>Total number of bits</td>
<td>1 Million</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>Yes. Two far-end crosstalk (FEXT) aggressors.</td>
</tr>
<tr>
<td>Ignore_Bits</td>
<td>500k</td>
</tr>
<tr>
<td></td>
<td>Note: This is set by the Rx model</td>
</tr>
<tr>
<td>Simulation type</td>
<td>Time domain (a.k.a. bit-by-bit)</td>
</tr>
<tr>
<td></td>
<td>Note: Simulations will be faster running in Statistical mode, however non-linear behavior may not be adequately represented.</td>
</tr>
<tr>
<td>Bit-by-bit extrapolation</td>
<td>Enabled</td>
</tr>
<tr>
<td></td>
<td>Note: Simulations will be faster without this mode enabled, however RJ will not be accounted for as accurately.</td>
</tr>
</tbody>
</table>
Step 4 (Phase 1): Initial Link Performance Analysis

**Bottom-left:** EH and EW pass/fail result for each Tx Preset (horizontal axis) and Repeater boost setting (rows, in dB)

**Right:** Average EH/EW for each Repeater boost setting

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**Introduction**

- Repeater Required?
- Define Sim Space
- Define Pass Criteria
- Conclusion

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**Execute & Analyze**

- **Bottom-left:** EH and EW pass/fail result for each Tx Preset (horizontal axis) and Repeater boost setting (rows, in dB)
- **Right:** Average EH/EW for each Repeater boost setting

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**Rx Post-Equalized EW (UI) vs. Repeater Boost (dB)**

- EH requirement (pass)
- EW requirement (pass)

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**Rx Post-Equalized EH (mV) vs. Repeater Boost (dB)**

- EH requirement (pass)
- EH requirement (marginal)

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**Preset**

- 0 1 2 3 4 5 6 7 8 9

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**UBM**
Step 4 (Phase 1): Initial Link Performance Analysis

Post-equalized eye diagram for all Tx Preset settings. The optimum Repeater boost (20.5 dB) is used for these cases. Tx Preset 8 yields the largest post-equalized eye opening.
Step 4 (Phase 1): Initial Link Performance Analysis

- A similar analysis is conducted for the alternate placement: Repeater on the Riser Card.
- In this configuration, the pre-channel loss is $\sim 25$ dB at 8 GHz; post-channel loss is $\sim 14$ GHz at 8 GHz.
- This placement shows consistently reduced performance compared to Main Board placement of the Repeater.

Repeater on Main Board, Preset 8, Boost=20.5 dB

Repeater on Riser Card, Preset 9, Boost=20.5 dB
Step 4 (Phase 2): Sensitivity to Placement

- Optimum Repeater placement is on the Main Board.
- Analyze the sensitivity of link performance due to the specific placement of the Repeater.
- Simulations are run with a ±2 inch variation in Repeater placement.

![Diagram of Repeater Placement]

- Closer to EP:
  - Root Complex (RC) to Main Board: 10 inches
  - Repeater: 2 inches
  - Riser Card: 5 inches
  - Add-In Card: 5 inches
  - End Point (EP): 2 inches

- Closer to RC:
  - Root Complex (RC) to Main Board: 8 inches
  - Repeater: 4 inches
  - Riser Card: 5 inches
  - Add-In Card: 5 inches
  - End Point (EP): 2 inches

±2 inches variation.
Step 4 (Phase 2): Sensitivity to Placement

**Introduction**

**Question:** Does the optimum Repeater setting change with a relatively minor shift in the specific placement?

**Answer:** No. Both plots peak at the same setting.
The last part of the Phase 2 sensitivity analysis is to look at the sensitivity of link performance to process, voltage, and temperature (PVT) variations.

To exacerbate the effects of PVT variation, the Repeater’s wide-band gain is varied by ±4 dB.

Overall link performance is not affected until both extremes of PVT variation and wide-band gain are realized.

As long as the Repeater’s wide-band gain setting is kept to a reasonable, mid-level value, the link performance will be robust across PVT corners.
Conclusions

A simple four-step process for evaluating Root Complex + Repeater + End Point PCIe Links:

Determine if a Repeater is necessary
- Does end-to-end channel exceed PCIe Base Specification?
- Does channel fail Seasim EH/EW analysis?

Setup simulation sweep space
- Include all Tx Presets
- Chose Repeater boost around pre-channel loss

Define a pass/fail criteria
- Final Receiver’s post-equalized eye height (EH) and eye width (EW)
- Achieving Rx EH/EW requirements across all Tx Presets

Execute simulation matrix
- Phase 1: Initial link performance analysis (simulating the sweep space)
- Phase 2: Understand link’s sensitivity to specific Repeater placement and PVT

Understand if reach extension device is needed.

Chose limited set of parameters which are most likely to impact system performance.

Define evaluation criteria up front to avoid subjective conclusions later on.

Break execution into two phases to minimize overall simulation time.
Thank you!

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QUESTIONS?
Appendix: Terminology

- **Root Complex (RC)** A defined System Element that includes at least one Host Bridge, Root Port, or Root Complex Integrated Endpoint.

- **End Point (EP)** One of several defined System Elements. A Function that has a Type 00h Configuration Space header.

- **Linear Repeater** An analog reach extension device which generally provides continuous time linear equalization (CTLE) and wide-band amplitude gain.

- **Link** The collection of two Ports and their interconnecting Lanes. A Link is a dual-simplex communications path between two components.

- **Link Segment** The collection of a Port and a Pseudo Port or two Pseudo Ports and their 45 interconnecting Lanes. A Link Segment is a dual simplex communications path between a Component and a Retimer or between two Retimers (two Pseudo Ports).