Introducing the Versal Architecture

Presented By

Sumit Shah
Director of Silicon Product Marketing and Management
October 2, 2018
The Technology Conundrum .. And the Need for a New Compute Paradigm

Processing Architectures are Not Scaling

40 YEARS OF PROCESSOR PERFORMANCE

A Single Architecture Can’t Do It Alone

- Safety Processing, or Latency-Critical Workloads
- Irregular data types, instruction sets, data operation
- Domain Specific Parallelism (e.g., Video, ML)
- Sensor Fusion, Pre-Processing, Data Aggregation
- Complex Algorithms, Full Linux “Services”

Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e 2018
Need for a New Programming Paradigm

Software Developer
Needs Agility and Abstraction

Need a Scalable, Unified Platform

Hardware Developer
Needs Flexibility to Optimize for Performance/Power

Ecosystem of Libraries

Familiar Platform

Modify, Design, Add Code

Flexible Platform to Optimize for Performance/Power
New Device Category: Adaptive Compute Acceleration Platform

**COMPUTE ACCELERATION**

- **Scalar Engines**
- **Adaptable Engines**
- **Intelligent Engines**

**ADAPTIVE**

- Diverse Workloads in Milliseconds
- Future-Proof for New Algorithms

**PLATFORM**

- Development Tools
- HW/SW Libraries
- Run-time Stack
- SW Programmable Silicon Infrastructure

Enabling Data Scientists, SW Developers, HW Developers

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Introducing the World’s First ACAP

> Heterogeneous Acceleration
> For Any Application
> For Any Developer
Breakthrough Performance for Cloud, Network, and Edge

**Cloud Compute**
Breakthrough AI Inference

- GoogleNet V1 Img/Sec (<2ms)
  - High-End GPU: 1
  - Versal Device: 8x

**Networking**
Multi-terabit Throughput

- Single-Chip Encrypted Traffic (Gbps)
  - UltraScale+ FPGA: 1
  - Versal Device: 4x

**5G Wireless**
Compute for Massive MIMO

- Int.16x16 DSP Compute (TeraMAC/ sec)
  - UltraScale+ RFSoC: 1
  - Versal Device: 5x

**Edge Compute**
AI Inference at Low Power

- ResNet50 Img/sec (batch=1)
  - UltraScale+ MPSoC: 1
  - Versal Device: 15x
Versal Architecture Overview

Adaptable Engines
- 2X compute density

Intelligent Engines
- AI Compute
- Diverse DSP workloads

Network-on-Chip
- Guaranteed Bandwidth
- Enables SW Programmability

DDR Memory
- 2X bandwidth/pin
- Server-class density

Scalar Engines
- Arm Cortex-A72 Application Processor
- Arm Cortex-R5 Real Time Processor

Protocol Engines
- Integrated 600G cores
- 4X encrypted bandwidth

Programmable I/O
- Any sensor, any interface
- Extendable peripheral set

Transceivers
- Broad range, 25G →112G
- 58G in mainstream devices

PCle & CCIX
- 2X PCIe & DMA bandwidth
- Cache-coherent interface to accelerators
Platform Management Controller
Bringing the Platform to Life & Keeping it Safe & Secure

Boot & Configuration
> Boots the platform in milliseconds (any engine first)
> 8X faster dynamic reconfiguration
> Advanced power & thermal management

Security, Safety & Reliability Enclave
> HW Root of Trust
> Cryptographic acceleration & confidentiality
> Enhanced diagnostics, system monitoring & anti-tamper
> Error mitigation, detection & management for safety

Integrated Platform Interfaces & High Speed Debug
> Integrated flash, system & debug interfaces
> High-speed non-invasive, chip-wide debug
A Processor in Every Device
Diverse Use Models for Scalar Processing

Edge Compute & Autonomous Systems
Complex processing for intelligent edge and endpoint

Control Plane Processing in the Network & Cloud
Data path management & device management

Operation & Management in Communication Systems
Board level control monitoring
The Arm Subsystem

Dual-Core ARM Cortex-A72 Application Processors

> Up to 1.7GHz for 2X single-threaded performance
> Cost and power optimized (half the power)
> Code compatibility (ARMv8-A architecture)
> Enables SW developers to start from a familiar place

Dual-Core ARM Cortex-R5 Real Processors

> Up to 750MHz for 1.4X greater performance
> Low latency and deterministic
> Flexible operation modes: Split-Mode and Lock-Step
> Highest levels of functional safety (ASIL and SIL)

1: DMIPS vs. Zynq UltraScale+ MPSoCs
Adaptable Engines

Adaptable Hardware Engines

Programmable logic for fine-grained parallel processing, data aggregation, and sensor fusion

Programmable memory hierarchy to optimize compute efficiency

High bandwidth, low latency data movement between engines and I/O
Greater Compute Density for Any Workload

Re-Architected Hardware Fabric
> 4X density per logic block for more compute
> Less external routing → greater performance
> Code and IP compatible with 16nm devices

Tune for Power & Performance
> Three operating voltages to choose from
> Balance power/performance for target app
> Equivalent to 3 speed grades in one device

Adaptable to any Workload
> Bit-level precision (1 → 1,000) for any algorithm
> Improves ML efficiency (compression, pruning)
> Forward-compatible to lower precision neural networks, e.g., BNN

ML Inference and Optimizations (e.g., pruning)

For Any Workload

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Intelligent Engines for Diverse Compute

DSP Engines
High-precision floating point & low latency
Granular control for customized data paths

AI Engines
High throughput, low latency, and power efficient
Ideal for AI inference and advanced signal processing
DSP Engines
Versatility and Granular Control of Data Path

Enhanced Compute architecture
> Greater than 1GHz of performance

Versatility for Wireless, ML, HPC, and more
> Integrated FP32, FP16 floating point, INT24 (HPC)
> Integrated complex 18x18 operation (wireless, cable access)
> Double the performance in INT8 operation (AI inference)

Code Portability for UltraScale+ 16nm designs
> Support for legacy IP and LogiCore libraries
> Compatibility with SysGen, Model Composer, HLS tools

Performance Improvement
- UltraScale+ 16nm
- Versal 7nm

Int8 Dot Product: 2.2X
Complex 18x18: 3.3X
32-bit Single Precision Floating Point: 3.6X
1.3GHz VLIW / SIMD vector processors
> Versatile core for ML and other advanced DSP workloads

Massive array of interconnected cores
> Instantiate multiple tiles (10s to 100s) for scalable compute

Terabytes/sec of interface bandwidth to other engines
> Direct, massive throughput to adaptable HW engines
> Implement core application with AI for “Whole App Acceleration”

SW programmable for any developer
> C programmable, compile in minutes
> Library-based design for ML framework developers
NoC for Ease of Use, Guaranteed Bandwidth, and Power Efficiency

High bandwidth terabit network-on-chip
  > Memory mapped access to all resources
  > Built-in arbitration between engines and memory

High Bandwidth, Low Latency, Low power
  > Guaranteed QoS
  > 8X power efficiency vs. FPGA implementations

Eases Kernel Placement
  > Easily swap kernels at NoC port boundaries
  > Simplifies connectivity between kernels
Adaptable Memory Hierarchy

The Right Memory for the Right Job

Scalar Engines
- Arm Cortex-A72
- Cache

Adaptable Engines
- Arm Cortex-R5
- Cache
- TCM
- OCM
- Accelerator RAM

Intelligent Engines
- WORKLOAD_1
- WORKLOAD_N
- UltraRAM
- UltraRAM
- UltraRAM
- UltraRAM
- UltraRAM

AI ENGINES
- PCIe & CCIX
- DDR
- HBM
- SerDes
- Network Cores
- MIPI
- LVDS
- GPIO

Increasing Bandwidth, Decreasing Density

- LUTRAM
  Distributed low-latency memory
- Block RAM & UltraRAM
  Embedded configurable SRAM
- (New) Accelerator RAM
  4 MB sharable across engines
- HBM
  In-package DRAM
- DDR External Memory
  DDR4-3200; LPDDR4-4266

Local data memory in AI engines

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Introducing the “Integrated Shell”

‘Shell’: Pre-Built Core Infrastructure & System Connectivity

- External host interface
- Memory subsystem
- Basic interfaces (e.g., JTAG, USB, GbE)

Key Architectural Elements of the Shell

- Platform Management Controller (PMC)
- Integrated host interfaces: PCIe & CCIX, DMA
- Scalable Memory Subsystem: DDR4 & LPRDDR4
- Network-on-Chip for connectivity and arbitration

Greater Performance, Device Utilization, and Productivity

- More of the platform available for application’s workload(s)
- Target application runs faster with less device congestion
- Turn-key, pre-engineered timing closure – no debug
Transceivers: Robust and Scalable Connectivity

32G NRZ Transceivers
- Optimized for latency and power

58G PAM4 Transceivers
- Tuned for the latest copper cable, backplane & optical interfaces

112G PAM4 Transceivers
- Industry-leading performance for copper cable, backplane, optical

COPPER CABLE
OPTICS
BACKPLANE

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Programmable I/O for Any Sensor, Interface, or Memory

- Different IO types provide a wide range of speeds and voltages
- Configure the same I/O for either memory or sensor interfaces per application requirements

<table>
<thead>
<tr>
<th>DC</th>
<th>400Mb/s</th>
<th>1600Mb/s</th>
<th>3200Mb/s</th>
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HDIO, MIO
(Legacy Standards)

XDIO
(High-Speed)

- 3.2Gb/s MIPI D-PHY
  - 8 Mpix Sensors & Displays
- 3.2Gb/s DDR4
  - Server Class Density Per Channel
- 4.2Gb/s LPDDR4 (0.6V)
  - Highest Memory Bandwidth Per Pin
Versal Core Series Enables “Smart Cities”
Video Surveillance with Machine Learning

Host Connectivity and Network Connectivity
Integrated PCIe and Ethernet

Adaptable Engines Optimize Compute/Watt
Video scaling, custom memory hierarchy, compression

DSP Engines for Video Transcode
Scalable for legacy and emerging video formats

AI Engines for Real-Time Image Recognition
License Plate/Facial Recognition

Network On Chip and Memory Subsystem
Interconnects memory and compute Engines

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For Any Developer

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<tr>
<th>Frameworks</th>
<th>TensorFlow</th>
<th>Caffe</th>
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<td>New Unified Software Development Environment</td>
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Part of the Xilinx Product & Technology Portfolio

DEVICE CATEGORY

- FPGA
- SoC
- ACAP

FEATURED PRODUCTS

- Spartan
- Artix
- Kintex
- Virtex

- Zynq-7000
- Zynq UltraScale+ MPSoC
- Zynq UltraScale+ RFSoC
- Versal
Announcing the First Two Series of the Versal Portfolio

AI Core Series
Breakthrough AI Inference Throughput
> Portfolio’s highest compute and low latency inference
> Optimized for cloud, networking, & autonomous applications
> For highest range of AI and workload acceleration

Prime Series
Broad Applicability Across Multiple Markets
> Mid-range series in the Versal portfolio
> Optimized for connectivity
> For in-line acceleration and diverse workloads
# Versal AI Core Series

<table>
<thead>
<tr>
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<td>Accelerator RAM (Mb)</td>
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<td>Total SRAM Capacity (Mb)</td>
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<td>NoC Master / NoC Slave Ports</td>
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<td>1 x Gen4x16, CCIX</td>
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<tr>
<td>Transceivers</td>
<td>8</td>
<td>44</td>
<td>24</td>
<td>44</td>
<td>44</td>
</tr>
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</table>

**Highest AI Inference Throughput**

50 – 150 INT8 TOPs

**First Available Device**

256Gb/s PCIe & CCIX Bandwidth to Host

**Scalable DDR**

128b – 256b w/ECC

**Enabling Ethernet at**

10G/25G/50G/100G

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## Versal Prime Series

### Intelligent Engines
- **DSP Engines**
  - VM1102: 472
  - VM1302: 736
  - VM1402: 1,504
  - VM1502: 1,312
  - VM1802: 1,968
  - VM1902: 3,984
- **System Logic Cells (K)**
  - VM1102: 352
  - VM1302: 572
  - VM1402: 1,002
  - VM1502: 797
  - VM1802: 1,968
  - VM1902: 2,030

### Adaptable Engines
- **Total SRAM Capacity (Mb)**
  - VM1102: 35
  - VM1302: 63
  - VM1402: 87
  - VM1502: 80
  - VM1802: 164
  - VM1902: 245

### Scalable Engines
- **Application Processing Unit**
  - Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC
- **Real-time Processing Unit**
  - Dual-core Arm Cortex-R5, 32KB/32KB L1 Cache, 256KB TCM w/ECC and 256KB OCM w/ECC

### Foundational Platform
- **NoC Master/NoC Slave Ports**
  - VM1102: 5
  - VM1302: 16
  - VM1402: 16
  - VM1502: 28
  - VM1802: 28
  - VM1902: 16
- **DDR Bus Widths**
  - VM1102: 64
  - VM1302: 128
  - VM1402: 256
  - VM1502: 256
  - VM1802: 288
  - VM1902: 384

### I/O
- **Programmable I/O**
  - VM1102: 316
  - VM1302: 554
  - VM1402: 770
  - VM1502: 500
  - VM1802: 770
  - VM1902: 824
- **Transceiver**
  - VM1102: 12
  - VM1302: 24
  - VM1402: 24
  - VM1502: 44
  - VM1802: 44
  - VM1902: 52

### First Available Device
- VM1102
- VM1302
- VM1402
- VM1502
- VM1802
- VM1902

### Other Features
- **6X Scalable Logic Density**
- **I/O Count Optimized**
- **Transceiver Bandwidth Optimized**
- **Integrated DDR Controllers & Protocol Engines**
Versal Roadmap

2H 2019

AI Core
AI Inference Throughout

Prime
Broadest Application

2020

Premium
112G Serdes
600G Cores

AI Edge
Lowest power AI

2021

AI RF
AI w/ Integrated RF

HBM
Memory Integration
Getting Started

Visit www.xilinx.com/versal
> Check out the Media Kit
> Watch ACAP Intro video
> Subscribe to mailing list for the latest news

View documentation and resources
> Data Sheet Overview
> Product Tables
> Versal Architecture and AI Engine White Papers
Key Take-Aways

**Versal: The First ACAP**
- Heterogeneous Acceleration
- For Any Application
- For Any Developer

**Announcing Two Families**
- Versal Prime Series for Broad Application
- Versal AI Core Series for Highest AI Throughput

**Availability**
- Early Access Program for SW and tools
- Devices Available 2H 2019

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## Versal AI Core Series

### Intelligent Engines

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<td>NoC Master / NoC Slave Ports</td>
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### I/O

- **Scalable DDR 128b – 256b w/ECC**
- **Enabling Ethernet at 10G/25G/50G/100G**
- **256Gb/s PCIe & CCIX Bandwidth to Host**

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## Versal Prime Series

### Intelligent Engines
- **DSP Engines**:
  - VM1102: 472
  - VM1302: 736
  - VM1402: 1,504
  - VM1502: 1,312
  - VM1802: 1,968
  - VM2502: 3,984
  - VM2602: 1,880
  - VM2702: 2,500
  - VM2902: 3,080

### Adaptable Engines
- **System Logic Cells (K)**:
  - VM1102: 352
  - VM1302: 572
  - VM1402: 1,002
  - VM1502: 797
  - VM1802: 1,968
  - VM2502: 2,030
  - VM2602: 1,263
  - VM2702: 1,805
  - VM2902: 2,154

### Total SRAM Capacity (Mb)
- VM1102: 35
- VM1302: 63
- VM1402: 87
- VM1502: 80
- VM1802: 164
- VM2502: 245
- VM2602: 174
- VM2702: 243
- VM2902: 294

### Scalar Engines
- **Application Processing Unit**
  - Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC

### Foundational Platform

### DDR Bus Widths

### DDR Memory Controllers
- VM1102: 1, VM1302: 2, VM1402: 4, VM1502: 2, VM1802: 4, VM2502: 5, VM2602: 6, VM2702: 6

### CCIX & PCIe® w/DMA (CPM)
- VM1102: 1 x Gen4x8, 2 x Gen4x8, VM1302: 2 x Gen4x8, 2 x Gen4x8, VM1402: 4 x Gen4x8, 4 x Gen4x8, VM1502: 1 x Gen4x8, VM1802: 1 x Gen4x8, 2 x Gen4x8

### PCI Express®
- VM1102: 1 x Gen4x8, VM1302: 2 x Gen4x8, VM1402: 2 x Gen4x8, VM1502: 4 x Gen4x8, VM1802: 4 x Gen4x8

### Multirate Ethernet MAC
- VM1102: 1, VM1302: 2, VM1402: 2, VM1502: 4, VM1802: 4

### I/O
- **Programmable I/O (4G, 3.3V)**:
  - VM1102: 216, 100
  - VM1302: 432, 122
  - VM1402: 648, 122
  - VM1502: 378, 122
  - VM1802: 648, 122
  - VM2502: 702, 122
  - VM2602: 702, 100
  - VM2702: 702, 122
  - VM2902: 702, 122

- **Transceiver (32G, 58G)**:
  - VM1102: 12, 0
  - VM1302: 24, 0
  - VM1402: 24, 0
  - VM1502: 44, 0
  - VM1802: 44, 0
  - VM2502: 16, 28
  - VM2602: 20, 32
  - VM2702: 32, 44
  - VM2902: 40, 52

### Key Features
- **6X Scalable Logic Density**
- **Integrated DDR Controllers & Protocol Engines**
- **Transceiver Bandwidth Optimized**
- **I/O Count Optimized**

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## Versal AI Core Series

<table>
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<tr>
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## Adaptable Engines

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## Scalable Engines

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## Versal Prime Series

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<td>Real-Time Processing Unit</td>
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