PERSEUS Plus HEVC
the first single-FPGA real-time 4Kp60 encoder

Presented By

V-NOVA

Name: Fabio Murra and Obioma Okehie
Title: PERSEUS Plus, the first single-FPGA real-time 4Kp60 encoder
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Unique compression technologies to dramatically improve density & video quality to all screens over any network

- Large video team of 60 in London
- Significant patent portfolio (>250 patents granted)
- Already deployed and engaged with major MSO’s
Traditional approaches to video compression

h.264, HEVC, VP9, AV1

Traditionally, standards have been developed within MPEG every 7-10 years to freeze the codec algorithms and deploy it as a hardware block within dedicated encoding / decoding devices and SoCs needed to deal with the high complexity of the algorithm in real time.
PERSEUS Plus: a new approach

- Unique hierarchical image representation is far more efficient than the traditional block-based codecs
- Combining PERSEUS Plus with an existing base codec improves the overall quality and bandwidth requirements
- The approach better utilises the hardware resources available in modern chipsets and FPGAs

Lower res base increases density 4x
PERSEUS Plus: a new approach

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V-Nova becoming a standard:

PERSEUS Pro undergoing standardization as VC-6/ST-2117

PERSEUS Plus in process for “Low Complexity Codec Enhancements”
PERSEUS on Xilinx FPGA: unique benefits

**Unbeatable Density**
- 4x increase in density on FPGA
- 50x denser than the equivalent software-only implementation
- UHDp60 in single FPGA.

**Bandwidth savings**
- Up to 50% more efficient
- Live UHDp60 @8Mbps, 1080p60 @3Mbps
- Increase reach, improve quality of experience, reduce cost

**Codec Agnostic**
- PERSUS Plus is codec agnostic
- Works with h.264, HEVC, VP9 and even AV1 when available
- Maximum compatibility with existing workflow
The ONLY 4Kp60 real-time encoder on single FPGA

4Kp60 on single VU9P

4Kp60 on 4 x VU9P

4Kp60 on 80 x x86 cores

<table>
<thead>
<tr>
<th>V-Nova PERSEUS+ NGC HEVC</th>
<th>NGC HEVC only</th>
<th>x265 Software (very slow preset)</th>
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PERSEUS: from Algorithm to Board
Compression algorithm to Board

- Design spec
- Algorithm
- Fix-Pointing
- RTL Coding
- RTL Verification
- Board Installation
- Synthesis / P&R
- System Verification
- Board Programming
- Host Machine setup
- SDAccel / Vivado
- Questa / Xsim
Going through the implementation options

> **Two options to achieving design implementation**

>> Full hardware flow
   - We have full control of every aspect of the implementation and deployment platforms
   - Tools used for pre-synthesis stages can be flexible
   - Take full responsibility on host / kernel drivers
   - Typically longer design times (Much work involved)

>> SDAccel design flow
   - Static region abstracted out. Hence, only need to care about the core IP
   - Reduces design time
   - Integration with partner IP’s much easier and faster

> **Option we chose**

>> SDAccel *RTL-kernel* design flow
   - OpenCL runtime
   - XMA runtime
SDAccel

- Started from a known good design
- Split design into separate kernels (parallelism)
- Generated RTL kernels (.xo) and microblaze executables (.elf) via Vivado
- Integrate host code and external IP within SDAccel
### FPGA occupancy: 4Kp60 in a single VU9P FPGA

![Diagram of FPGA components]

<table>
<thead>
<tr>
<th>Item</th>
<th>Current LUTs</th>
<th>Memory LUTs</th>
<th>Current DSPs</th>
<th>Current FFs</th>
<th>36kbit BRAMs (RAMB36)</th>
<th>(OR) 18kbit BRAMs (RAMB18)</th>
<th>BRAM (Kbits)</th>
<th>288Kbit UltraRams (RAMB288)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core-IP %</td>
<td>62.94</td>
<td>20.11</td>
<td>45.77</td>
<td>32.91</td>
<td>45.09</td>
<td>19.12</td>
<td>64.22</td>
<td>41.67</td>
</tr>
<tr>
<td>DSA static %</td>
<td>9.36</td>
<td>1.35</td>
<td>0.04</td>
<td>5.56</td>
<td>10.42</td>
<td>0.19</td>
<td>10.60</td>
<td>0.00</td>
</tr>
<tr>
<td>Fitting Percentage (%)</td>
<td>72.3</td>
<td>21.5</td>
<td>45.8</td>
<td>38.5</td>
<td>55.5</td>
<td>19.3</td>
<td>74.8</td>
<td>41.7</td>
</tr>
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Difficulties we faced and how we solved them (2017.4.op)

Close communication with Xilinx SME’s & FAE’s will help resolve most issues in a timely manner.

- Kernel verification (HW-Emu option does not enable backpressure on the memory interfaces)
  - Will require mixed signal simulator license to use external faster simulators for complex systems

- Accessing local memory contents (e.g. ROM values)
  - Create extra HW process to dump contents onto DDR

- Debugging the microblaze code
  - Connecting the microblaze processor to the AXI-MM interface to dump text printouts onto DDR

- Lack of control on allocation of local memory (DDR on FPGA)
  - Address re-routing logic required (for cases where the allocated address is outside the module address range)
Integrating PERSEUS Plus into FFmpeg framework

```
ffmpeg \n-f rawvideo -pix_fmt yuv420p -s:v 1920x1080 -r 30 -an -i 
/home/ffmpeg/VU9P/TestSequences/Kimono1_1920x1080_24.yuv \n-frames 240 -c:v libx264 -preset medium -profile:v high -crf 23 -bf 4 -refs 3 -g 30 -b:v 4000k -maxrate 4000k -bufsize 8000k -f h264 -r 30 -y ./sw_outdir/x264_medium_out0_br4000k.h264
```

Change < 20 characters to get hyper acceleration

```
$ ffmpeg \n-f rawvideo -pix_fmt yuv420p -s:v 1920x1080 -r 30 -an -i 
/home/ffmpeg/VU9P/TestSequences/Kimono1_1920x1080_24.yuv \n-frames 240 -b:v 4000k -g 30 -c:v pplusenc_fpga -y ./hw_outdir/out1_br4000k.h264
```

https://trac.ffmpeg.org/wiki/EncodingForStreamingSites
PERSEUS Plus

Visual Quality Improvement
UHD VQ improvements

4x lift in density coupled with:
- **Video quality** improvement
- **Bandwidth** savings
UHD VQ improvements

PERSEUS Plus HEVC (NGCodec)

HEVC (NGCodec)

RIDE-2160p60-420p @ 6mbps
Improving quality and density of existing deployments

- QSV h.264
- PERSEUS
- 'Watchability' (MS-SSIM) 1080p at 1.0 Mbps - Full HD over 4G

- MS-SSIM 480p at 500 kbps
- X.264
- Perseus

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Quality (higher is better) vs. Frames

- PERSEUS
- Plus h.264
- Native h.264
1. Acceleration for any 3rd party IP
2. Acceleration for Xilinx Video IP
PERSEUS XSA – Available for deployment

PERSEUS Plus
Xilinx VU9P implementation of PERSEUS Plus works with any codec

Benefits
Enhance existing server performance:
• add real-time 4Kp60
• increase ABR density
• Reduce power
• Reduce $ per channel

PERSEUS + any codec
QSV (available now)
x264 (available now)
x265 (available now)
VP9 (roadmap)
AVS2 (pending business case)
AV1 (pending business case)
VVC (pending business case)
PERSEUS XDE – Available soon

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## PERSEUS Plus Xilinx IP Offering

### Codec | Partner | Description | PERSEUS Plus benefits | Availability
---|---|---|---|---
H.264 HDE | Alma | High density encoder | Improve video quality | Feasibility
H.264 HQE | IDT | High quality encoder | | |
HEVC-HDE | NGCodec | High density encoder | | |
HEVC-HQE | NGCodec | High quality encoder | Improve density 4x | SOON
VP9-HQE | NGCodec | High quality encoder | Improve density 4x | Roadmap
Zynq-H.264 | Xilinx | Hardened H.264 core | Improved video quality | Feasibility
Zynq-H.265 | Xilinx | Hardened H.265 core | Improved video quality | Feasibility

### Codec | Partner | Description | PERSEUS Plus benefits | Availability
---|---|---|---|---
x.264 | | Open source software encoder | Improve video quality (from –medium to –very-slow) | NOW
x.265 | | Open source software encoder | Improve video quality (from –fastest to –medium) | NOW
QSV | | Intel hardened core | Improve density 3x | NOW

Under review