Revision Control Methodology

Presented By

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Agenda

- Motivation
- Recommendations for implementing a revision control strategy
  - RTL projects
  - IP projects
  - BD projects
- Future improvements
Importance of Maintaining a Revision Control Strategy

- Reproduce previous results
- Board revisions
- Co-development
- Compliance
- Revenue
Implementing a Revision Control Strategy
Foundations of Vivado

GUI – executes project Tcl

Project Flow
(add_files, import_files, launch_runs)

Non-Project Flow
(read_verilog, read_vhdl, place_design)

Focusing on project based scripted flow
Strategy for Successful Revision Control

- Use scripted flows for revision control
- Keep sources external to the project
- Revision control the source repository
- Generate a script to recreate the project
- Revision control the script
- Test your methodology
Adding Sources to Projects

> Use add_files for all sources
  >> Keeps sources external to the project
  >> Un-check “Copy sources into project”

> Filesets contain all project sources
  >> get_filesets
  >> Four “default” filesets
  >> get_files –of [get_filesets]
RTL Example

./userdir
  ./my_repo/2018.2
  ./workspace

./my_repo/2018.2

bft.vhdl
FifoBuffer.v
async_fifo.v
bft_package.vhdl
core_transform.vhdl
round_1.vhdl
round_2.vhdl
round_3.vhdl
round_4.vhdl
bft_full.xdc
build.tcl

build.tcl

vivado –source ..../my_repo/build.tcl
Creating a Project Script

> Manually create the script
  >> Minimalist
  >> Organized
  >> Risk missing some settings

> Automatically create the script using `write_project_tcl`
  >> Verbose
  >> Complicated
  >> Robust, should not miss any settings

> Scripts must be maintained as projects evolve
Understanding Xilinx IP

Xilinx IP Repository
vivado/<version>/data/ip/xilinx/

xadd_sub_v3_0
component.xml
RTL with parameters
constraints, etc.

xadd_sub_v4_0
component.xml
RTL with parameters
constraints, etc.

Upgrade to v4_0

Workspace

xadd_sub_0.xci
IP ver - v3_0
Params – A:8,B:8,Z:9
unique RTL
Templates, etc.

Source Repo

build.tcl
xadd_sub_0/
  xadd_sub_0.xci
    .ignore

build.tcl
xadd_sub_0/
  xadd_sub_0.xci
  *
Xilinx IP Revision Control Options

<table>
<thead>
<tr>
<th>IP Files to Revision Control</th>
<th>Size</th>
<th>Compile time</th>
<th>Re-customizable¹</th>
<th>Forced to upgrade²</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCI</td>
<td>S</td>
<td>Slow³</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>TCL (write_ip_tcl)</td>
<td>S</td>
<td>Slow³</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Whole IP directory</td>
<td>L</td>
<td>Fast</td>
<td>Y</td>
<td>N / locked</td>
</tr>
<tr>
<td>XCIX</td>
<td>M</td>
<td>Fast</td>
<td>Y</td>
<td>N / locked</td>
</tr>
<tr>
<td>DCP</td>
<td>S</td>
<td>Fast</td>
<td>N</td>
<td>NA</td>
</tr>
</tbody>
</table>

> Two real options
   >> XCI or XCIX

> Recommendation
   >> Start with only the XCI file
   >> On upgrade switch to XCIX for IP with changes that are too disruptive

¹ In the existing version of Vivado that generated the original XCI
² Rebuild project using the existing version of Vivado and open project with latest version
³ With Out-of-context synthesis and IP caching enabled, compile time differences may be negligible
Avoid Using the DCP

- A DCP generated out-of-context (OOC) is unconstrained
- IP are synthesized OOC
- Scoped timing constraints are used during the OOC synthesis run
- Timing constraints are discarded prior to writing the DCP
- Using the XCI or XCIX files ensure a fully constrained design
Managing Custom IP Using Repositories

> Develop IP in a revision controlled working directory
> Package the IP into a custom IP repository
  >> Follow Xilinx IP repository directory structure as a reference
  >> `<vivado_version>/data/ip/<company>/IPname_version`
> Working project directories
  >> Set IP repository path
  >> Add XCI
  >> Add both to the build script
Upgrading Custom IP (using Xilinx IP) Repositories

1. Create new IP directory from previous sources
2. Upgrade project and check in new IP files
3. Re-package all IP into new custom <vivado_version> repository
4. Rebuild project directory from previous sources
5. Update the IP repository
6. Upgrade project and check in new project files to repository

Revision Control

Working Directories

- 2018.1/sources build.tcl
- 2018.2/sources build.tcl
- Custom IP Repository 2018.1/… 2018.2/…
- 2018.1/sources build.tcl
- 2018.2/sources build.tcl

- IP 2018.1
- IP 2018.2
- Project 2018.1
- Project 2018.2
Propagation of Parameters in Block Designs

Xilinx IP Repository
vivado/<version>/data/ip/xilinx/

v_hDMI_tx_ss_0_v2
component.xml
RTL with parameters constraints, etc.

v_hDMI_tx_ss_0_v3
component.xml
RTL with parameters constraints, etc.

Workspace

design_1.bd
IP_ver = _v2
Non-default IP params
XCI name for each instance

Propagate parameters
Identify conflicts
Update XCI / BD

unique RTL for BD/IP, etc.

Source Repo

build.tcl
design_1/
design_1.bd
.ignore

build.tcl
design_1/
design_1.bd
.ip/
  _v_hDMI..._v2/*
  .ignore

Upgrade to V3
## Preserving Block Designs

<table>
<thead>
<tr>
<th>BD file to revision control</th>
<th>Size</th>
<th>Compile time</th>
<th>Preserve Layout</th>
<th>Forced to upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD</td>
<td>S</td>
<td>Slow(^1)</td>
<td>N(^2)</td>
<td>Y(^3)</td>
</tr>
<tr>
<td>TCL (write_bd_tcl)</td>
<td>S</td>
<td>Slow(^1)</td>
<td>Y(^4)</td>
<td>Y</td>
</tr>
<tr>
<td>Whole BD directory</td>
<td>L</td>
<td>Fast</td>
<td>Y</td>
<td>N / locked</td>
</tr>
</tbody>
</table>

> **Recommendation**

- Use `write_bd_tcl` to preserve entire BD including layout
- If you want selective IP upgrade, then move towards BD

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1. With Out-of-context synthesis and IP caching enabled, compile time differences may be negligible
2. Can be preserved by checking the BD/ui directory
3. Not with selective IP upgrade. Generated output products of IP still need to be preserved
4. Use –include_layout flag
Additional Files to Revision Control

> **Other source files**
  - XDC
  - Simulation test benches
  - Sysgen IP
  - HLS IP
  - Pre/post tcl scripts
  - Incremental compile DCPs
  - ELF files

> **Util_1 source set introduced in 2018.1**
  - Files are now managed by the project
  - Included in a project archive
Output Files to Consider for Revision Control

- Simulation scripts for 3rd party simulators (export_simulation)
- Hardware definition files for SDK (export_hardware)
- DSAs for export to SDx (write_dsa)
- Bitstreams (generate_bitstream)
- Hardware debug (.ltx, .lpr, debug dashboards)
- Intermediate run results (runs / checkpoints)
Future Revision Control Improvements

- Auto create .ignore files
- Separate output products from the sources
- Make the BD the one true source for a design
- BD Differences
  - Compare two BD to understand the differences between the designs
Summary

> Vivado provides the frameworks to develop your revision control strategy

> Six general steps
  > Use scripted flows for revision control
  > Keep source files in a repository
  > Revision control the repository
  > Create a Tcl script to recreate the project
  > Revision control the script
  > Test your scripts