RF Solutions with Zynq ® UltraScale+ ™ RFSoC

Presented By

Glenn Steiner
Sr. Manager
Xilinx
The First Programmable RFSoC

✓ Integrated RF-Class Analog Converters and Error Correction Technology

✓ Delivering 50-75% Power & Footprint Reduction

✓ Full Programmability Across the RF Signal Chain
Zynq UltraScale+ RFSoC
Introduction
Part of a Complete System Based on Production-Proven MPSoCs

**Monolithically Integrated**

**Hardened Engines**
- PCIe Gen3
- 100G Cores

**33G Transceivers**
- 33Gb/s
- 28G Backplane Capable

**Processing System**
- Quad-Core A53 (64-bit)
- Dual-Core R5 (32-bit)

**Programmable Logic**
- 16nm FinFET
- UltraScale+ FPGA Fabric

**DSP-Intensive**
- 4,272 DSP slices
- 7,612 GMACs

**Analog-to-Digital Converters**
- Up to 4.096 GSPS

**Digital-to-Analog Converters**
- Up to 6.544 GSPS

**Soft Decision Forward Error Correction**
- LDPC & Turbo Support
Xilinx RF Converters – An Evolution and A Revolution

Full Spectrum Bandwidth = 4GHz
DAC = 6.55GSPS, ADC = 4.096GSPS

10-bit, 200-kSPS

DAC: 6Gsp
ADC: 2/4Gsps

16nm Test Chip

56G High Speed PAM4 Serial Transceivers
Zynq UltraScale + RFSoC Applications
Software Defined Radio on a Chip

Zynq US+ RFSoC

Processing System
Quad ARM Cortex-A53
Dual ARM Cortex-R5

Programmable Logic
680K – 930K System Logic Cells
3168 – 4272 DSP Slices

Digital Baseband

CPRI, 10GE, 25GE, ..
..1001001010111010101...
..1001001010111010101...

GTY
28Gb/s

SD FEC

RF in
0 – 4GHz

RF out
0 – 4GHz

RF I/O
(multi-standard, multi-band)

LNA

AAF

BPF

PA

DDC

RF DAC

DUC

RF ADC

RF ADC

RF DAC

RF ADC

SD FEC

GTY

28Gb/s

Programmable Logic
680K – 930K System Logic Cells
3168 – 4272 DSP Slices

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Enabling 5G Architectures

Zynq UltraScale+ RFSoC - Advancing 5G Architectures

- **Spectral Efficiency**
- **Power Efficiency**
- **Network Densification**

**Zynq UltraScale+ RFSoC**
- Remote Radio for Massive-MIMO
- **Power** • **Form Factor**
- Digital Beamforming
- CPRI / eCPRI
- Fronthaul

**Zynq UltraScale+ RFSoC**
- Wireless Backhaul
- **Throughput** • **Power** • **Form Factor**
- Ethernet
- Point-to-Point Reach, Reliability, Throughput

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Zynq UltraScale+ RFSoC in 5G New Radio

- Digital Beamforming (Digital & RF Domain) Single Processor Control
- Up to 16x16 RF Integration
- Processing System
  - CPU0: Beamforming Control
  - CPU1: RF Calibration
  - CPU2: DPD SW
  - CPU3: Operation & Maintenance
  - DPD HW
  - CFR
  - DUC
  - DDC
  - Partial L1 Beamforming Transform (iFFT/FFT)
- SDN Control
- System Monitoring Configuration
- IP for Offloading L1 Closer to Radio Reduces Fronthaul Throughput

Air Interface

- DAC
- ADC

Digital Beamforming

- Up To 25Gb/s
- To Baseband

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Zynq UltraScale+ RFSoC in Wireless Backhaul

- Multi-Level LDPC (Optionally bypass SD-FEC)
- ARM Processing System
- Up to 4x4 RF Integration

Air Interface

Point-to-Point Communication

33G Transceivers

To/From Baseband

L2 Processing

SD-FEC

Log Likelihood Ratio

Mod/Demod

Digital Front-End

DAC

ADC

Multi-Level LDPC (Bypass SD-FEC)
DOCSIS 3.1 Remote PHY Node

Distributed Access Architecture

- “Fiber Deep” deployed closer to the home for greater bandwidth & power efficiency
- Remote PHY node moves PHY layer processing closer to the home, increasing network capacity
DOCSIS 3.1 Remote PHY Node

- **ZYNQ RFSoC**
- **Processing System**
  - Traffic Management
  - GCP
- **LDPC for DOCSIS 3.1**
- **Validated DOCSIS 3.1 OFDM IP**
- **DPD IP**
- **RF Integration**
  - For Power and Footprint
- **To/From Headend Office**
  - Optical Fiber
- **To/From Cable Modems**
  - Coaxial Cable (Full Duplex)

- **MAC Packet Processing (MACSEC)**
- **D-UEPI IP**
- **U-DEPI IP**
- **DOCSIS3.0 SCQAM**
- **Downstream LDPC**
- **Upstream LDPC**
- **DOCSIS 3.1 OFDM**
- **DOCSIS 3.1 OFDMA**
- **DOCSIS3.0 A-TDMA**
- **DUC**
- **DPD**
- **DAC**
- **ADC**
- **Managed by A53**

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Zynq UltraScale+ RFSoC Product Family and Benefits
## Zynq UltraScale+ RFSoC Family Overview

<table>
<thead>
<tr>
<th>RF Data Converters &amp; Soft Decision FEC</th>
<th>ZU21DR</th>
<th>ZU25DR</th>
<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>12-bit, 4GSPS ADC</td>
<td>–</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>–</td>
</tr>
<tr>
<td>12-bit, 2GSPS ADC</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>16</td>
</tr>
<tr>
<td>14-bit, 6.4GSPS DAC</td>
<td>–</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>SD-FEC</td>
<td>8</td>
<td>–</td>
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<td>8</td>
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</tbody>
</table>

### Processing System & Programmable Logic

<table>
<thead>
<tr>
<th></th>
<th>ZU21DR</th>
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<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application Processor Core</td>
<td>Quad-core ARM Cortex-A53 MPCore up to 1.5GHz</td>
<td></td>
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</tr>
<tr>
<td>Real-Time Processor Core</td>
<td>Dual-core ARM Cortex-R5 MPCore up to 533MHz</td>
<td></td>
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</tr>
<tr>
<td>High Speed Connectivity</td>
<td>DDR4-2600, PCIe Gen3 x16, 100G Ethernet</td>
<td></td>
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</tr>
<tr>
<td>Logic Density (System Logic Cells)</td>
<td>930K</td>
<td>678K</td>
<td>930K</td>
<td>930K</td>
<td>930K</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>4,272</td>
<td>3,145</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
</tr>
<tr>
<td>33G Transceivers</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>
Key Benefits of Integrated RF Data Converters

**Fully Programmable Direct RF Sampling Radio Platform**
- RF-signal processing moved to the digital domain for a fully Programmable Solution
- Software Defined Solution for multi-mode and multi-band radios

**Reduced System Power**
- Reduces data converter power by using advanced technology and Digitally Assisted Analog
- Elimination of power hungry FPGA-to-Analog interfaces like JESD204

**Dramatic System Footprint Reduction**
- Eliminates discrete converters and associated JESD PCB area
- Enables increasing channel counts across a range of new radio applications

**Shorter Design Cycle**
- Simplified HW design with fewer RF components and the elimination of JESD Interfaces
- Simpler Data Converter Subsystem configuration from within Xilinx Vivado tools
Programmable Direct RF Sampling For Radio

> Moving RF Signal Processing into the Digital Domain
  >> Flexible Platform based on Programmable HW and SW addresses a range of radio applications

> Remove less flexible RF signal processing components
  >> Analog/RF components have limited flexibility and performance

> Enable a programmable platform that can be used across radio types
  >> Multiple radio variants required to address global frequency allocations and different bandwidths
  >> Ability to support new and emerging standards such as Carrier Aggregation
Baseband/IF Sampling & RF Signal Processing

- **FPGA / DFE**
- **CPRI 10GE**
- **Baseband Interface**

**RFIC**
- **3.5GHz RF Signal**
- **Analog Frequency Shifting and Filtering**

**DAC**
- **LPF**
- **Q**
- **I**

**ADC**
- **LPF**
- **Q**
- **I**

**LO**
- **BPF**
- **Duplex Filter**
- **Receiver**

**Calibration & Control**

**JESD**
- **SPI**
- **Calibration & Control**
- **Baseband Interface**
Direct RF Sampling & Digital Signal Processing

- **RF-DAC**
- **RF-ADC**
- **LNA**
- **BPF**
- **PLL**
- **Ref Clock 245.76MHz**
- **3.5GHz RF Signal**

**Digital Frequency Shifting and Filtering**

- **ZYNQ RFSoC**
- **FPGA / DFE**
- **CPRI**
- **10GE**
- **Baseband Interface**
- **Band Select**
- **3.5GHz**
- **4.9152GHz**
- **3.93216GHz**

**Digital Baseband Interface**

- **3.5GHz DUC**
- **3.5GHz DDC**
- **3.5GHz PLL**
- **Reference Clock 4.9152GHz**
- **Reference Clock 245.76MHz**

**Receiver**

- **Duplex Filter**

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Discrete Direct RF Sampling Solution Case Study
8T8R 200MHz Band 42 Radio

Quad ARM Cortex-A53
Dual ARM Cortex-R5

Processing System

16 lanes of JESD interfacing required to interface to discrete RF ADCs & DACs

4W of power used to implement FPGA JESD Interface

ZYNQ MPSoC

Programmable Logic

Serial Transceivers

Transceivers 12.5Gb/s

Transceivers 12.5Gb/s

Transceivers 12.5Gb/s

Transceivers 12.5Gb/s

JESD IP

Discrete RF DC + JESD IP:
Total Power = 30W
Total Area = 2125 mm²

4W

CPRI 10/40/100 GE

Quad packaged external RF Data Converters

8 Tx Channels

2 x 15mm x 15mm

8 Rx Channels

2 x 15mm x 15mm

JESD

RF DAC

RF DAC

RF DAC

RF DAC

DUC

RF DAC

RF DAC

DUC

JESD

JESD

Significant footprint and Power of External Data Converters

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Integrated Direct RF Sampling Case Study
8T8R 200MHz Band 42 Radio

4W JESD interface is replaced with a 9W 8T8R RF Sampling Data Converter Subsystem

Eliminate the power and PCB area of 16 JESD lanes

Eliminate ~ 26W of discrete RF Data Converter Power and PCB area

Integrated ZU+ RFSoC:
Total Power = 9W (70% savings)
Total Area = 1225 mm² (42% savings)

Power consumption of Data Converters implemented on 16nm FinFET is greatly reduced by using the latest digitally assisted analog techniques

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Advantages of an Integrated SD-FEC

High Throughput and Compute Bandwidth
- High performance core with robust LPDC and Turbo engines
- Configurable interface to control throughput per design requirements

Flexible Customization and Design Integration
- Dynamically optimize parameters and codes for evolving standards
- Coupled with an HW & SW platform

Reduced System Power
- Hardened 16nm FinFET silicon vs. soft implementation in FPGA fabric
- Meets thermal requirements for key applications
Dramatic Power Reduction vs. Soft Core
Example of 2x LDPC Cores at 2Gb/s Throughput

LDPC FEC Soft Cores
~1M System Logic Cells (425K LUTs)

- 33% Logic of Device

- LDPC #1
- Processing System

- LDPC #2

~6.4W of Dynamic Power

- 307MHz $F_{\text{MAX}}$
- 150k LUTs
- 258 BRAM Kbits for storage & buffering

80% Power Reduction

Integrated SD-FEC
(ZU21DR RFSoC)

- 614MHz $F_{\text{MAX}}$
- No additional resources required
- More flexibility & functionality available vs. soft core

~1.2W of Dynamic Power
Zynq® UltraScale+™ RFSoC
RF ADC & RF DAC Overview
RF ADC Block 2GS/s Configuration (ZU29DR Only)

m03_axis (Real or I/Q)
m02_axis (Real or I/Q)
m01_axis (Real or I/Q)
m00_axis (Real or I/Q)

AXI Stream Data Buses Up to 8 x 16-bit words
AXI Lite (PS Control)

Control & Status

DDC

ADC 3
2GS/s 12-bits

ADC 2
2GS/s 12-bits

ADC 1
2GS/s 12-bits

ADC 0
2GS/s 12-bits

Sampling Clock
PLL

2.49KΩ

VCM01

VCM23

100Ω

100Ω

100Ω

100Ω

100Ω

245MHz – 4GHz

m03_axis (Real or I/Q)
m02_axis (Real or I/Q)
m01_axis (Real or I/Q)
m00_axis (Real or I/Q)

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RF ADC Block 4GS/s Configuration (ZU25DR, ZU27DR, & ZU28DR Only)

AXI Stream Data Buses
Up to 8 x 16-bit words

m03_axis (Q)
m02_axis (I)

AXI Lite
(PS Control)

m01_axis (Q)
m00_axis (I)

Control & Status

IP Core

DDC

ADC 23
4GS/s 12-bits

ADC 01
4GS/s 12-bits

Sampling Clock

PLL

VIN23_P
VIN23_N

ADC_CLK_P
ADC_CLK_N

ADC_REXIT

SYSREF_P
SYSREF_N

VIN01_P
VIN01_N

VCM23

100Ω

100Ω

100Ω

100Ω

100Ω

100Ω

(245MHz – 4GHz)

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RF DAC Block Diagram
(ZU25DR, ZU27DR, ZU28DR, & ZU29DR)

AXI Stream Data Buses
Up to 16 x 16-bit words

m03_axis (Real or I/Q)
m02_axis (Real or I/Q)

AXI Lite
(PS Control)

m01_axis (Real or I/Q)
m00_axis (Real or I/Q)
Zynq UltraScale+ RFSoC Product Solutions
Zynq UltraScale+ RFSoC Kits

> Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit
  >> XCZU28DR-2FFVG1517E RFSoC
    - 8x 4GSPS 12-bit ADCs
    - 8x 6.5GSPS 14-bit DAC
    - 8 soft-decision forward error correction (SD-FECs)
  >> FMC+ :12 x 32.75 Gb/s GTY transceivers and 34 user defined differential I/O signals
  >> XM500 RFMC balun transformer card w 4 DACs/ 4 ADCs to baluns 4 DACs/ 4 ADCs to SMAs
  >> Price: $8,995
  >> Part Number: EK-U1-ZCU111-G

> Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit
  >> XCZU29DR RFSoC
    - 16x 2GSPS 12-bit ADCs
    - 16x 6.5GSPS 14-bit DAC
  >> Balun Board, Bullseye Cables, Filters
  >> Price: $14,995
  >> Part Number: CK-U1-ZCU1275-G
RF DC Evaluation Tool Highlights (ZCU111)

> LabVIEW based evaluation GUI running on PC
  ▪ Ethernet Interface to board

> Loopback (DAC to ADC) for multiple channels evaluation
  ▪ Key parameters measurement (i.e. NSD, SFDR, THD, Harmonics, Spurious Performance)
  ▪ 2 tones test (i.e. IM3)

> DAC / ADC standalone evaluation
  ▪ DAC analysis => generate test vectors
  ▪ ADC analysis => FFT spectrum analysis for various input test signals with signal generator

> Advance Features
  ▪ Nyquist zone, DDC/DUC, Mixer, NCO, Looping feature
  ▪ File input / export for customized test vectors / modulation
RF Analyzer Debug Tool Highlights

> **Act as a debug tool**
  - Support the ZU+ RFSoC configuration
  - Cross-check features and functionalities
  - Ease of use – no FPGA experience required
  - Not require any additional external resources (i.e. DDR)

> **Compatible with any platforms**
  - ZU+ RFSoC performance can be evaluated in any customers’ boards

> **JTAG based communication interface**
  - JTAG USB cables connected between debug tool & customers’ platforms
  - All communications via JTAG:
    - CTRL: JTAG-to-UART
    - DATA: JTAG-to-AXI

> **Features**
  - Simplified version of RF DC Evaluation Tool
ZCU111 Power Measurement & Power Advantage Tool

- Tool Measures & Displays All Rails, SysMon Voltages & Temperature
  - Including ZU+ RFSoC Converter Power
- Text, Plots, & Data Logging Included
- Currently supported on ZCU102, ZCU106 and NOW ZCU111
- Works with Customer Designs Without Impact
  - Less temperature unless R5 code included
- Separate GUI Enables More to Be Seen
Documentation

> PG269 – RF-ADC/DAC Product Guide
  >> driver/API – Appendix C
  >> HTML driver docs in XSDK build
     (system.mss file Documentation link, GitHub)
  >> Xilinx linux/baremetal wikis

> PG256 – SD-FEC Product Guide
  >> bare-metal driver/API – Appendix C
  >> Linux driver/API from source files via Doxygen
  >> HTML driver docs in XSDK build
     (system.mss file Documentation link, GitHub)
  >> Xilinx linux wiki

Also very helpful to new ZU+ users:
  >> UG1209 – ZU+ MPSoC Embedded Design Tutorial
  >> UG1228 – ZU+ Embedded Design Methodology Guide
  >> UG1087 – ZU+ MPSoC Register Reference Guide
Zynq® UltraScale+™ RFSoC
Hardware & Software Design Flow
Zynq UltraScale+ RFSoC Design Flow Overview

Xilinx tools support the configuration and integration of the complete RF Data Converter Subsystem.

Up to 6 TMACs of customizable DSP

Complete Solution

Tool Suite

VIVADO

HLx Editions

SDx

Environments

System Generator

SDK

IP Integrator

IP Portfolio

Complete Solution

DSP

SSR IP

DPD

DOCSIS 3.x

DOCSIS FDx*

Evaluation Platforms

ZCU111

ZC1275

Custom DSP

Processing System
Quad ARM Cortex-A53
Dual ARM Cortex-R5

Control & Configuration

RF DAC

RF ADC

AXI Lite

AXI Stream

DUC

8 – 16 Tx Channels

8 – 16 Rx Channels

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Super Sample Rate Support & IP

> Super Sample Rate – Processing multiple samples per clock
  >> Data into FPGA @ much higher sample rate than the FPGA clock
    – Sample rate into FPGA greater than PL clock rate
  >> Need to parallelize the input and process multiple samples per FPGA clock cycle
  >> Requested by A&D customers where RF-ADC/DACs do not meet there DUC/DDCs needs

> SysGen has developed an SSR programmatical library of 26 SSR IP blocks
  >> Including FIR, Complex Mult, Mult, DDS and others (2018.3)
  >> SysGen provides additional Super Rate Support
RF-ADC/DAC Implementation Steps

1. Add an RF-ADC/DAC instance using IPI
   • Single instance

2. Use GUI to configure and customize the IP
   • Right click IP to generate example design and testbench, plus DAC HW stimulus generator and ADC HW sink
   • Use BSPs for HW examples per board

3. Connect the RF-ADC/DAC instance to the PS, additional logic, RTL, outside world…

4. Implement (Synthesis, PnR…)

5. Generate the bitstream, export the HDF

6. Implement your Software Project
   • XSDK, Petalinux, 3rd party…
SD-FEC Implementation Steps

1. Add SD-FEC instance using IPI
   - SD-FEC requires a license – but it’s free xilinx.com/products/intellectual-property/sd-fec.html
   - Place SD-FEC IP instances (see PG256 for placement constraints)

2. Use GUI to configure and customize the IP
   - Includes Optional Example Designs
     1) Testbench simulation
     2) PS-based example design

3. Connect SD-FEC instances to the PS, additional logic IP, RTL, outside world…

4. Implement (Synthesis, PnR…)

5. Generate the bitstream, export the HDF

6. Implement your Software Project
   - XSDK, Petalinux, 3rd party…
Drivers & Software
The Processing System is identical to a ZU+ MPSoC, except:

- No GPU,
- Quad Cortex-A53 APU only (no dual)
- All other PS blocks remain the same

A portion of the PL of a ZU+ MPSoC device has been replaced with the SD-FEC, RF-ADC/DAC blocks

No change to peripheral interfaces or drivers (I2C, QSPI...)

- Software users coming from a ZU+ design already know how to use the RFSoC PS
Zynq UltraScale+ RFSoC Drivers

> **RF-ADC/DAC – rfdc_v* (3.2) (PG269 – Appendix C)**
  >> Bare-Metal – XSDK build, GitHub, Linux – GitHub (embeddedsw)
  >> Linux and bare-metal APIs are identical
  >> Control plane manipulation, avoiding registers
  >> 77 APIs total (as of 2018.1)

<table>
<thead>
<tr>
<th>Driver</th>
<th>Type</th>
<th>Uses Libmetal?</th>
</tr>
</thead>
<tbody>
<tr>
<td>rfdc</td>
<td>Bare-metal</td>
<td>Yes</td>
</tr>
<tr>
<td>rfdc</td>
<td>Linux</td>
<td>Yes</td>
</tr>
<tr>
<td>sd_fec</td>
<td>Bare-metal</td>
<td>No</td>
</tr>
<tr>
<td>sd_fec</td>
<td>Linux</td>
<td>Yes</td>
</tr>
</tbody>
</table>

> **SD-FEC – sd_fec_v* (1.0) (PG256 – Appendix C)**
  >> Bare-Metal – In the XSDK build, GitHub
     Linux – GitHub (linux-xlnx) – linked from Xilinx linux drivers wiki
  >> Linux and bare-metal APIs differ
  >> Control plane manipulation, data table updates, register manipulation option via API
  >> 7 main bare-metal APIs, plus 84 specialized register/table API calls (as of 2018.1)

> Three of the four driver combinations use libmetal library

.../Xilinx/embeddedsw/XilinxProcessorIPLib/drivers
A Simple RF-ADC/DAC Example Explained

> Set the RF-ADC/DAC instance
> Populate the data structures per the initial Vivado settings
> Two nested loops checking which blocks are enabled
  >> The first runs through each Tile
  >> The second runs through each Block within each Tile
> Modify Mixer Settings from initial configuration
> Write new Mixer Settings
> Modify QMC Settings from initial configuration
> Write new QMC Settings

Software changes can have drastic effects on the hardware (example: setting the wrong data rate will generate a FIFO overflow)
A Simplified Linux Zynq UltraScale+ RFSoC Boot Example

**Time**

- **Power Up**
- **Power and Anti-Tamper Monitoring**
- **FSBL**
- **uboot**
- **Linux**
- **Application(s) Running**
- **PMU/CSU**
- **APU/RPU**
- **Load bitstream**
- **Start SD-FEC and/or ADC/DAC**
- **RF Operation**
- **ZU+ RFSoC**

<table>
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<tr>
<th>Processing System</th>
<th>Programmable Logic</th>
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- The PMU/CSU initialize as in a ZU+
- The FSBL (First Stage Boot Loader) loads the bitstream including the SD-FEC and/or RF-ADC/DAC blocks
- In parallel the PMU/CSU/APU/RPU finish initialization and the SD-FEC and/or RF-ADC/DAC blocks initialize via on-board state machines *(no user interaction)*
- Software access to the IP is **optionally** started through *_Lookup* then *_CfgInitialize* API commands
- Application code can then **optionally** interact with the SD-FECs or RF-ADC/DAC as needed through APIs

- **The RF-ADC/DAC initialize and can operate without software interaction**
See The RF Evaluation Tool Demonstration During The Break
RF Data Converter Evaluation Tool - Overview

On-Chip Mem. 
Tx I/Q vectors 

RF DAC

On-Chip Mem. 
Rx I/Q vectors 

RF ADC

USB to UART

Gigabit Ethernet

NI Labview GUI

ADC Results & Analysis 
and 
DAC stimuli building

DAC Results & Analysis (optional)

LPF path

HPF path

Tx

Rx
Beta RF DC Evaluation Tool Measurement simple set-up

- DAC outputs to Spectrum Analyzer (optional)
- DAC channel output to Spectrum Analyzer
- USB / Ethernet cable connected to PC
- DAC to ADC loopback with BPF in between
- DAC to ADC loopback FFT results on TRD
- DAC outputs to Spectrum Analyzer (optional)
- Spectrum Analyzer (optional)
Summary

- Integrated RF Data Converter Subsystem addresses a wide range of applications
- Significantly reduces the Power and Footprint of high channel count systems
- Enables adaptable Radio HW platforms
- Full support in Vivado accelerates development time versus discrete solutions
- Data Converter Evaluation Board, Design, and Evaluation Tools
Adaptable.
Intelligent.
RF Solutions with Zynq® UltraScale+™ RFSoC