State of FPGA-based Acceleration

Presented By

Vinay Singh
Sr. Director, Software Solutions and Platform Marketing

October 2, 2018
FPGA-Based Acceleration Momentum

Accelerated Applications

250+ Companies
Developing Applications

Developers

10x More Developers
Onboarded since 2017

Acceleration Platforms

4 Cloud
2 On-premise

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Develop & Deploy Applications From Cloud to On-Premise

SDAccel Environment

aws
F1 Instance VU9P
Sep. 2017

F1 Instance VU9P
Nov. 2017

FP1 Instance VU9P
June 2018

F3 Instance VU9P
Sep. 2018

New instance F1.4xlarge
Sep. 2018

Alveo U200, U250
Oct. 2, 2018

Alveo U200, U250
Oct. 2, 2018

General Availability

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Announcing EC2 F1 New Capabilities

- New instance size: f1.4xlarge provides a significant performance boost compared to f1.2xlarge

- Virtual Ethernet: enabling high-performance networking acceleration use-cases like firewalls, routers, filtering and more

- DRAM data retention: boosting FPGA images pipeline runtime execution

- New FPGA developer AMI supporting Vivado 2018.2 for faster compile times, higher frequencies and improved timing closure

> Visit AWS Developer Hangout zone to learn more!
## Acceleration Ecosystem

<table>
<thead>
<tr>
<th></th>
<th>Developers</th>
<th>Partners</th>
<th>Apps</th>
</tr>
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<tr>
<td></td>
<td>115</td>
<td>43</td>
<td>15</td>
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<tr>
<td>2017</td>
<td>1127</td>
<td>268</td>
<td>35</td>
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<td>2018</td>
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<tr>
<td>Developers Trained Companies + Academia</td>
<td>Accelerator Program (Approved Partner)</td>
<td>Published Apps</td>
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Getting Developers Onboarded

In-person

Co-located at strategic events
SC17, FPGA2018, XDF, CVPR, ...

Virtual on-demand

Amazon EC2 F1 SDAccel Developer Lab

Work through this self-paced tutorial where you will receive an overview of AWS F1 and SDAccel® with step-by-step instructions on using Amazon EC2 F1 instances to accelerate your applications. In this virtual developer lab, you will connect to an F1 instance, experience F1 acceleration, and develop and optimize F1 applications with SDAccel.

https://www.xilinx.com/products/design-tools/cloud-based-acceleration.html#sdaccellab

Developers Trained
Companies + Academia

2017 115
2018 1127

University Courses

Prof. Zhiru Zhang, Cornell
High-level Digital Design Automation Labs and project offered on AWS F1, Fall 2018

Prof. Jason Cong, UCLA
Customizable Computing for Big Applications, Fall 2018
Parallel and Distributed Computing, Winter 2019

Prof. Krste Asanovic, UC Berkeley
CS152 Computer Architecture and Engineering, Spring 2018

eLearning & Instructor-Led Courses

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Acceleration In Education

Xilinx University Program

Accelerate Your Research on the AWS Cloud with Xilinx FPGAs

- Scalable infrastructure
- No tools or license setup
- Integrate with over 100+ AWS services
- Get started with AWS EC2 F1 instances

PROFESSORS
University Teaching and Research
- Get the latest Xilinx technology
- Attend a professor workshop
- Access teaching material
- XUP Professor Area...

STUDENTS
Class Room and Projects
- Download free FPGA design tools
- Purchase your own board
- Access technical resources
- XUP Students Area...

www.xilinx.com/xup

Open Hardware design competition EMEA 2018
AWS F1 Category Winner and Finalists

5 Points to Rule Them All
Winner: AWS EC2 F1 prize

AWS EC2 F1: circFA
Implementation
Optimize the algorithm for the FPGA, preserving precision accuracy and adaptability of the software version

AWS EC2 F1: FastBrain

Politecnico di Milano
Emanuele Del Sozzo, Marco Rebozzi, Lorenzo Di Tucci (Prof. Marco D. Santambrogio)
Project Link

Politecnico di Milano
Peverelli Francesca, Zena Alberto, Cabri Enrico (Prof. Marco Santambrogio)
Project Link

Politecnico di Milano
Filippo Carloni, Giada Casagrande, Valentina Corbetta (Prof. Marco Santambrogio)

Acceleration Posters @ XDF

FireSim: Productive, Scalable, FPGA-Accelerated Cycle-Accurate Hardware Simulation using Cloud FPGAs
Sagar Farahbakhch, Hayo Meus, Dongmin Kim, David Bevan, Alex Bauer, Benaeddine Abboushi, Tadej Bakic, Jonathan Force, David Atienza, Yaron Averbuch
Post of Electrical Engineering and Computer Science, University of Virginia, sfarahbakhch@virginia.edu

Automata Processing on FPGAs
Chunfu Bu, Yinhe Dong, Ted Xie, Jack Wadden, Mirco Stan, Kevin Shadron
Department of Computer Science, University of Virginia, chunfu@virginia.edu

DEMOCRATIZE ACCELERATED GENOMIC PIPELINES ON FPGA
Lorenzo Di Tucci, Giulia Guidi, Marco Rebozzi, Sara Notargiacomo, Marco D. Santambrogio
Dipartimento di Informatica, Informazione e Comunicazioni, Politecnico di Milano (Italy), lorenzo.ditucci@polimi.it

Galapagos: A Full Stack Approach to FPGA Integration in the Cloud
Nafi Tarafdar, Nariman Eskandari, Paul Chow
Electrical and Computer Engineering, University of Toronto, ntarafdar@gmail.com

FPGAACCELERATED BASEBAND FOR WIRELESS SYSTEMS
Chunhua Tan, Kuizeng Li, Joseph Cavallaro
Department of Electrical and Computer Engineering, Rensselaer Polytechnic Institute, johncav@rpi.edu

RICE
Rosetta: A Realistic HLS Benchmark Suite for FPGAs
Students: Yiyun Zhou, Ritchie Zhao, Hanchun Jin
Faculty Advisor: Zhiwu Zheng
School of Electrical and Computer Engineering, Cornell University

Accelerator Startups from Academia

www.inaccel.com
xelera.io/

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Enable companies to accelerate products/services on the cloud and on-premise

- Leverage your Existing algorithms and IP
- Deploy Custom Hardware to Millions in Public Cloud
- Extend your existing business model
- Discounted XBB cards for development
- Connect to Xilinx marketing, FPGA expertise and funding opportunities

www.xilinx.com/accelerator-program
## Accelerated Applications

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<tr>
<th>Compression</th>
<th>Data Analytics</th>
<th>Published Apps</th>
<th>Financial Computing</th>
<th>Genomics</th>
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<tr>
<td>CAST</td>
<td>BLACKLYNX</td>
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<td>MAXELER</td>
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<td>XILINX</td>
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<td>SUMUP ANALYTICS</td>
<td>alcon COMPUTING</td>
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<td>LegUp</td>
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<td>POLITECNICO DI TORINO</td>
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<td>BigZetta Systems</td>
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<th>Image Processing</th>
<th>Machine Learning</th>
<th>Security</th>
<th>Video</th>
<th>Tool</th>
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<td>XILINX Accelerated Computing</td>
<td>DEEPHI XILINX</td>
<td>ZOTech mle inaccel</td>
<td>NGCODEC PATHPARTNER</td>
<td>XILINX PLUNIFY FireSim Reconfigure.io</td>
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<td>CTACCEL</td>
<td>mle</td>
<td>Titan</td>
<td>skreens</td>
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[https://www.xilinx.com/products/design-tools/acceleration-zone.html#libraries](https://www.xilinx.com/products/design-tools/acceleration-zone.html#libraries)
Xilinx ML Suite - Fastest Real Time Inference

Your Application

RESTful API, python

TensorFlow, mxnet, Caffe

xfdNN Compiler • Auto-quantizer ML Software Libraries

XILINX

GPU

CPU

Googlenet v1

Img/s

0 1000 2000 3000 4000

4x

20x

* See White Paper for performance details

Alveo

U200, U250

https://www.xilinx.com/ml

https://github.com/xilinx/ml-suite
Xilinx ABR Video - Real Time Video Streaming

High performance HEVC and VP9 Encoder

Fully configured transcoding pipeline

Easy programming interface with FFmpeg

60 fps for real-time video streaming

7x greater than x265 slow

10x greater than Libvpx
<table>
<thead>
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<th><strong>Acceleration Resources</strong></th>
<th><strong>Developers</strong></th>
<th><strong>Data Scientists, ML Practitioners</strong></th>
<th><strong>Academics</strong></th>
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<td>AWS F1 SDAccel Developer Lab</td>
<td>AWS F1 ML Suite Developer Lab (coming soon)</td>
<td>Sign-up for: AWS Educate, Xilinx University Program</td>
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<tr>
<td><strong>Start-ups, IP Providers</strong></td>
<td>Sign-up for: Xilinx Accelerator Program</td>
<td>Cloud End Users</td>
<td>On-premise End Users</td>
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<td>AWS F1 Apps and Libraries</td>
<td>Xilinx Alveo Accelerator Cards</td>
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Accelerated Apps

Developers

Acceleration Platforms

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