



State of FPGA-based Acceleration

Presented By

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Sr. Director, Software Solutions and Platform Marketing

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FPGA-Based Acceleration Momentum

Accelerated
Applications

**250+ Companies
Developing Applications**

Developers

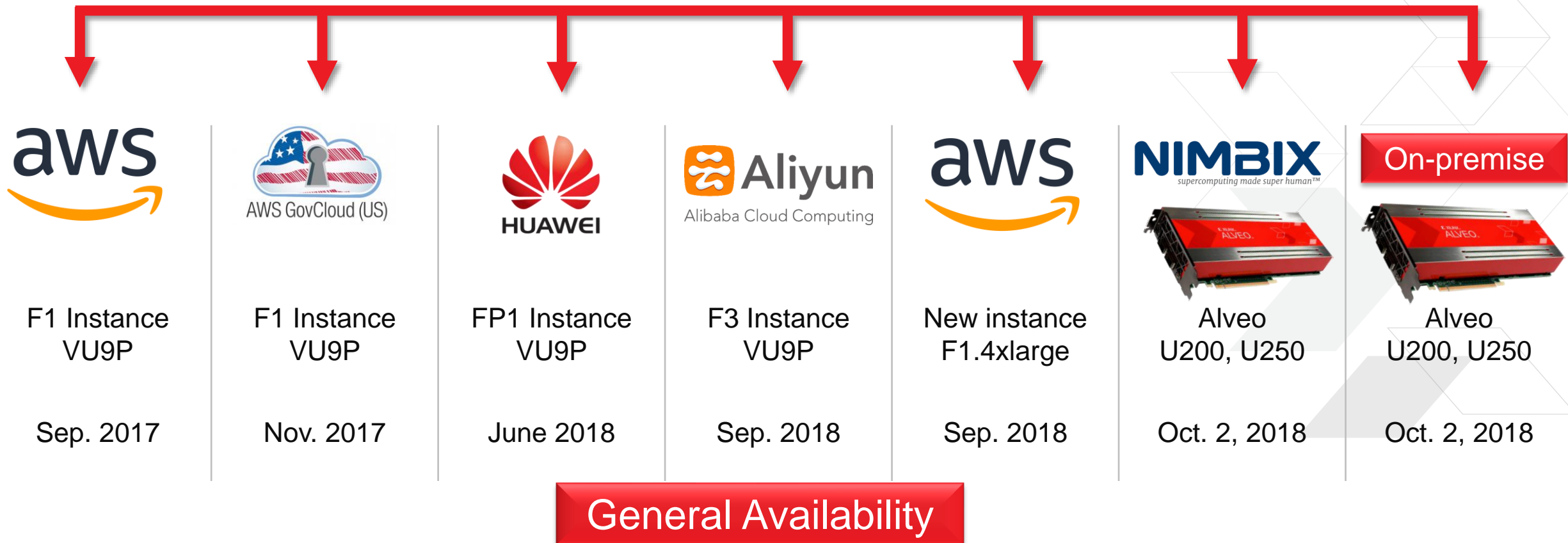
**10x More Developers
Onboarded since 2017**

Acceleration
Platforms

**4 Cloud
2 On-premise**

Develop & Deploy Applications From Cloud to On-Premise

SDAccel[™]
Environment



Announcing EC2 F1 New Capabilities

- New instance size: f1.4xlarge provides a significant performance boost compared to f1.2xlarge
 - Virtual Ethernet: enabling high-performance networking acceleration use-cases like firewalls, routers, filtering and more
 - DRAM data retention: boosting FPGA images pipeline runtime execution
 - New FPGA developer AMI supporting Vivado 2018.2 for faster compile times, higher frequencies and improved timing closure
- > → Visit AWS Developer Hangout zone to learn more!



3 FPGA instance types



F1 Virtual Ethernet



DRAM Data Retention

Acceleration Ecosystem

Developers

115 **1127**

2017

2018

Developers Trained
Companies + Academia

Partners

43 **268**

2017

2018

Accelerator Program
(Approved Partner)

Apps

15 **35**

2017

2018

Published Apps

Getting Developers Onboarded

In-person



Co-located at strategic events
SC17, FPGA2018, XDF, CVPR, ...

Virtual on-demand

Amazon EC2 F1 SDAccel Developer Lab

Work through this self-paced tutorial where you will receive an overview of AWS F1 and SDAccel™ with step-by-step instructions on using Amazon EC2 F1 instances to accelerate your applications. In this virtual developer lab, you will connect to an F1 instance, experience F1 acceleration, and develop and optimize F1 applications with SDAccel.



Get Started

<https://www.xilinx.com/products/design-tools/cloud-based-acceleration.html#sdaccellab>

115

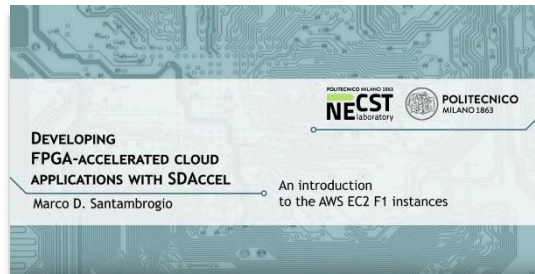
1127

2017

2018

Developers Trained
Companies + Academia

University Courses



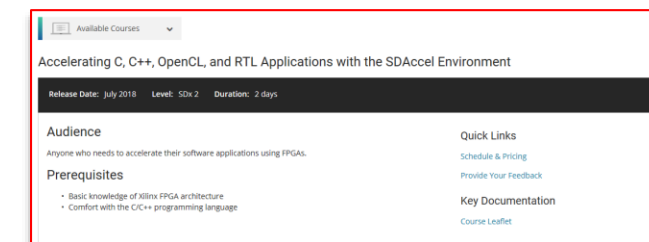
Prof. Zhiru Zhang, Cornell
High-level Digital Design
Automation Labs and project
offered on AWS F1, Fall 2018

Prof. Jason Cong, UCLA
Customizable Computing for Big
Applications, Fall 2018
Parallel and Distributed
Computing, Winter 2019

**Prof. Krste Asanovic,
UC Berkeley**
CS152 Computer Architecture
and Engineering, Spring 2018

eLearning & Instructor-Led Courses

eLearning Modules	Duration in Minutes		
	Lecture	Demo	Lab
SDAccel Introduction	20	-	-
SDx Tools Overview	20	15	60
Host Code – OpenCL Execution Model	20	-	-
Profiling	20	-	-
Optimization Methodologies	15	-	-
RTL Kernel Wizard	20	-	-
C based Kernels	15	-	-
C based Kernel Optimizations	15	-	-
Setting up SDAccel Environments for XBB	-	15	-



Acceleration In Education

Xilinx University Program



Accelerate Your Research on the AWS Cloud with Xilinx FPGAs

- Scalable infrastructure
- No tools or license setup
- Integrate with over 100+ AWS services
- Get started with AWS EC2 F1 instances

PROFESSORS

University Teaching and Research

- Get the latest Xilinx technology
- Attend a professor workshop
- Access teaching material
- XUP Professor Area...

STUDENTS

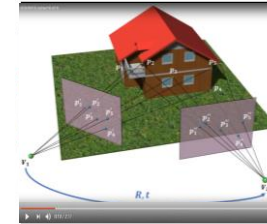
Class Room and Projects

- Download free FPGA design tools
- Purchase your own board
- Access technical resources
- XUP Students Area...

www.xilinx.com/xup

Open Hardware design competition EMEA 2018 AWS F1 Category Winner and Finalists

5 Points to Rule Them All
Winner: AWS EC2 F1 prize



Politecnico di Milano
Emanuele Del Sozzo, Marco Rabozzi, Lorenzo Di Tucci
(Prof. Marco D. Santambrogio)
[Project Link](#)

AWS EC2 F1: circFA




Politecnico di Milano
Peverelli Francesco, Zeni Alberto, Cabri Enrico
(Prof. Marco Santambrogio)
[Project link](#)

AWS EC2 F1: FastBrain




Politecnico di Milano
Filippo Carloni, Giada Casagrande, Valentina Corbetta
(Prof. Marco Santambrogio)


Acceleration Posters @ XDF




FireSim: Productive, Scalable, FPGA-Accelerated Cycle-Accurate Hardware Simulation using Cloud FPGAs
Sagar Karandikar, Howard Mao, Donggyu Kim, David Biancolin, Alon Amid, Borivoje Nikolic, Randy Katz, Jonathan Bachrach, Krste Asanovic.
Dept. of Electrical Engineering and Computer Sciences, UC Berkeley. Contact: sagark@eecs.berkeley.edu




Automata Processing on FPGAs
Chunkun Bo, Vinh Dang, Ted Xie, Jack Wadden, Mircea Stan, Kevin Skadron
Department of Computer Science, University of Virginia. chunkun@virginia.edu




DEMOCRATIZE ACCELERATED GENOMIC PIPELINES ON FPGA
Lorenzo Di Tucci, Giulia Guidi, Marco Rabozzi, Sara Notargiacomo, Marco D. Santambrogio
Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano (Milano). lorenzo.ditucci@polimi.it



Galapagos: A Full Stack Approach to FPGA Integration in the Cloud
Naif Tarafdar, Nariman Eskandari, Paul Chow
Electrical and Computer Engineering, University of Toronto. naif.tarafdar@mail.utoronto.ca

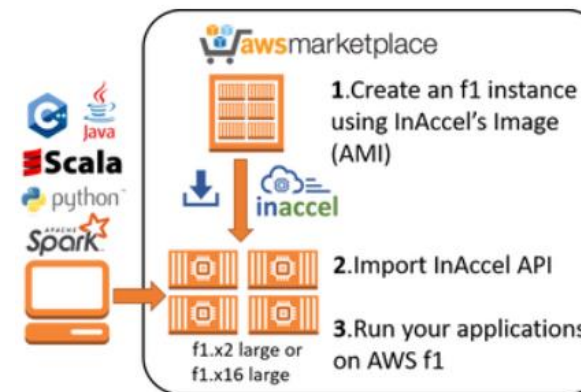


FPGA ACCELERATED BASEBAND FOR WIRELESS SYSTEMS
Chance Tarver, Kaipeng Li, Joseph Cavallaro
Department of Electrical and Computer Engineering, Rice University. {cat12, k33, cavallar}@rice.edu

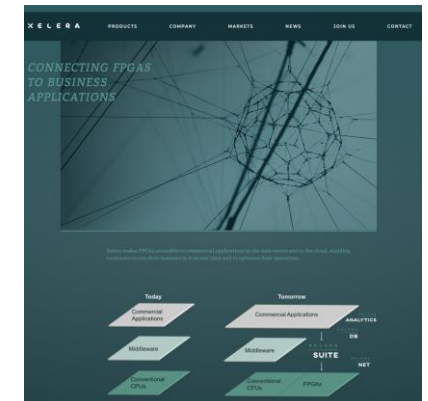


Rosetta: A Realistic HLS Benchmark Suite for FPGAs
Students: Yuan Zhou, Ritchie Zhao, Hanchen Jin
Faculty Advisor: Zhiru Zhang
School of Electrical and Computer Engineering, Cornell University

Accelerator Startups from Academia



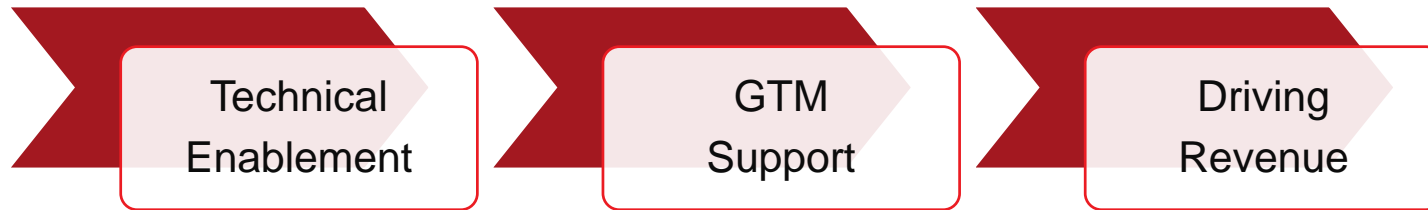
www.inaccel.com



xelera.io/

Xilinx Accelerator Program for Developers

Enable companies to accelerate products/services
on the cloud and on-premise



- >> Leverage your Existing algorithms and IP
- >> Deploy Custom Hardware to Millions in Public Cloud
- >> Extend your existing business model
- >> Discounted XBB cards for development
- >> Connect to Xilinx marketing, FPGA expertise and [funding opportunities](#)

www.xilinx.com/accelerator-program

43

2017

Accelerator Program
(Approved Partner)

268

2018

Accelerated Applications

Compression

CAST

Accelize

XILINX

Data Analytics

BLACKLYNX

XILINX

BigZetta
Systems

LegUp

Axonerve

Published Apps

15

2017

35

2018

Financial Computing

MAXELLER
Technologies
Maximum Performance Computing

SUMUP ANALYTICS



POLITECNICO
DI TORINO

Genomics

deSeq
Genetics

FALCON
COMPUTING

edico genome
an Illumina company

Image Processing

XILINX

CTACCEL
Accelerated Computing

ALUE
Advanced Logic Built-in for Electronics

Machine Learning

DEEPhi
深 鉴 科 技

XILINX

inaccel

mle
missing link electronics

Mipsology

Security

ZO
TECH

Titan
IC

SECURE-IC
THE SECURITY SCIENCE COMPANY

Video

NGCODEC
NEXT GENERATION VIDEO COMPRESSION

PATHPARTNER

skreens

Tool

XILINX
PLUNIFY

FireSim

Reconfigure.io



<https://www.xilinx.com/products/design-tools/acceleration-zone.html#libraries>

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XILINX

Xilinx ML Suite - Fastest Real Time Inference

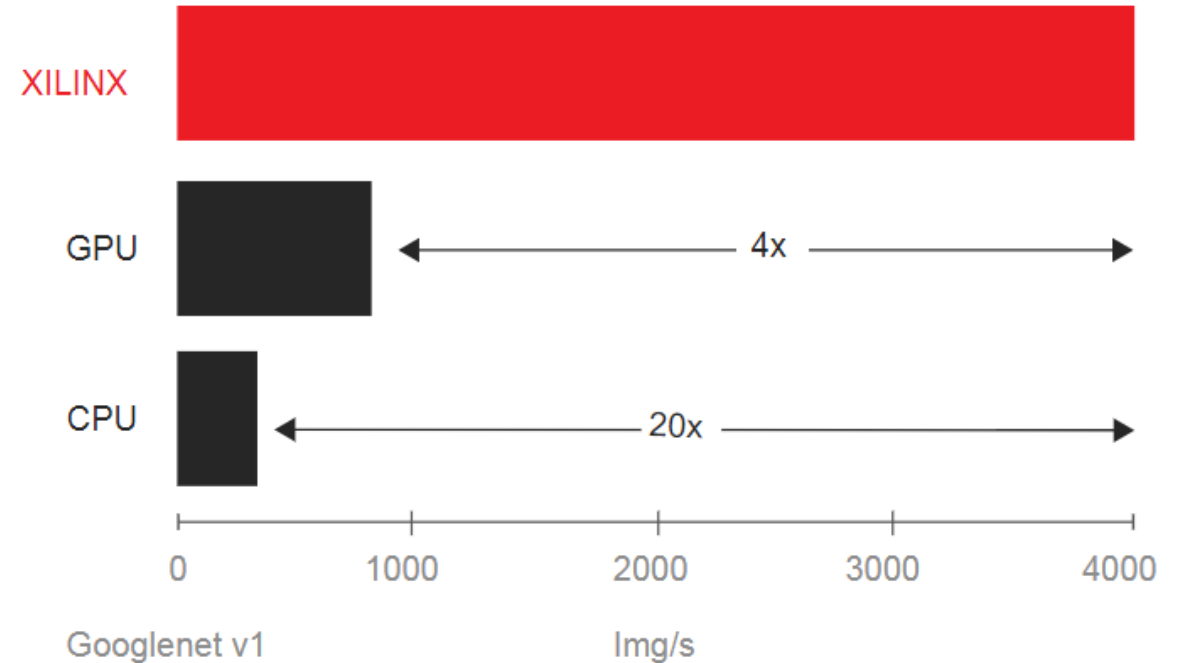
Your Application

{RESTful API} python™

TensorFlow mxnet Caffe

xfDNN

Compiler • Auto-quantizer
ML Software Libraries



* See [White Paper](#) for performance details



NIMBIX



Alveo
U200, U250

<https://www.xilinx.com/ml>

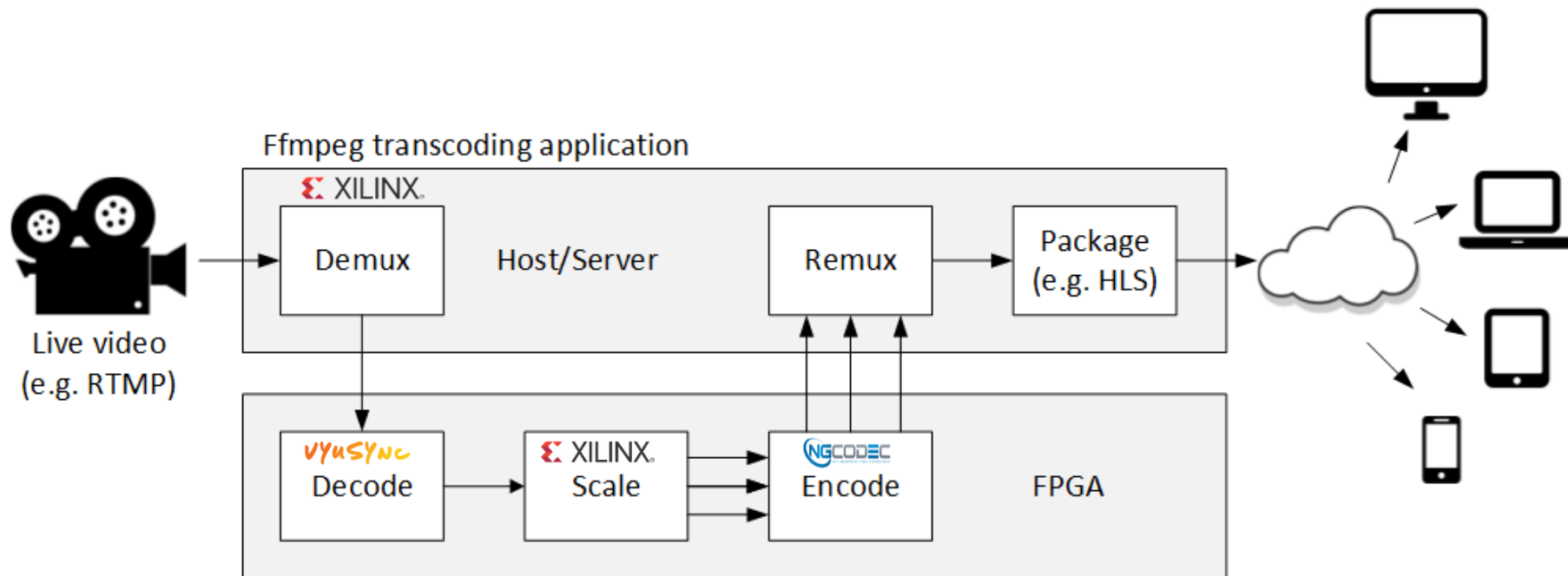
<https://github.com/xilinx/ml-suite>



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Xilinx ABR Video - Real Time Video Streaming



High performance HEVC and VP9 Encoder

Fully configured transcoding pipeline

Easy programming interface with FFmpeg

60 fps for real-time video streaming

7x greater than x265 slow

10x greater than Libvpx

Acceleration Resources

Developers

AWS F1 SDAccel Developer Lab

www.xilinx.com/products/design-tools/cloud-based-acceleration.html#sdaccellab

Data Scientists, ML Practitioners

AWS F1 ML Suite Developer Lab
(coming soon)

www.xilinx.com/ml

Academics

Sign-up for: AWS Educate,
Xilinx University Program

aws.amazon.com/education/F1-instances-for-educators/
www.xilinx.com/xup

Start-ups, IP Providers

Sign-up for:
Xilinx Accelerator Program

www.xilinx.com/products/design-tools/acceleration-zone/accelerator-program.html

Cloud End Users

AWS F1 Apps
and Libraries

www.xilinx.com/products/design-tools/acceleration-zone.html#libraries

On-premise End Users

Xilinx Alveo
Accelerator Cards

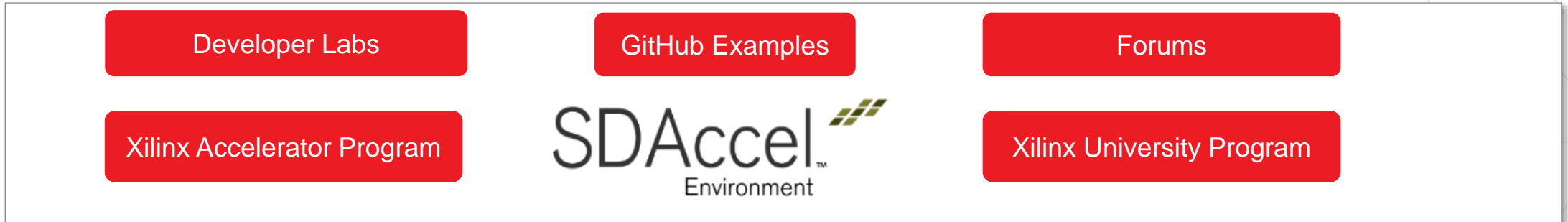
www.xilinx.com/alveo
www.nimbix.net/alveo

FPGA-based Acceleration Momentum

Accelerated
Apps



Developers



Acceleration
Platforms



