The Creation of Tomorrow’s Most Complex Technologies Starts Now

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Trends in Emulation and Prototyping

Increasing # of ASIC and SoC Starts
> Driven by AI / ML, 5G, Automotive, Vision & Hyperscaler ASIC & SoCs
> Impacted by evolving architectures, SW content, and complexity growth

New Emulation and Prototyping Product Categories
> Prototyping expected to grow faster than emulation due to increasing SW content
> Enterprise prototyping - Enhanced features enables rack-based prototyping

Emulation in Cloud
> To offload temporary ‘peak’ E&P capacity from on-premise to cloud-based
> Startups can lower initial E&P investment and scale compute resources
> Enables moving resources from CapEx to OpEx
Xilinx History
in Emulation and Prototyping Market

- Xilinx is the market leader in emulation and prototyping
  - #1 market share
  - Multi-generation Industry-leading technology

- Need for larger FPGAs continues
  - Becoming important to multiple markets
XILINX

Meet the World’s Largest FPGA

Virtex® UltraScale+™ VU19P FPGA
Virtex® UltraScale+™ VU19P FPGA

9 Million System Logic Cells
- Implementing larger, more complex ASIC/SoC technologies
- Enabling highly customized algorithms and applications

2,072 User I/Os
- Simplifying multi-FPGA design platforms
- Enabling scalability, debug, and real-world validation

80 28G Transceivers
- Enabling high port density test equipment
- Validating system design with emerging interface standards
The Highest Logic Capacity

1.6X Logic Capacity

Enabling Large-Scale ASIC/SoC Emulation & Prototyping

10 Arm® Cortex®-A9 CPUs
Virtex® UltraScale™ VU440 FPGA

16 Arm Cortex-A9 CPUs
Virtex UltraScale+™ VU19P FPGA
The Highest I/O Bandwidth

2,072 I/O Count

1.5Tb/s I/O Bandwidth

Enabling Scalability, Debug, and Real-World Validation

Memory for Storage/Debug
Multi-FPGA Interconnect
Real-World I/O Traffic

1.4X

1.4X

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The Highest Transceiver Bandwidth

80
28G Transceivers

4.5Tb/s
Transceiver Bandwidth

Enabling high port density test equipment with latest interface standards

1.7X

2.9X

(e.g., Bus Protocol Analyzer)
3rd Generation State-of-the-Art Development Platform

Designed from the ground-up for emulation-class design support

Tools & IP

- Automated design closure assistance
- Interactive suggestion and design tuning

Compile-Time & Quality-of-Results

- Multi-generation compile time improvement
- Distributed, parallel compile to shorten iterations

Robust Debug Support

- High-speed probes without re-compile
- Remote, multi-user debug

The Vivado® Design Suite in conjunction with the UltraFast™ methodology enables unmatched time to integration and implementation
Xilinx Continues Leadership in Highest Capacity FPGAs

- **VU19P**
  - 9M System Logic Cells
  - 3rd Gen SSI technology

- **VU440**
  - 5.5M System Logic Cells
  - 2nd Gen SSI technology

- **7V2000T**
  - 2M System Logic Cells
  - 1st Gen SSI technology
Summary

Three consecutive generations of the world’s largest FPGAs

Highest logic and I/O capacity for the most complex SoCs/ASICs

Industry-leading tools, IP, and design flows for low-risk, fastest time-to-market
Building the Adaptable, Intelligent World