

MOVING A GENERATION AHEAD WITH ALL PROGRAMMABLE FPGAS, SOCS, AND 3D ICs

At the 28nm node, Xilinx® introduced several new technologies that created an extra generation of value for customers and moved Xilinx a generation ahead of its competition. Rather than simply migrate the existing FPGA architecture to the next node, Xilinx introduced numerous FPGA innovations and pioneered the first commercial All Programmable 3D ICs and SoCs.

These All Programmable devices, all shipping today, employ "All" forms of programmable technologies—going well beyond programmable hardware to software, beyond digital to Analog Mixed Signal (AMS), and beyond single die to multi-die 3D IC implementations (Figure 1). With these new All Programmable devices, design teams can achieve greater degrees of programmable systems integration, increase overall system performance, reduce BOM costs, and get ever smarter, more innovative products to market more quickly.

STAYING A GENERATION AHEAD AT 20nm

PORTFOLIO
All Programmable FPGAs, SoCs and 3D ICs
Available today

All Programmable SoC

- First shipped: Q4, 2011
- Integrating FPGA, CPU, DSP, AMS
- Competitor silicon not available

All Programmable FPGA Family

- First shipped: Q1, 2011
- Delivering one extra node of power and performance

All Programmable 3D ICs

- First shipped: Q3, 2011
- Integrating 2x logic and SerDes bandwidth
- Competitor working only on test chips

At 28nm, Xilinx has expanded "programmability" beyond logic to create a line of All Programmable devices.

The transformation of Xilinx's product portfolio can be traced back to 2008, under the leadership of new CEO Moshe Gavrielov. Xilinx set in motion a comprehensive strategy to expand its technology portfolio, expand market reach, and move a generation ahead starting at the 28nm node. This included the go-ahead to commercially produce two entirely new classes of devices that Xilinx Labs and product-engineering teams had been prototyping and evaluating for years. The company also engaged with TSMC to create a new silicon process at 28nm called HPL (High Performance, Low-Power) tailored for the sweet spot of FPGAs with the optimal mix of performance and low power. Recognizing power as a top concern for customers, Xilinx implemented the entire All Programmable product line on this process (see cover story, Xcell Journal issue 76). Xilinx also assembled a first-class EDA design team to develop an entirely new, modern design suite. The goal was to not only boost customer productivity for the five different 28nm device families, but also to provide the scalability required for the next decade of All Programmable devices.

ZYNQ-7000 All Programmable SOC

The first of these new classes of devices, the Zynq-7000 All Programmable SoC (system-on-chip), is an EE Times Innovation of the Year award winner in addition to being an industry game-changing product. An All Programmable SoC combines three forms of programmability for mass customization: hardware, software, and I/O programmability. The idea of the device was born from the insights gained from a wide range of customer feedback through the many years and generations of delivering FPGAs that had soft- and hard-core processors on-chip.

Starting in the late 1990s, Xilinx and competitors began offering soft processor cores that customers could synthesize into the logic structures of FPGAs. In this way, design teams were able to closely link processing with logic functionality in the same fabric and achieve greater degrees of BOM cost reduction. In practice, many of these soft processors were used for embedded state machines, rather than running the OSes and software stacks typically associated with more complex systems. In the mid-2000s, as new semiconductor processes allowed FPGA vendors to offer higher-capacity devices, vendors began to improve the processing performance of these FPGAs by embedding hard processor cores alongside FPGA logic. Xilinx, for example, introduced the Virtex[®]-4 FX and later Virtex-5 FX families, each of which included a PowerPC[®] CPU core embedded alongside the FPGA logic.

While the Virtex FX families greatly improved processor performance over soft implementations, they required design teams to first program the FPGA logic before they could program the processor. Once the FPGA logic was programmed, the design team then needed to create their own peripherals, memory subsystems, and ultimately "embedded systems" and the associated plumbing to and from the logic. While expert design teams well-versed in FPGA design welcomed the resulting boost in processor performance, the architecture was counterintuitive to more popular, traditional embedded-system design methodologies. Learning from this experience, in 2008 Xilinx began architecting the Zynq-7000 All Programmable SoC and, equally important, the associated ecosystem—the firmware and software development tools and infrastructure—to facilitate the programming of the device.

For the Zynq-7000 All Programmable SoC, Xilinx chose the highly popular and well-supported 1-GHz ARM[®] A9 dual-core processor system, and worked with ARM to create the AXI4 interface standard to facilitate the plug and play of third-party, Xilinx, and customer-developed cores in the logic portion of the architecture. Xilinx also architected the Zynq family to boot directly from the processor. This allows system designers to work in a familiar fashion and helps design teams get an early jump on software development—speeding time-to-market. Because the processor boots first, even software designers not familiar with FPGA logic or hardware design can begin to use the device and perhaps expand their programming repertoire. Xilinx also gave the Zynq-7000 a rich set of peripheral IP and programmable, high speed I/O—delivering to customers not just an FPGA or an FPGA with a processor but all told, a truly All Programmable SoC.

Xilinx announced the architecture in 2010 to give customers and ecosystem partners a jump on product development. The company delivered the first All Programmable SoC to customers in the winter of 2011. One of the first customers to receive this device, a company that had been defining and developing their design using a Zynq emulation platform for more than a year, was able to get the design operating successfully within a few hours of receiving the silicon. Today, Zynq is in as much demand as the other Xilinx FPGA families, with most applications integrating systems functions that used to be done in separate CPU, DSP, FPGA, and AMS components. For details on the Zynq-7000 All Programmable SoC, read the March 2011 cover story in Xcell

Journal issue 75. As of September 2012, one company has announced plans to release a competitive device, but has yet to announce the delivery of silicon or a significant ecosystem to adequately support it.

All Programmable 3D ICs

The second of the radical new device classes that Xilinx pioneered at 28nm is what Xilinx calls “All Programmable 3D ICs.” Back in 2004, Xilinx Labs began to explore and eventually prototype the stacking of multiple silicon dice in single IC configuration as a way to go beyond the scaling limits of Moore’s Law to create new levels of programmable systems integration. Xilinx’s scientists created test chips of various 3D IC architectures, exploring alternative ways of stacking silicon dice and using through-silicon vias (TSVs) to both power the dice and support die-to-die communications. Through extensive prototyping and a view toward reliable manufacturing, the company concluded that the most practical near-term commercially viable architecture would be one Xilinx called “Stacked Silicon Interconnect” (SSI). In this architecture, multiple dice are placed side-by-side on top of a passive silicon interposer, which facilitates the interconnect/communication between the many dice. With more than 10,000 interconnects that can be programmed among the dice, along with programmability of each die and the I/O, Xilinx has created not only the first commercial 3D IC, but the first All Programmable 3D IC. To learn more details about the SSI technology, read the cover story in Xcell Journal issue 77.

In early 2012, Xilinx delivered the very first 3D ICs to customers. The Virtex-7 2000T device stacks four FPGA logic slices side-by-side. The device established a new record for IC transistor counts (more than 6.8 billion transistors) at the 28nm node and smashed the record for FPGA logic capacity, offering 2 million logic cells (the equivalent of 20 million ASIC gates). The device is double the size of the competition’s largest FPGA, essentially offering logic capacity that is a generation ahead of what one would have expected at that process node. What’s more, this SSI technology architecture will allow Xilinx to offer capacity that exceeds Moore’s Law for future-generation products as well.

The Virtex-7 2000T device has been tremendously well received by customers who have designed it into applications that include ASIC prototyping, storage, and high-performance computing systems. These applications all require the highest capacity of programmable logic the industry can offer. However, Xilinx has also extended its 3D IC technology to enable another innovation a generation ahead of the competition, targeted for the highest-performance applications in the communications market.

In the summer of 2012, Xilinx announced the Virtex-7 H580T, the first of three heterogeneous All Programmable 3D ICs tailored for the communications market (see cover story, Xcell Journal issue 80). Where the Virtex-7 2000T is a homogeneous 3D IC in that all four of its dice/slices are primarily composed of FPGA logic, the Virtex-7 H580T is the first heterogeneous 3D IC.

To make the Virtex-7 H580T, Xilinx placed a dedicated 28G transceiver die alongside two FPGA dice on the passive silicon interposer. In doing so, Xilinx is able to offer a device with eight 28-Gbps transceivers, forty-eight 13.1-Gbps transceivers and 580k logic cells. For applications such as a 2x100G optical transport line card based on a CFP2 optical module, the Virtex-7 H580T provides an astounding five-chip-to-one reduction in BOM and associated board area over previous implementations.

The Virtex-7 H580T is just the first heterogeneous 3D device Xilinx is delivering in its 28 nm family. The Virtex-7 H870T device comprises two eight-channel transceiver dice alongside three FPGA logic dice on a single chip, yielding a total of sixteen 28-Gbps transceivers, seventy-two 13.1-Gbps transceivers, and 876,160 logic cells on one chip. The Virtex-7 H870T device is targeted at the next generation in wired communications—the 400G market. Xilinx’s 3D IC technology will allow customers to begin development of 400G applications as the market begins to take shape and gain a significant market advantage—perhaps moving a generation ahead of their competitors.

The All Programmable 3D IC is yet another class of All Programmable device that has yet to see competition. Although one company recently announced it has produced a test chip with foundry TSMC, the company has yet to publicly announce the delivery of samples or production devices to customers.

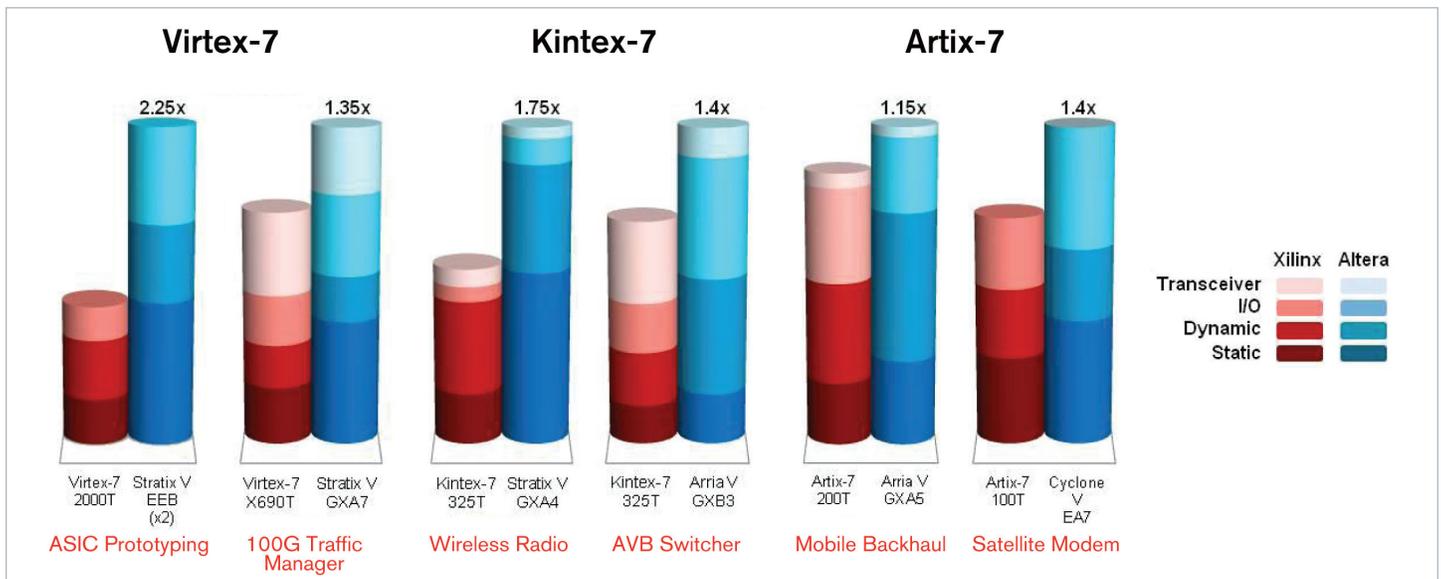
All Programmable FPGAs

FPGAs have come a long way since Xilinx introduced the industry's first FPGA, the 1,000 ASIC-gate-equivalent XC2064, back in November of 1985. The earliest FPGAs, positioned as an alternative to gate arrays and ASICs, were primarily used as “glue logic” to facilitate communications between two devices not originally meant to talk to each other, or to add last-minute functionality errantly left off the larger ASIC. Fast-forward to today and it is evident that modern devices have far outgrown the comparison to gate arrays. Today's All Programmable FPGAs include not only millions of gates of programmable logic, but also embedded memory controllers, high-speed I/O, and, increasingly, analog/mixed-signal circuitry. With yesterday's FPGAs, design teams could fix a problem in their system or “glue” elements together. With today's All Programmable FPGAs customers can create high-performance packet processing, waveform processing, image/video processing, or high-performance computing functions that can be reprogrammed dynamically in the system or upgraded in the field.

Where Xilinx has yet to see competition in the All Programmable SoC and 3D IC device markets, to move a generation ahead in the traditional FPGA market could be considered an even more impressive achievement. To accomplish this, Xilinx set in motion a clear strategy to be first to 28nm with FPGA silicon, with an expanded portfolio to cover low-end, midrange, and high-end requirements. Xilinx also set goals to differentiate all 28nm silicon with 1) a generation worth of advantages vs. the competition in system performance and integration, 2) an additional generation of power reduction, 3) a leapfrog in SerDes with the lowest jitter and unmatched channel equalization, and 4) a next-generation tool suite offering a step function in productivity and quality-of-result (QoR) advantages and scalability for the future.

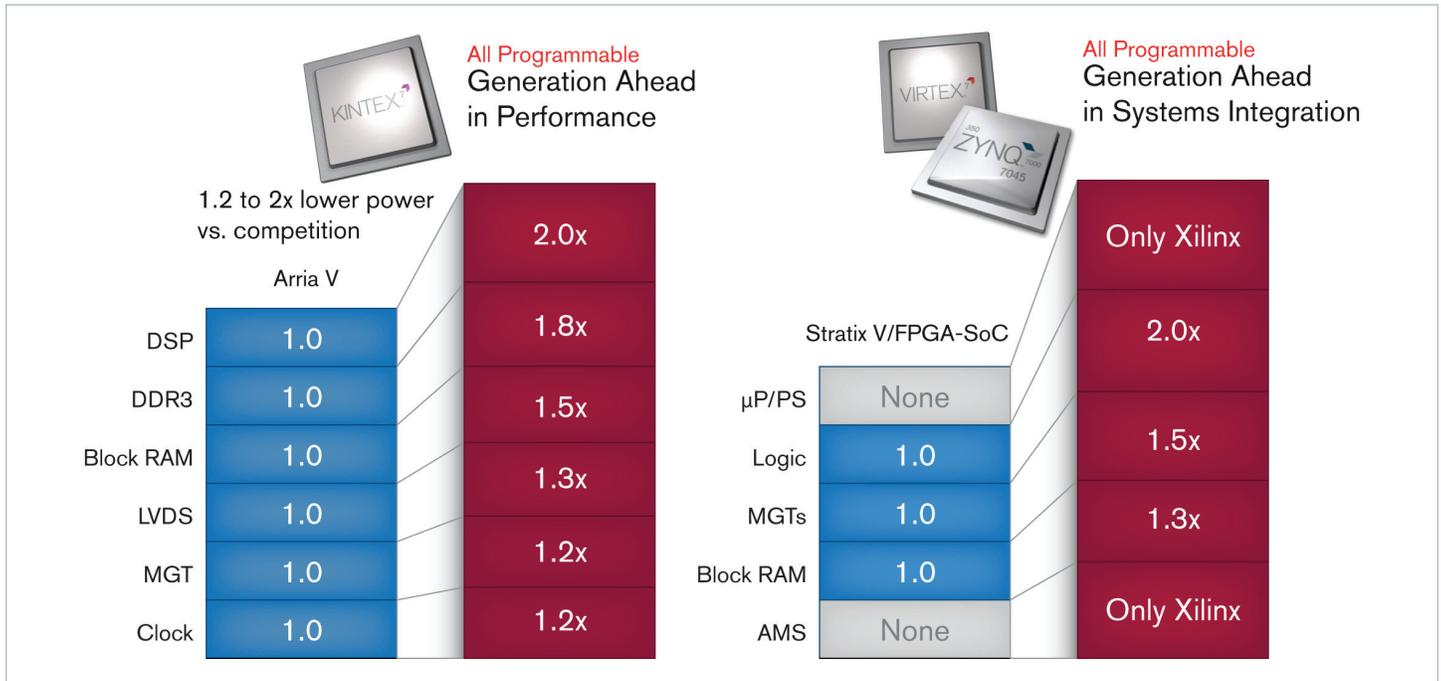
Xilinx in fact has already accomplished all of these tasks, delivering the first 28nm-family device (which happens to be the first of the midrange devices), the Kintex™-7 K325T, in March of 2011. Xilinx was actually the first company in the entire semiconductor industry to tape out 28nm silicon. Xilinx's decision to implement its entire 28nm line of All Programmable device on TSMC's HPL process, along with key architectural innovations targeting further power reduction, have enabled Xilinx to ship All Programmable FPGAs today to customers that deliver 35-50 percent lower power than competing devices running at the same performance levels—that's a generation ahead in terms of power efficiency (Figure 2). Xilinx's 28nm FPGAs also deliver unmatched performance and integration (Figure 3). The key contributors to system performance and levels of integration—including Block RAM, DSP, memory interfaces, transceivers, and logic elements—all outperform the competition by 1.2x to 2x, with an average of 1.5x. That's approximately a generation ahead.

TOTAL POWER REDUCTION BENCHMARKS



Customer designs show 35 percent lower power on average vs. the competition at the same performance.

STAYING A GENERATION AHEAD AT 20nm



Xilinx's 28nm FPGAs have a generation-ahead performance and integration advantage over the competition. The company has delivered its All Programmable devices to specifications with no errata to FPGA production devices.

What's more, Xilinx's All Programmable FPGAs have features that competing FPGAs simply don't have. For example, all of Xilinx's 28nm FPGAs include programmable Analog Mixed Signal blocks that further reduce BOM costs by supporting the implementation of analog system functions within the FPGA rather than by means of external discrete analog devices.

Productivity with Vivado

To improve designer productivity with its All Programmable devices at 28nm and beyond, Xilinx also developed from the ground up a next-generation design environment and tool suite, Vivado™ (Figure 4). This development took more than four years by the calendar, and 500 man years of effort. Without this design suite, design teams could not effectively leverage Xilinx's 3D ICs. For FPGAs and SoCs, the Vivado Design Suite further improves the quality of results of designs by up to three speed grades, cuts dynamic power by up to 50 percent, improves routability and resource utilization by over 20 percent, and speeds time to integration and implementation as much as fourfold. To learn more about Vivado, read the cover story in Xcell Journal issue 79.

Vivado is critical to enabling the new All Programmable portfolio of devices and levels of "programmable systems integration" they enable. As a result, there is a focus that goes beyond accelerating implementation flows and QoR, leveraging state-of-the-art analytical engines and closure automation. To enable significant levels of integration, Vivado includes support for hierarchy, IP packaging and reuse, automated IP stitching, and high-speed verification. To further speed time-to-market and raise the level of design abstraction, Vivado supports flows that start with C-based design and verification, and leverages high-level synthesis and automated AXI interface generation to speed the time from C to RTL IP creation and integration. In this way, Vivado not only accelerates time to implementation, but time to C and RTL integration at the front end of design.

28nm PRODUCTIVITY ADVANTAGE

Altera Quartus

Traditional RTL-based IP integration
with fast verification

Decade old implementation, database,
and engines

Xilinx Vivado

C and standards based IP
integration with fast verification

Hierarchical implementation and
advanced closure automation

28nm
Productivity Advantage

- More than 100x faster C Verification
 - More than 4x faster C to Verified RTL
 - 3-100x faster RTL simulation and hardware co-simulation
 - 4-5x faster IP reuse and time to IP integration
 - More than 4x faster design closure
 - More than 3x faster incremental ECO
 - 20% better LUT utilization
 - Up to 3 speed grade performance advantage
 - ~35% average power advantage at the same performance
- ✓ Up to 4x faster time to market
 - ✓ Up to 3x faster speed grades
 - ✓ One-third less power

Xilinx's Vivado gives designers a state-of-the-art design suite to vastly speed productivity and time-to-market.

Summary

Xilinx now develops "All" forms of programmable technologies—going well beyond programmable hardware to software, beyond digital to AMS, and beyond single-die to multi-die 3D IC implementations. Xilinx infuses these technologies into All Programmable FPGAs, SoCs, and 3D ICs, enabling design teams to achieve greater degrees of programmable systems integration, increase overall system performance, reduce BOM costs, and get more innovative products to market more quickly. The transformation of Xilinx's product portfolio can be traced back to 2008, with some innovations starting as far back as 2006. The result is a portfolio that today is delivering an extra generation of value for customers, and moving Xilinx a generation ahead of its competition.

As we look forward to 20nm, Xilinx is expanding on its leadership with even more advanced FPGAs, 2nd generation SoCs and 3D ICs, and the Vivado design system, enabling Xilinx to stay a generation ahead. Xilinx is benefiting from a multi-year head start in fine tuning SoC and 3D IC technology with customers, redefining how to develop and deliver critical core technology such as high speed serial transceivers, improving design methodologies and tools, expanding system level ecosystems and supply chains, and assuring both quality and reliability.

Take the NEXT STEP

To learn more about Xilinx's 28nm product development, please visit: www.xilinx.com/about/generation-ahead

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com



© Copyright 2012 Xilinx, Inc. XILINX, the Xilinx logo, Virtex, Spartan, ISE and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Printed in the U.S.A.